ASIC/FPGA Chip Design

Power Grid and Clock Design

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Outline

- Power Distribution Design
  - Introduction
  - IR Drop
  - Ldi/dt Drop
- Decoupling Capacitances
- Clock Considerations
- PLL/DLL Architecture

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Power Distribution Design

- Power means V_{DD} and GND
  - Not available easily at all locations in chip
- Clock should be routed from input pad to all flip flops
- Power Distribution (Multi-dimensional problem)
  - Off-chip
    - DC-DC converters
    - Power planes
    - Packages
    - Sockets
    - Power pins
  - On-Chip
    - Connection to the gates
    - On-chip distribution

Power Distribution Design

- Much of the complexity of power distribution systems arises due to the large number of transistors on a chip, the RLC nature of interconnect, and the frequency of operation.

- Today's state-of-the-art designs have the following specs:
  - Clock frequency: Over 1GHz
  - Power: over 100 W
  - Current levels: 100A
  - Supply voltage: 1.2V and below

- Fluctuations in the power system lead to timing variations and design failure

- **Rule-of-thumb:** For gates to functionally operate correctly max voltage noise/fluctuation on the supply should be less than 10% of (V_{DD}-GND)

Power Distribution Design

- Noise/fluctuation on the supply is due to resistance and inductance along the current path
  - IR Drop
  - Ldi/dt Drop at package pins

$$\text{Voltage Drop}: \Delta V = IR + L\frac{di}{dt}$$

- Voltage drops affects:
  - Clock Skew
  - Gate Performance
  - Clock Jitter
  - Overall timing and functionality

- Another dimension is about the **"power intensity"** issues
  - Power grid electromigration b/c of the large currents that affect long-term reliability

Power Supply Isolation

- Chips often contain
  - Noisy circuits
    - Pad-drivers
    - Clock generators
    - Large RAM arrays
  - Noise-sensitive circuits
    - PLLs and DLLs
    - Receive amplifiers
- We would like to isolate the noise sensitive circuits from the noise generated by the noisy circuits
- To do this we need to make sure the two circuits share as little of the power distribution network as possible
- Typically provide separate power and/or GND pins
  - Quiet GND and VDD

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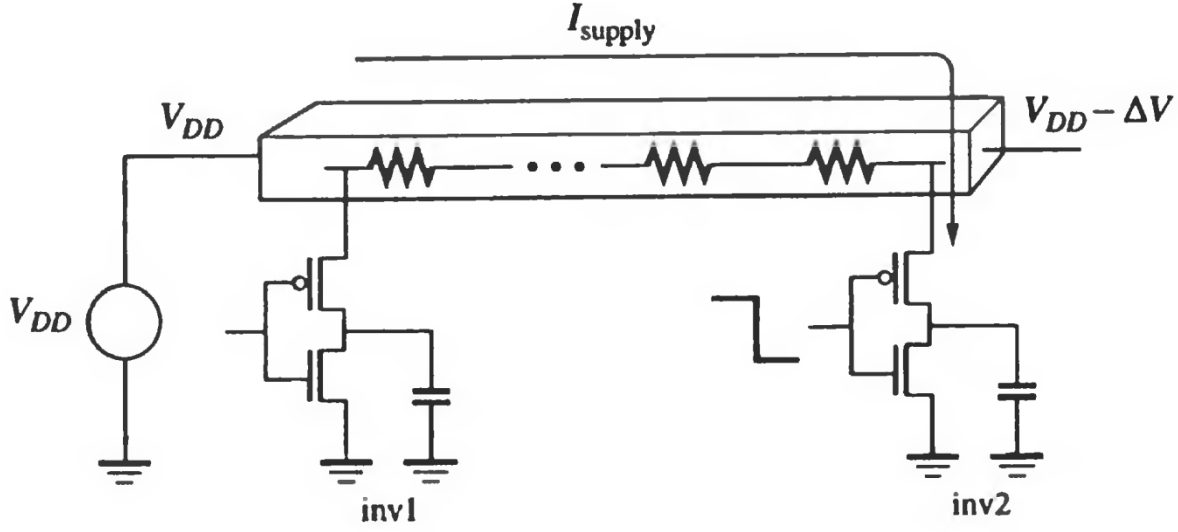
IR Drop

- IR drop is mainly due to the resistance on VDD lines.
- Basic concept with an example:
  - Two buffers connected to a resistive power supply
  - As the large driver, inv2, begins to switch, the demand for current reduces the voltage in the power grid.
  - The voltage remains high near the VDD connection at the periphery of the chip, but drops by ΔV at the connection to inv2.

IR drop reduces the VDD and increases the GND (ground bounce) over their respective paths.



IR Drop

- IR drop is caused by simultaneous switching of
  - Clock buffers
  - Bus drivers
  - Memory decoder drivers

- IR Drop Effects:
  1) Reduces the drive capability of the gates and increases the overall delay
     - A 5% drop in supply voltage can affect delay by 10-15%, which is serious when managing clock skews in the range of 100 ps.
  2) Compromises the noise margins of the logic gates due to the voltage drop in the power grid and increase in voltage in the ground grid.
     - VDD in deep submicron processes has been scaled down, which has resulted in very small noise margins. With IR drop, the margins are reduced even further!

How to avoid IR Drop?

- IR drop reduces the drive capability of the gates and increases the overall delay
  - Typically a 5% drop in supply voltage can affect delay by 10-15% or more!
  - Very serious when managing clock skews in the range of 100 picoseconds.

- To avoid IR drop:
  - Widen the lines that experience the largest voltage drops since increasing the width decreases the resistance (and the IR drop).
    - May not be always feasible due to the routing area constraints.
  - Add/remove metal straps.
  - Reduce buffer sizes if possible.

How to avoid IR Drop?

- The number of pins assigned to VDD and GND can also be increased to reduce IR drop. By providing more supply pins, the current requirements for a given section can be satisfied from a number of sources.
- This would limit the number of pins available for I/O.
- One effective solution may be to use a ball-grid array where the power supply connections can be placed at various points within the chip. The key design issue is the proper placement of the bumps around the chip.
- Note that solder bumps cannot be used in sensitive areas such as memories and dynamic logic as they generate alpha-particles that may cause logic value upsets on the sensitive nodes.

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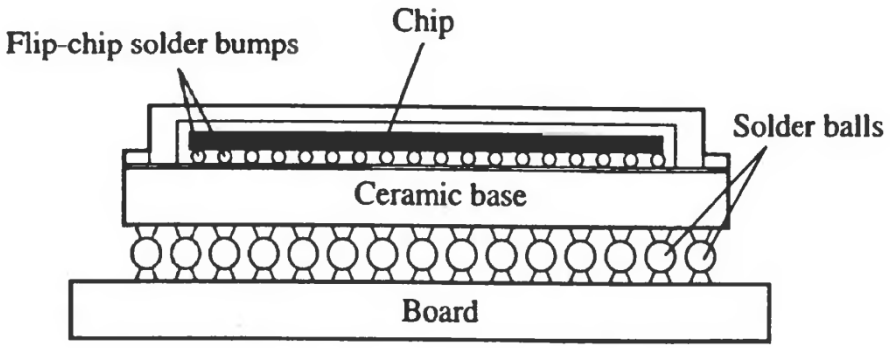
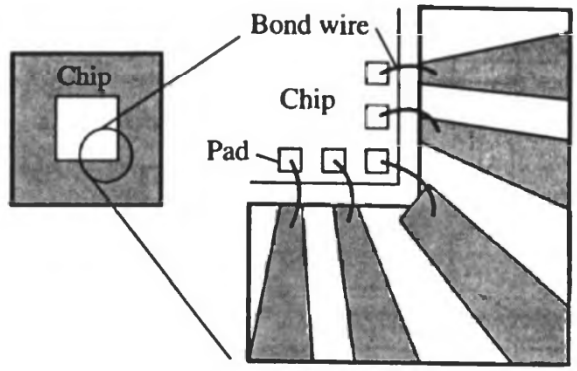
Ldi/dt Drop

- Ldi/dt drop is mainly because of the package pin inductance
  - Typically around 1-2 nH
- The inductance arises from the bonding wire used to connect the chip I/O pads to the lead frame in the traditional dual-inline package (DIP).
- Today many companies have moved to ceramic ball-grid array (BGA) packaging due to the large number of chip I/O and power/ground connections
- The inductance of each solder bump is of the order of 0.1 nH.



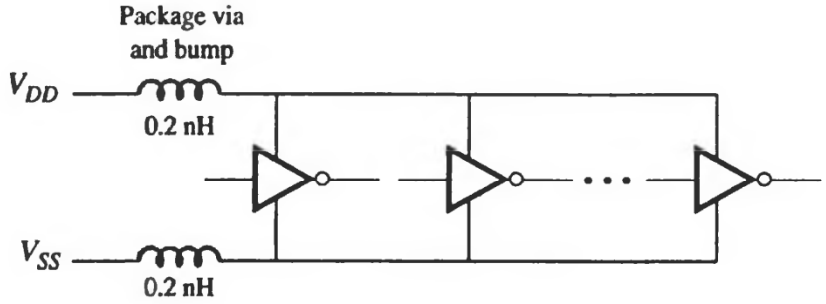
Ball Grid Array Packaging



DIP Packaging

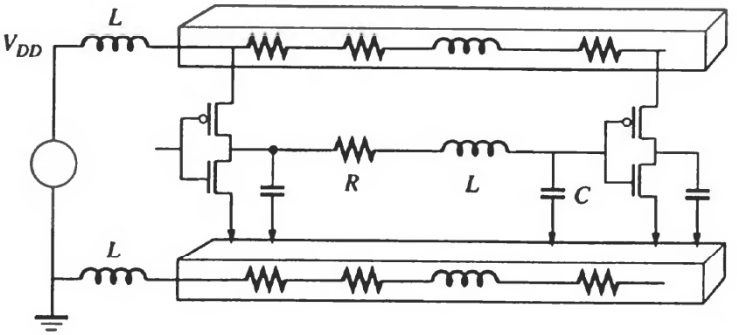
Ldi/dt Drop

❖ **Example:** A current level of 25mA is supplied by V_{DD} and flows into the circuit over a 100ps time interval. If the bump and via generate 0.2 nH of inductance, then the total voltage drop due to the inductance on both rails is



$$V_L = 2 \times L \frac{di}{dt} = 2 \times 0.2nH \times \frac{25mA}{100ps} = 100mV$$

- ❑ This is a significant drop considering that the supply voltage may only be 1.2V.
- ❑ General Case:
  - ➢ Packaging Inductances
  - ➢ Power Grid Inductance
  - ➢ Power Grid Resistances
  - ➢ RLC model of the interconnect



Electromigration

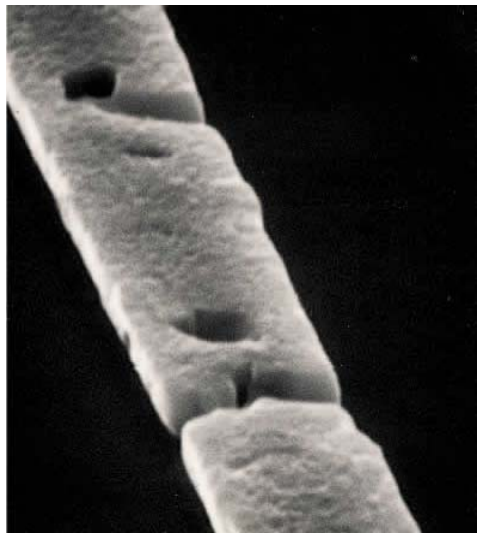
- The migration of metal molecules due to the high current densities and narrow line widths leading to a short or open in the metal line.

- Once electromigration happens, the chip may not operate properly

Electromigration

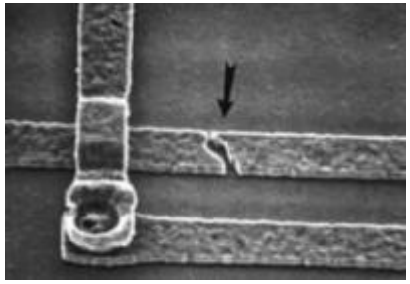
- The current density in each wire segment is computed using the wire dimensions (W: width, T: thickness)

$$J_{avg} = \frac{I_{avg}}{W \times T}$$



- The electromigration failure happens if:

$$J_{avg} > J_{max}$$



- The width of the metal segments with the failure should be adjusted to meet this criterion.

How to Avoid Electromigration ?

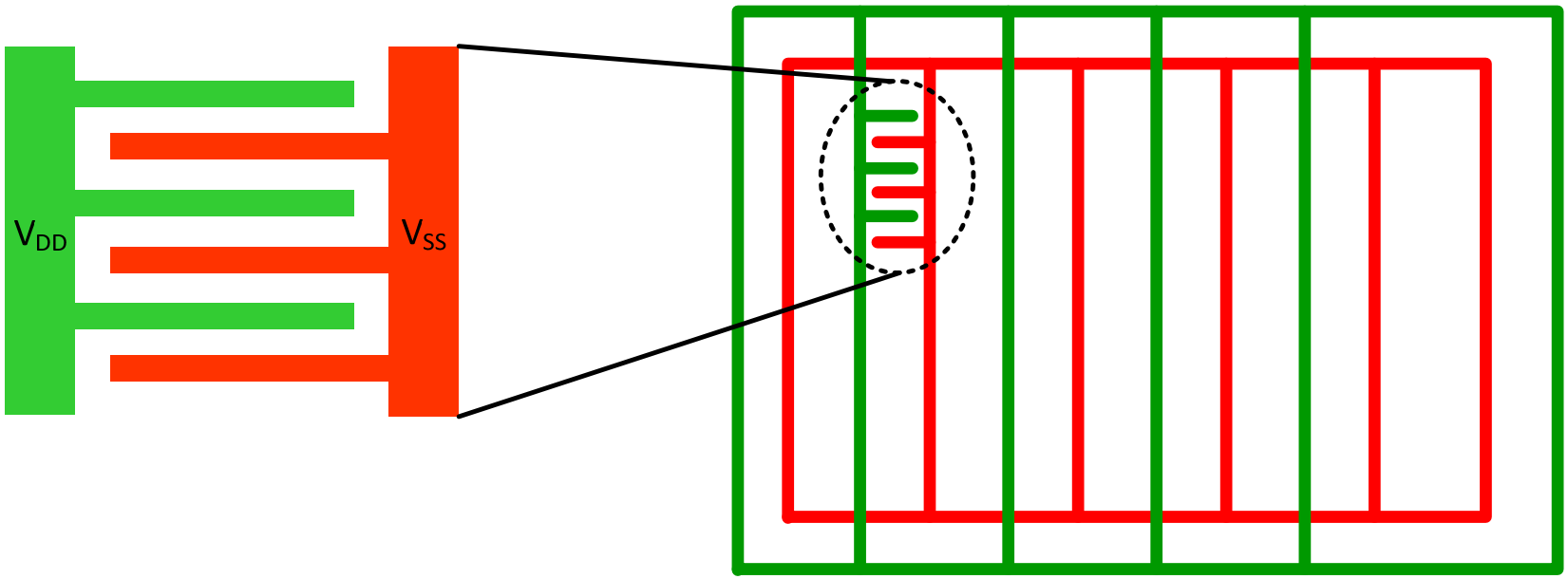
❑ The electromigration failure can be reduced in several ways. The basic idea in all approaches is to reduce the average current density experienced by any metal segment.

- The simplest approach is to widen the metal lines.
  - Costs area and can reduce yields.

- Changing the current flow in the power grid itself by adding jumpers and straps between different points in the grid.
  - It reroutes current from the affected areas but should be verified to confirm the problem has not been moved to another part of the chip.

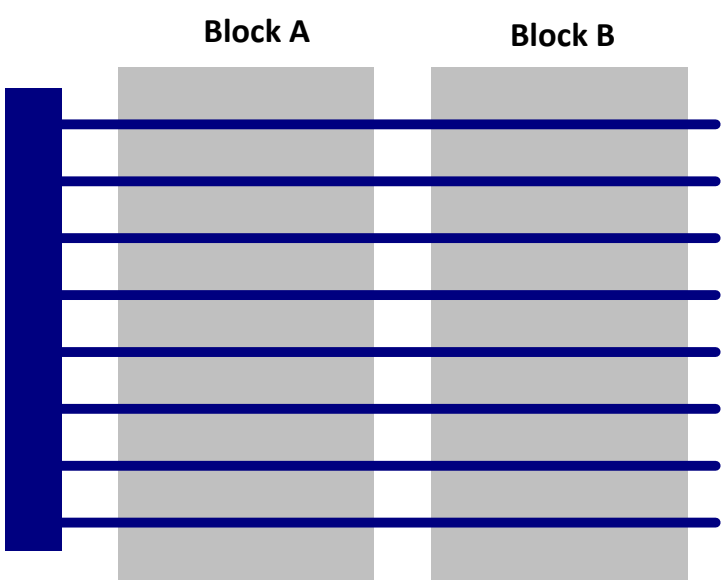
Power Routing Considerations

- An IC designer has to design a chip power system with having the IR drop, Ldi/dt drop and electromigration in mind.
- A simplified model for the power distribution:



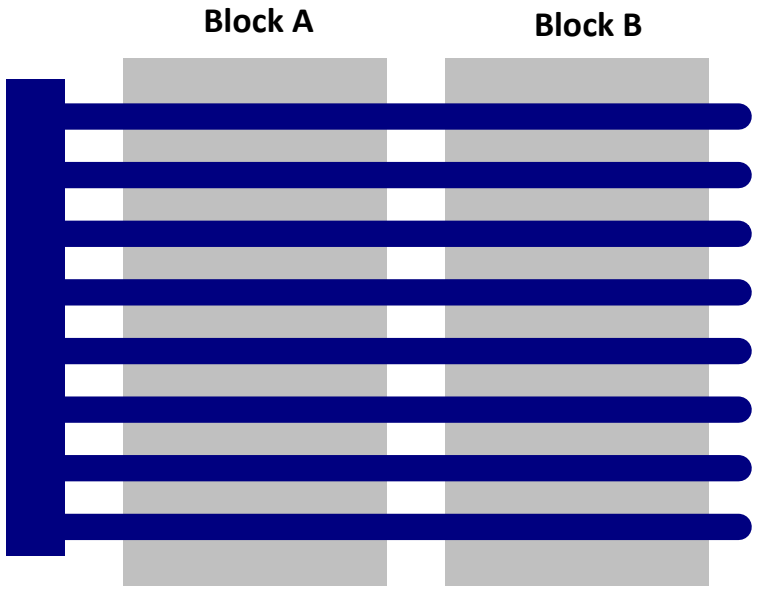
Power Routing Considerations

- Power routing options/strategies for several blocks:



- A large IR drop in block B
- Power consumed by A before it reaches B
- More blocks more complications

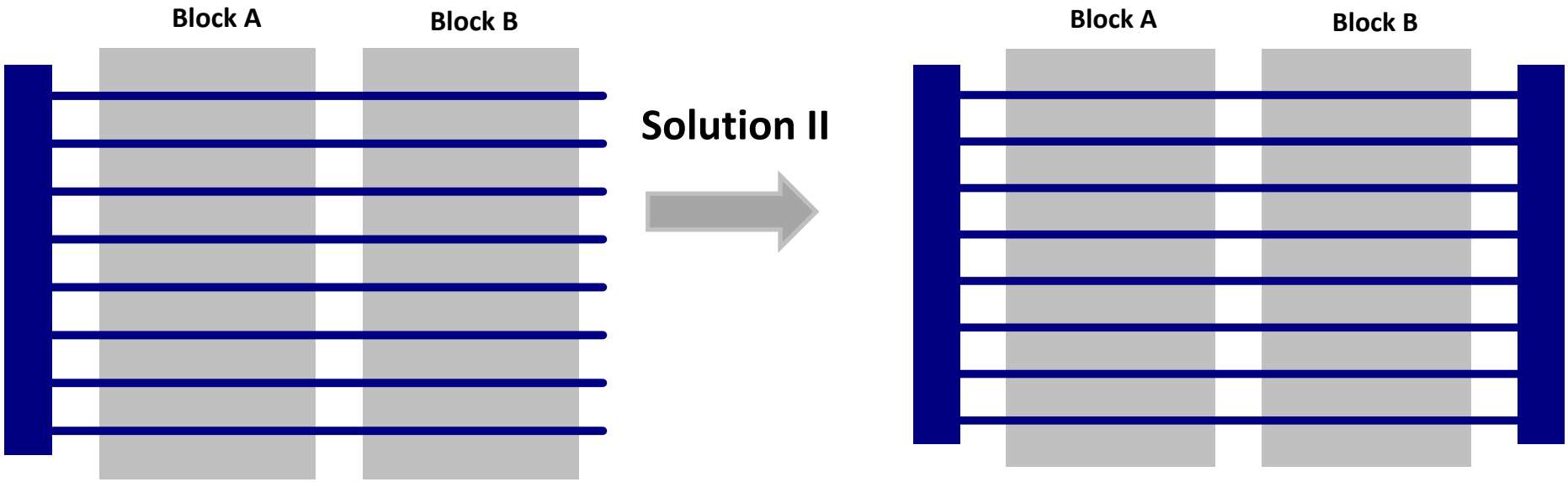
Solution I



- Larger metal trucks to handle the current
- Better power management (+)
- More silicon area required (-)

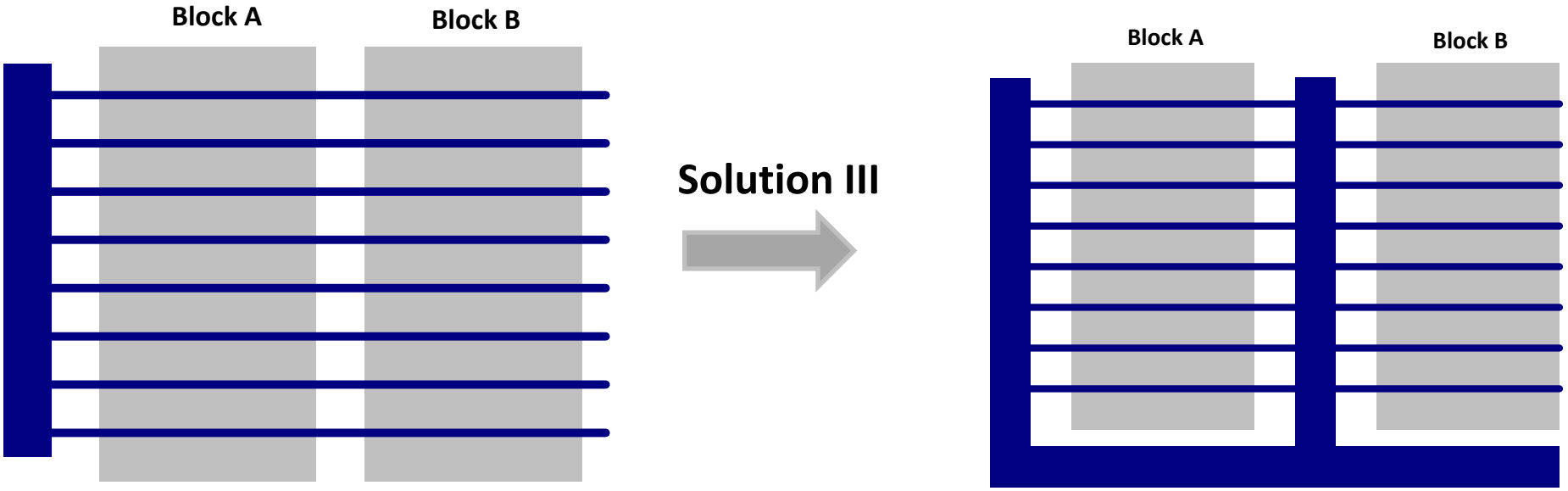
Power Routing Considerations

- Power routing options/strategies for several blocks:
  - Current from both sides of the block thus minimizing IR drop in the middle
  - Main trunks should be wide enough to handle current



Power Routing Considerations

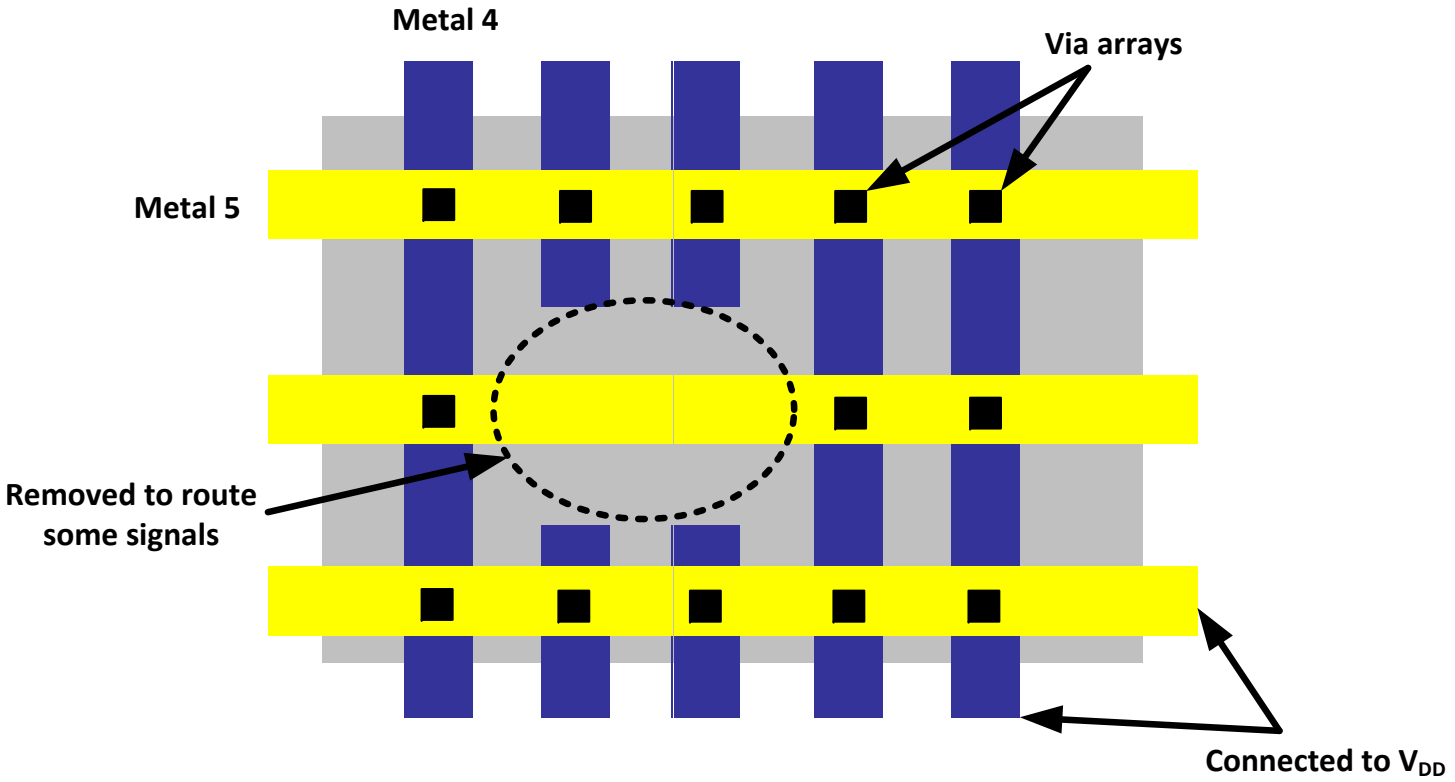
- Power routing options/strategies for several blocks:



- Main trunks should be wide enough to handle current
- Electromigration problem should be be checked in T junctions, which have a high current density, specially around the bends

Power Routing Considerations

- Power routing options/strategies for several blocks:
  - A grid of two metal layers



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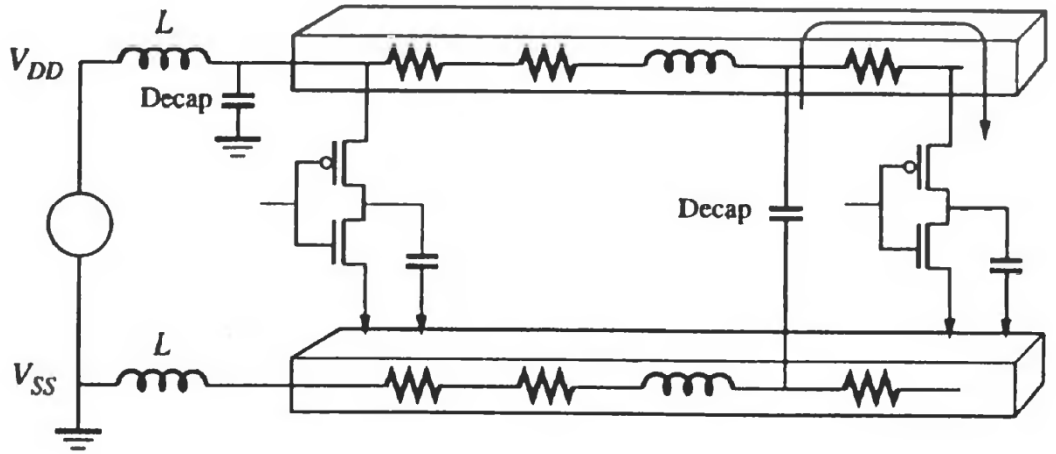
Decoupling Capacitances (Decaps)

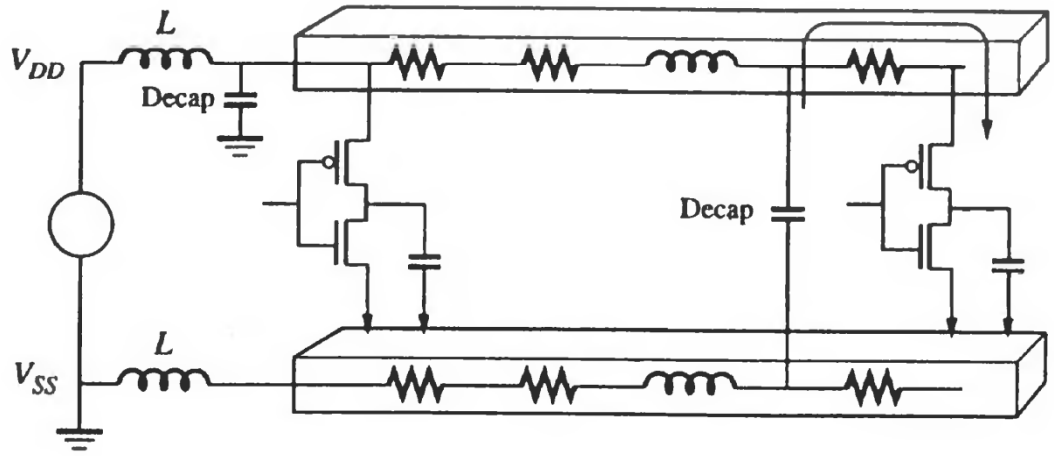
- On-chip decoupling capacitances (decaps) are commonly used to keep the power supply within the noise budget, especially during peak demand periods in high-frequency switching applications.
- **Decaps**: large-valued capacitances, holding a reservoir of charge, located near the power pins and any large driver.
- Decaps can reduce the amount of metal needed for distribution
  - Change peak requirement to average requirement



Decoupling Capacitances (Decaps)

❑ When large buffers switch from low to high, these decaps are the first line of defense for IR drop and Ldi/dt effects. The needed current for the switching process is obtained from the local decap.

❑ Later, current flows from the V_{DD} pad to refill the reservoir of charge for the next switching operation.



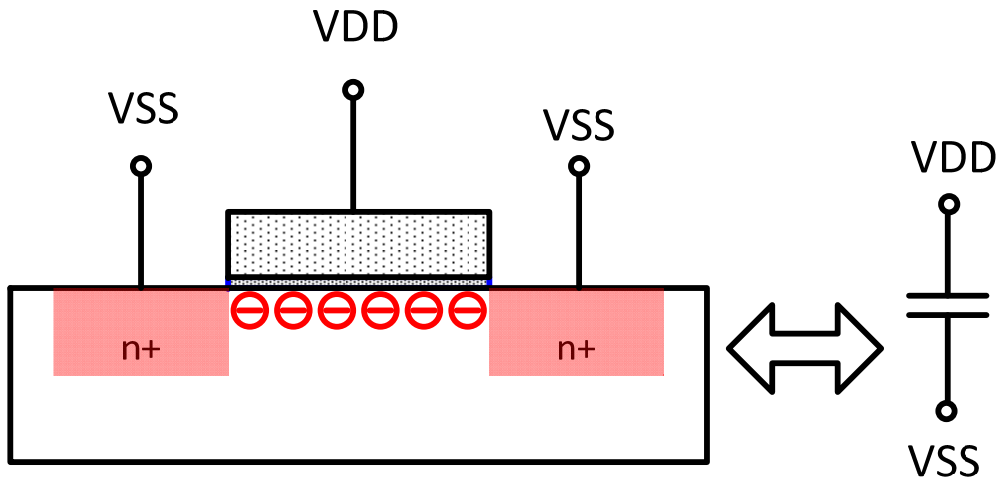
Decoupling Capacitances (Decaps)

- The on-chip decoupling capacitance is usually implemented using an NMOS transistor with the gate connected to V_{DD} and the S/D connected to V_{SS}.

- The device is therefore in the linear region of operation.

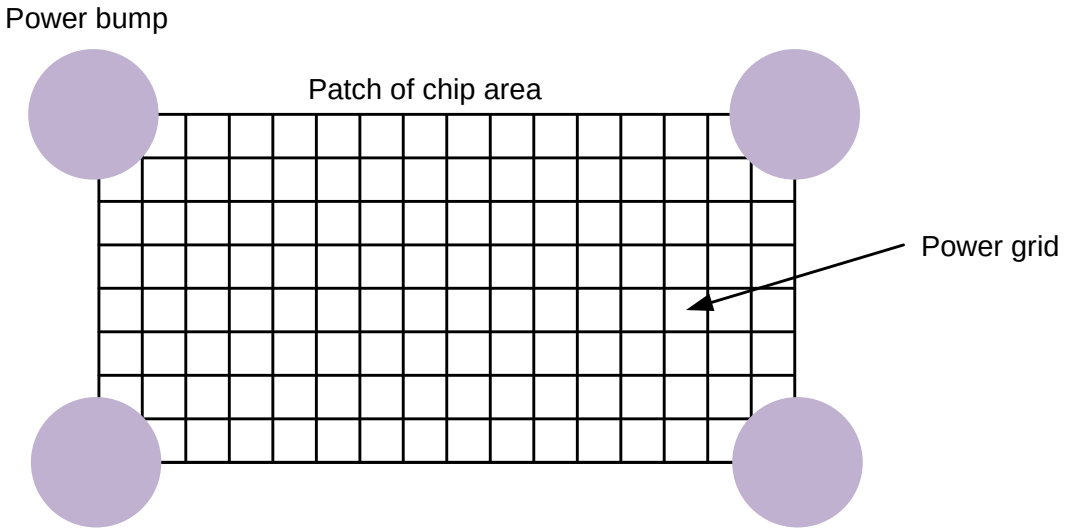
- The parallel-plate capacitor is formed by the poly on one side and the channel inversion layer on the other side.

$$C_{decap} = C_{ox}WL + C_{ol}W$$



Decoupling Capacitances (Decaps)

- The two main design issues are to decide how much decoupling capacitance to include and where to place them.
- These are determined through the large amount of simulations on the target chip.
- The location of the decaps should be based on the location of the large buffers that are switching during the peak demand periods.
- Simulations can be carried out on a representative patch of the power grid between power bumps, which are the solder bumps connected to V_{DD}.
- Any buffer and driver can be connected to the grid.



Decoupling Capacitances (Decaps)

- There are many factors to consider when deciding how much capacitance to employ and where to place them.

- There is a certain amount of decoupling that is already present in the circuit due to the devices that do not switch. This includes gate and S/D capacitances as well as wire capacitances for all nodes that are charged up to VDD. This value may be subtracted off the target decoupling capacitance needed in the circuit. (Symbiotic Bypass Caps.)

- The decaps are placed near the power pins to offset any effect of inductance due to solder bumps or bonding wires.

- The decaps should be placed in as many open areas of the chip as possible.

- Normally the amount of decoupling capacitance used is 10 times the amount of capacitance switched on every cycle.

Decoupling Capacitances (Decaps)

- We need a bypass capacitor of about 0.25nF for each 1mm^2 area of the chip

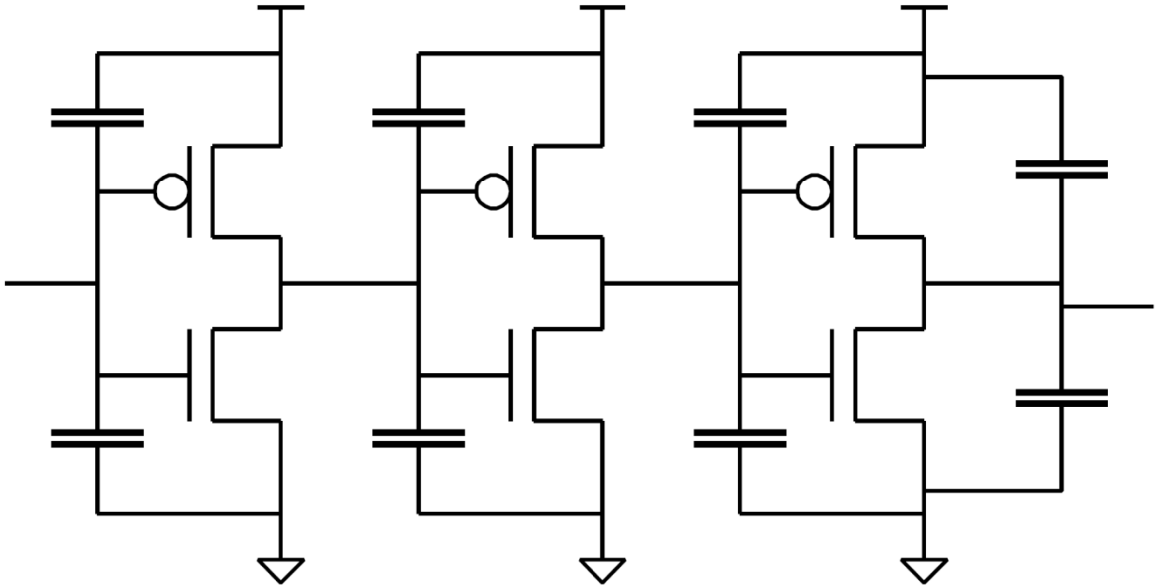
- For comparison, an MOS capacitor covering a 1mm^2 area has a capacitance of about 5nF/mm^2

- So, our bypass capacitor uses 5% of the silicon area!

- Can be made much smaller with local regulation

Decoupling Capacitances (Symbiotic)

- Where are the bypass capacitors in this picture?
- Gates that are not switching at a given instant in time act as symbiotic decaps
- If only one gate in 60 switches at a given instant, the bypass capacitance is 30 times the switched capacitance



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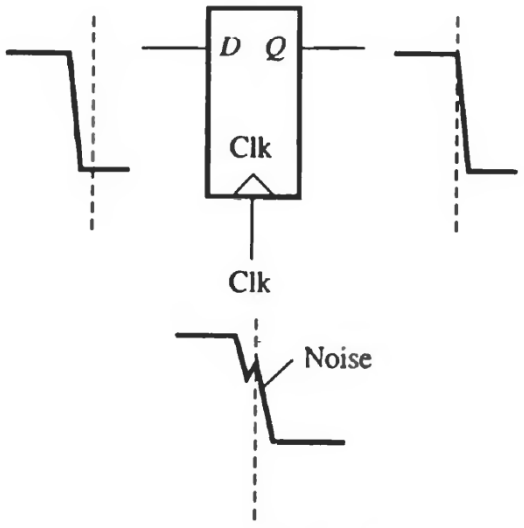
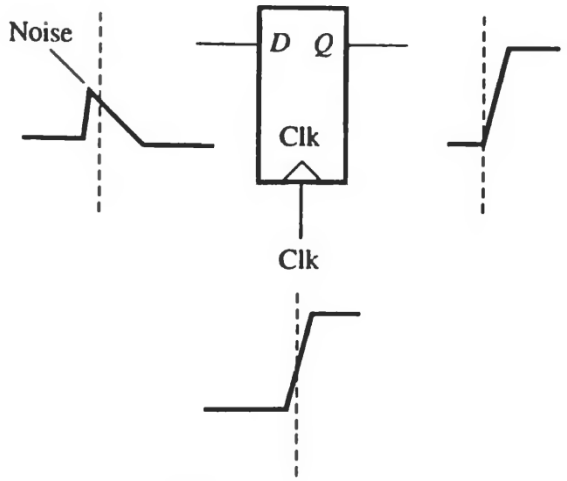
Noise on Clock



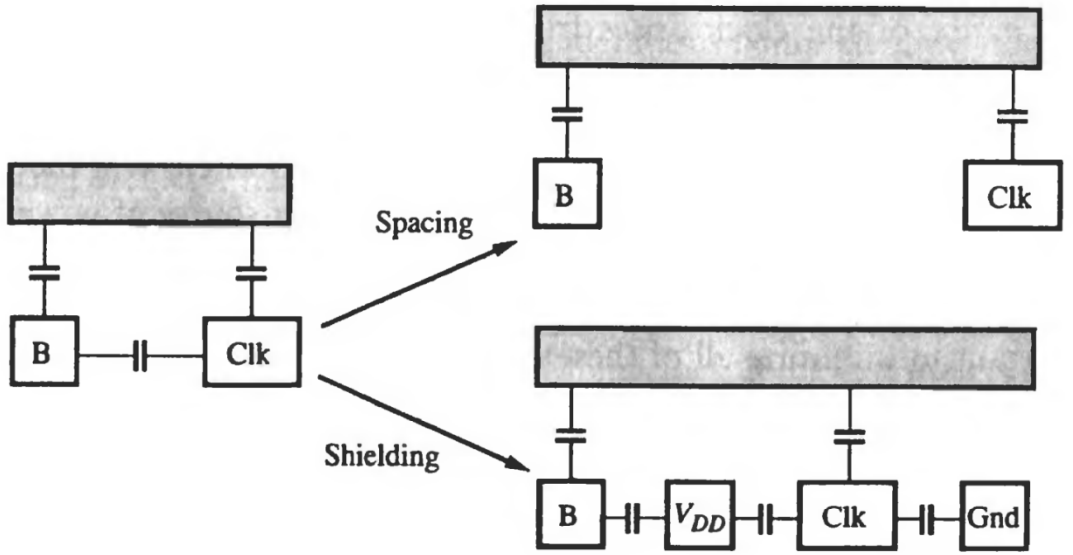
Glitch on Clock input



Glitch on data input

Noise on Clock: Layout solutions to coupling

- There is a potential for noise events due to the coupling capacitances.



- The spacing has a lower capacitance and thus reduces power to some degree.
- Shielding is beneficial for both capacitive and inductive coupling. Typically clocks are shielded to protect them from unwanted noise and also to protect other sensitive signals from mutual coupling to the clock.
- The price of shielding is the increased capacitance and power dissipation.

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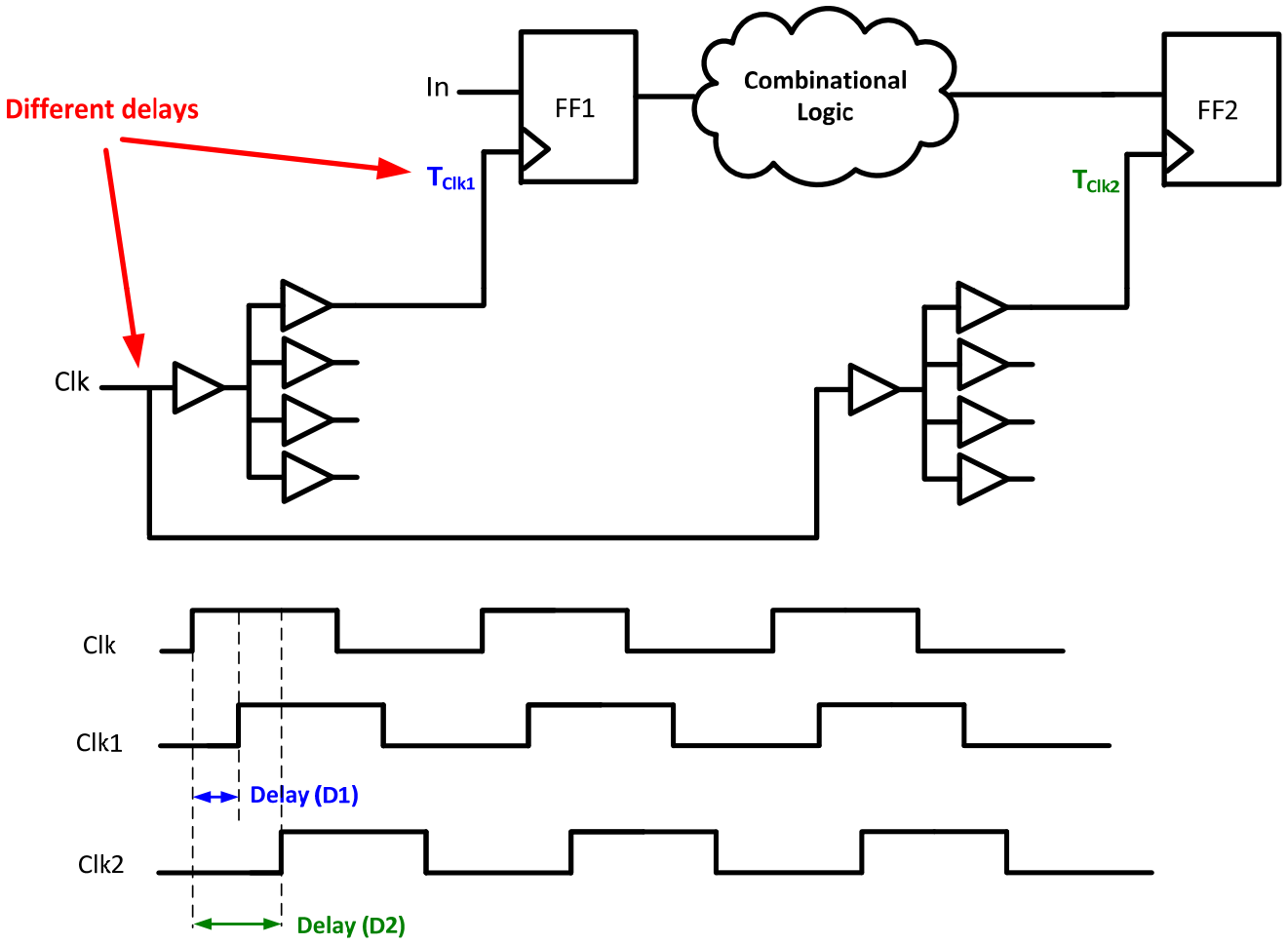
Clock Synchronization with PLL & DLL

- Remember that clock buffers are used to route clock, which incurs clock delay/latency
- Synchronization of an externally supplied master clock with the internal clock of the chip.
- Synchronization is needed:
  - When a master clock is distributed to several chips on PCB
  - To synchronize a local clock with an external clock because the data transfers are synchronized with the local clocks, data may be sampled at a wrong time
  - Clock latency value may differ from chip to chip or module to module
- Synchronization is done using phase-locked loop (**PLL**) or delay-locked loop (**DLL**).
- PPL are mainly used for:
  - Locking to external signals
  - Phase control
  - Frequency multiplication
  - Frequency division

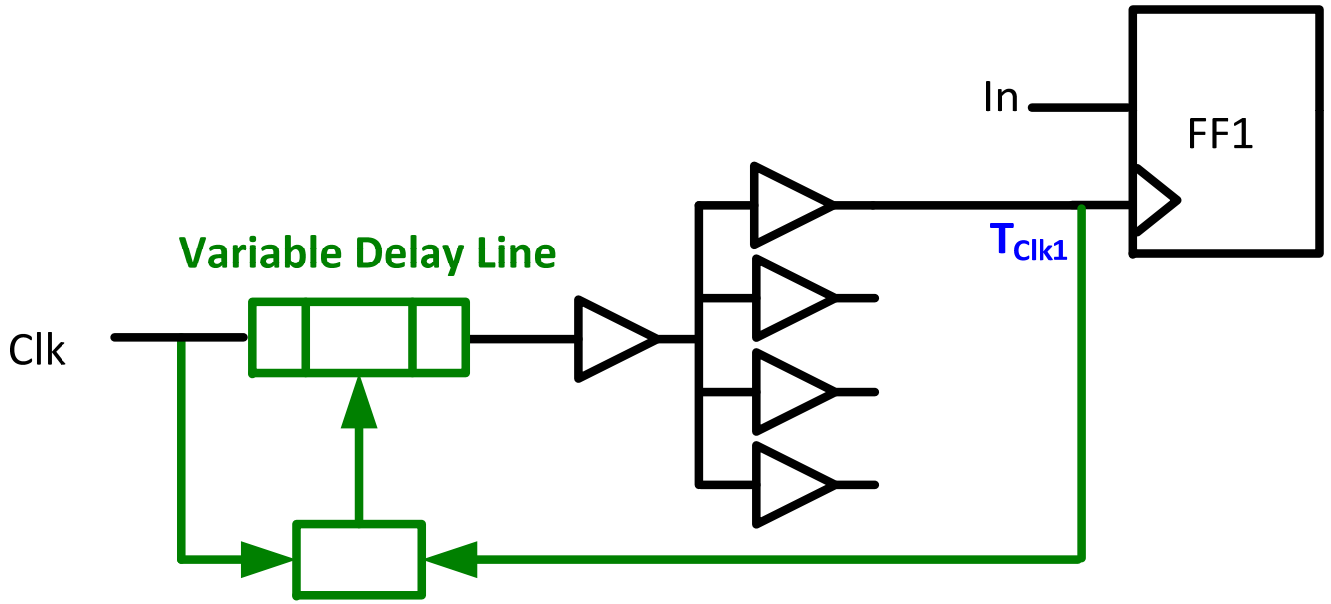
Clock Synchronization with PLL & DLL

- Clock latency between different points in design



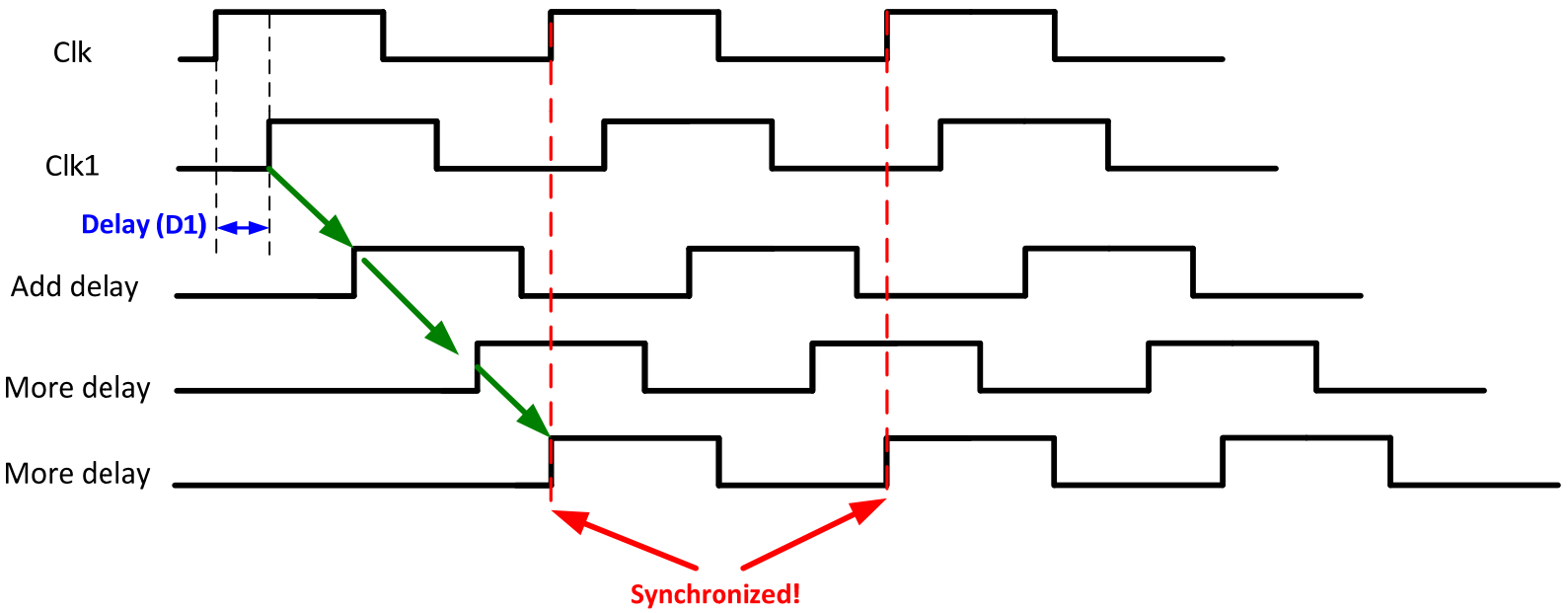
PLL/DLL Idea

❑ Create enough delay to match the phase/delay of the master clock with the local clock through a feedback line. (insert enough delay to clock line up!)



PLL/DLL Idea

❑ Create enough delay to match the phase/delay of the master clock with the local clock through a feedback line. (Insert enough delay so that clocks line up!)



PLL & DLL

- DLL and PLL circuits are closely related. Both use feedback control to lock output clock to the incoming clock.
- PLLs must lock on to the frequency and phase of the reference clock
- DLLs simply lock to a constant phase of the reference clock
- Therefore, locking process in a PLL requires more time than a DLL
- If we simply want synchronization, we could use a DLL
- If we needed the internal clock to run at a multiple of external clock frequency we must use a PLL

PLL & DLL in FPGAs

- Most FPGAs have PLLs and DLLs already designed in their hardware, which can be instantiated as a core to your design.

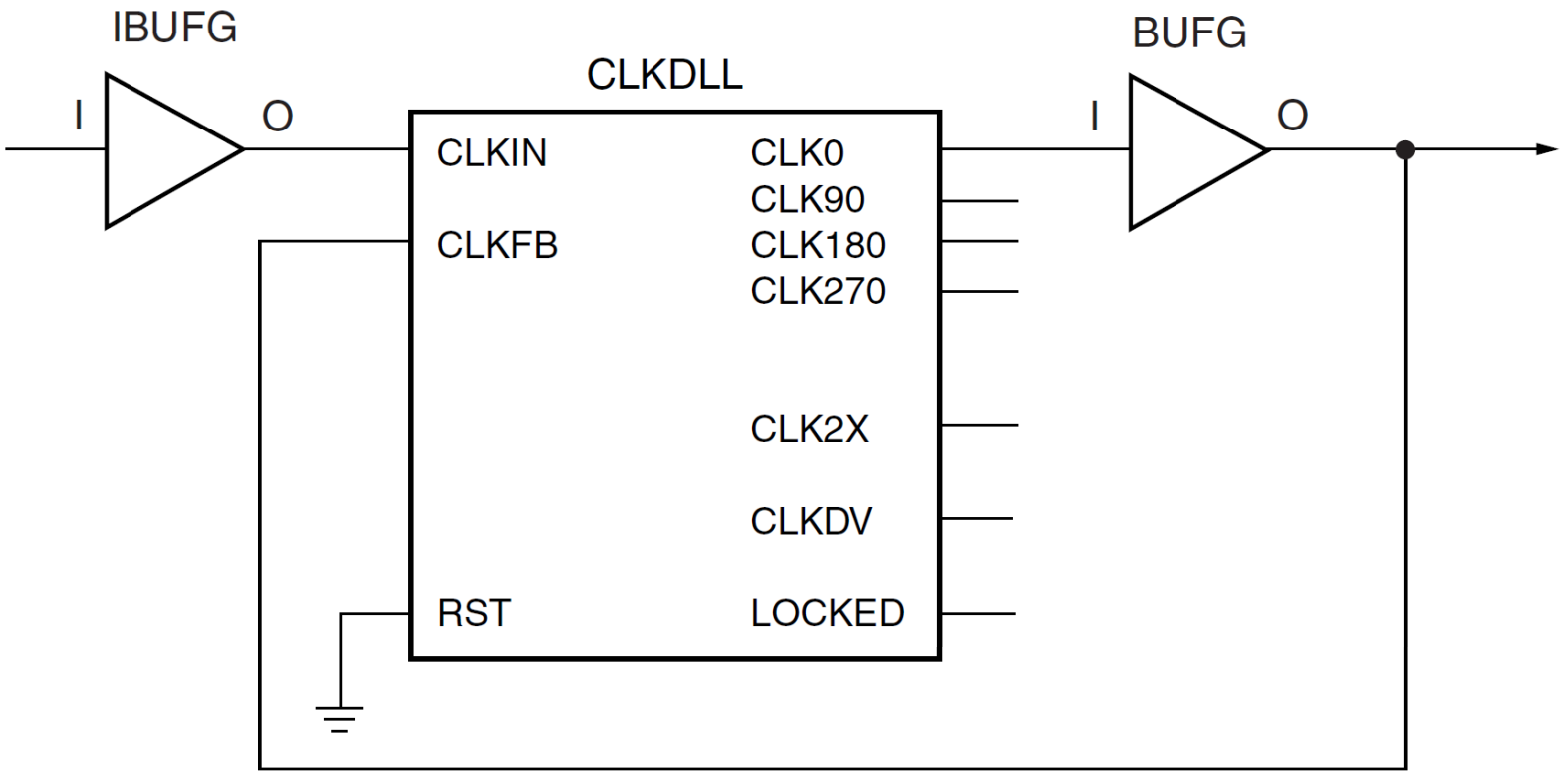
- For instance, Virtex has up to 8 fully digital DLLs that provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

- In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or can divide the user source clock by up to 16.

- Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design b/c the clock path on the board no longer distributes such a high-speed signal.

PLL & DLL in Virtex FPGAs

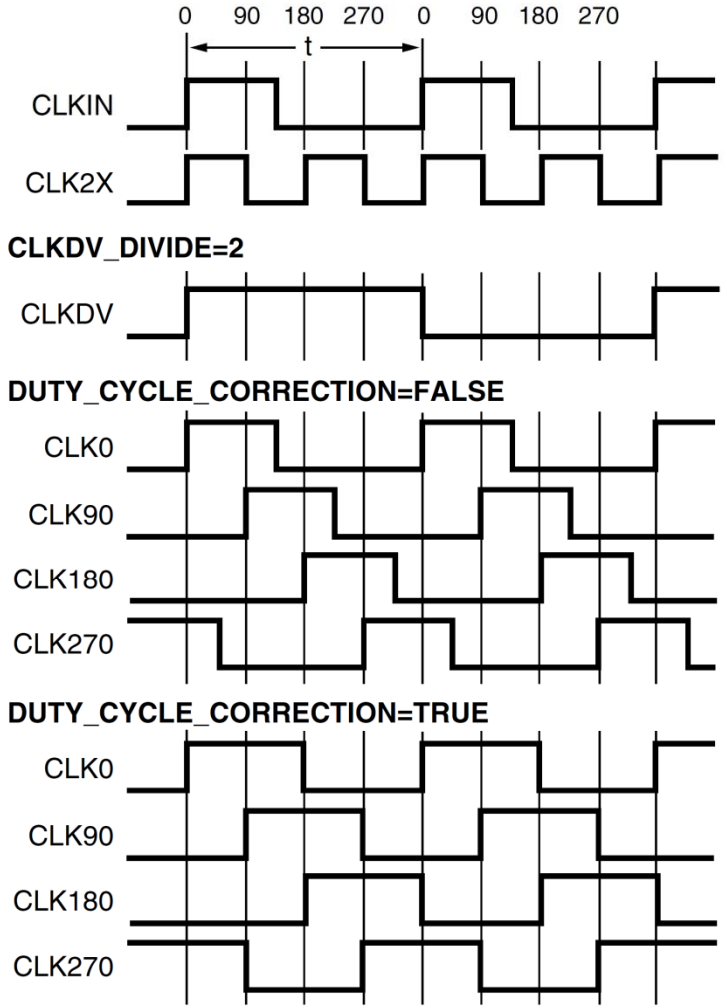
- CLKDLL



PLL & DLL in Virtex FPGAs

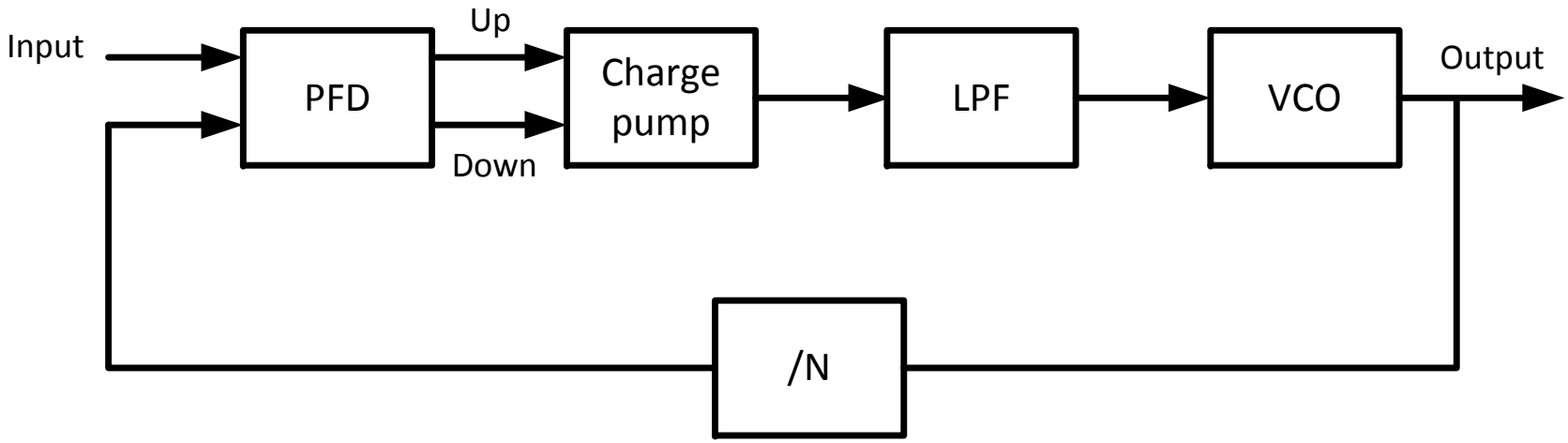
- Various possible outputs:

- The DLL clock outputs can drive a buffer, a global clock buffer, or they can route directly to destination clock pins



PLL/DLL Architecture

- A PLL consists of:
  - Phase/frequency detector (PFD)
  - A charge pump
  - A loop filter (LP)
  - A voltage-controlled oscillator (VCO)

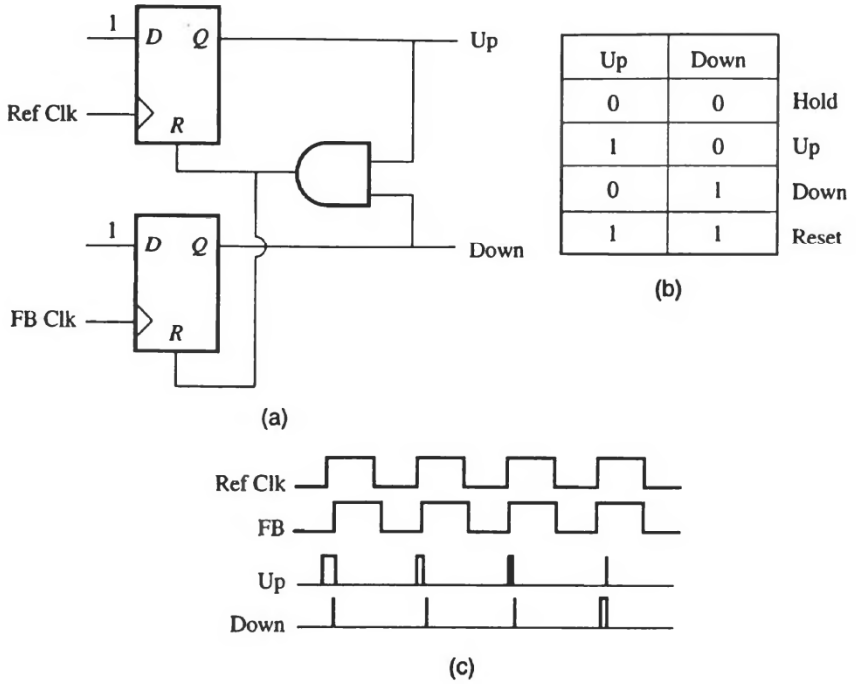


PLL/DLL Architecture : PFD

- The phase/frequency detector detects the difference between the edges of the reference clock and the feedback clock.
- The role of this block is to control the VCO by moving its frequency up or down depending on the edges of the incoming clocks.

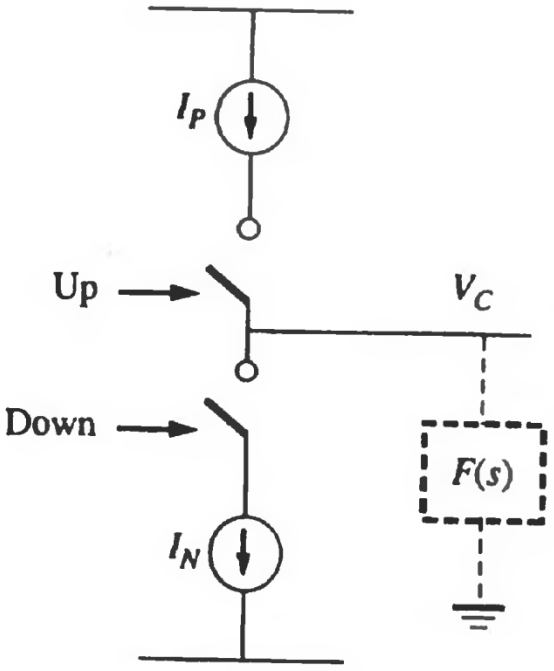
- If the feedback clock switches ahead (behind) of the reference clock, a down (up) signal is generated to slow down (speed up) the VCO.

- If both up and down are high, it is viewed as a reset condition.



PLL/DLL Architecture : Charge Pump

- Up/down signals are applied to a charge pump.
- The up signal will switch on the upper current source and raise the output voltage.
- The down signal will discharge the output capacitance and lower the control voltage.
- In case that both are high, the current flows harmlessly from VDD to GND.



PLL/DLL Architecture : Loop Filter

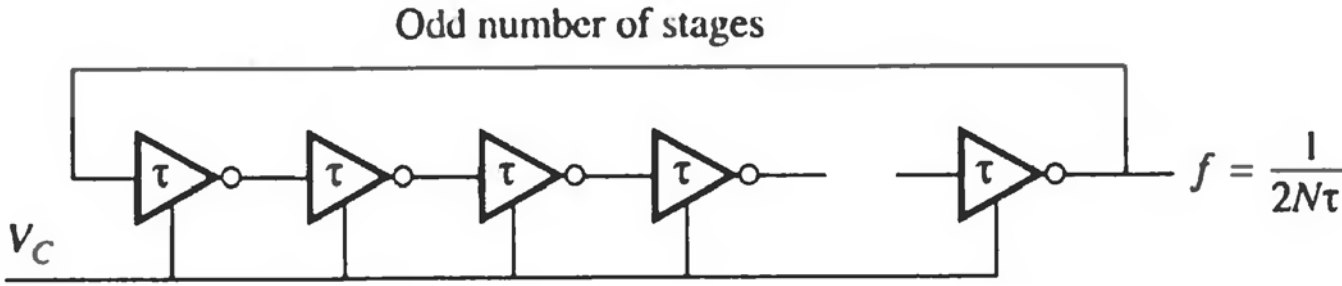
- The filter F(s) determines the order and stability of the overall PLL system. Its role is to filter out the high-frequency switching components in the up/down signals and deliver a slowly changing control voltage to the VCO.

- Can be modeled using a linear system.

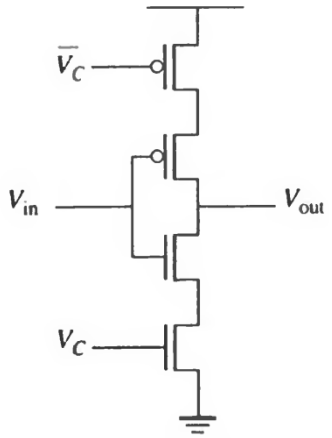
- The phase is the loop variable and the phase difference is determined and amplified.

PLL/DLL Architecture : VCO

- VCO acts as an integrator and generates a periodic output based on a control voltage input.
- Basic principle: a ring oscillator with a controllable delay τ
- The delay of each stage is adjusted by the control voltage V_c.

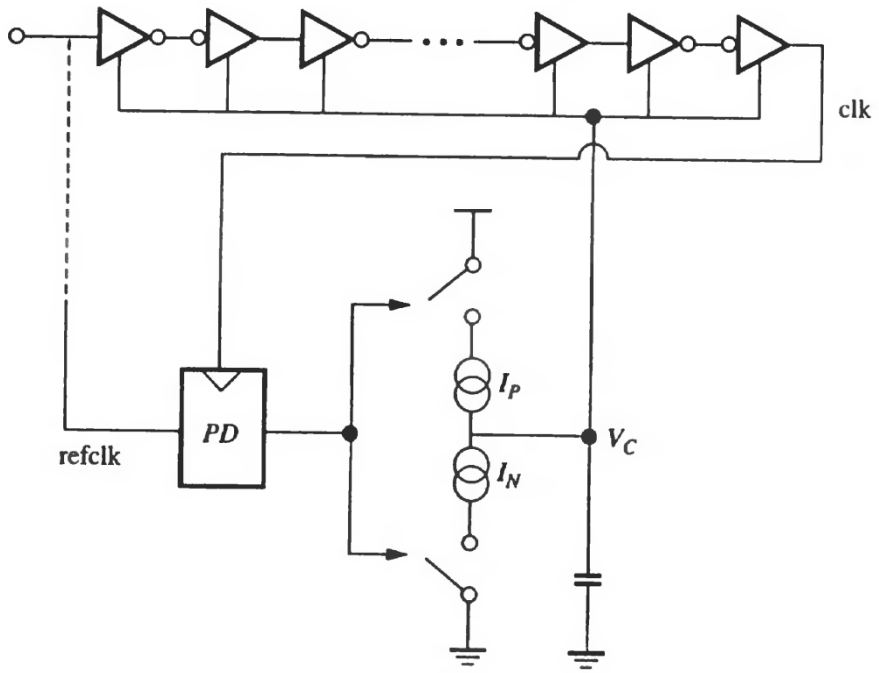


- The control voltage adjusts the amount of current delivered to the inverter to charge and discharge the next stage
- As the current varies, the delay through the inverter varies as well.



PLL/DLL Architecture :

- The PLL can be modified to implement a DLL by a substitution of the VCO with a voltage-controlled delay line (VCDL).
- The circuit utilizes the control signal to vary the delay of each inverter.
- DLL is more stable and much easier to design.
- Widely used in clock and data recovery.



PLL vs. DLL

- When it comes to choosing between a PLL or a DLL for a particular application, the differences in the architectures must be understood.

- The oscillator used in the PLL inherently introduces instability and an accumulation of phase error. This in turn degrades the performance of the PLL when attempting to compensate for the delay of the clock distribution network.

- Conversely, the unconditionally stable DLL architecture does not accumulate phase error. For this reason, for delay compensation and clock conditioning, DLL architecture should be used. On the other hand, the PLL typically has an advantage when it comes to frequency synthesis (frequency multiplication/division).

Low Power Design Techniques

- **Two major types of techniques to lower the dissipated power:**
  - Circuit-oriented techniques
  - Fabrication-oriented techniques

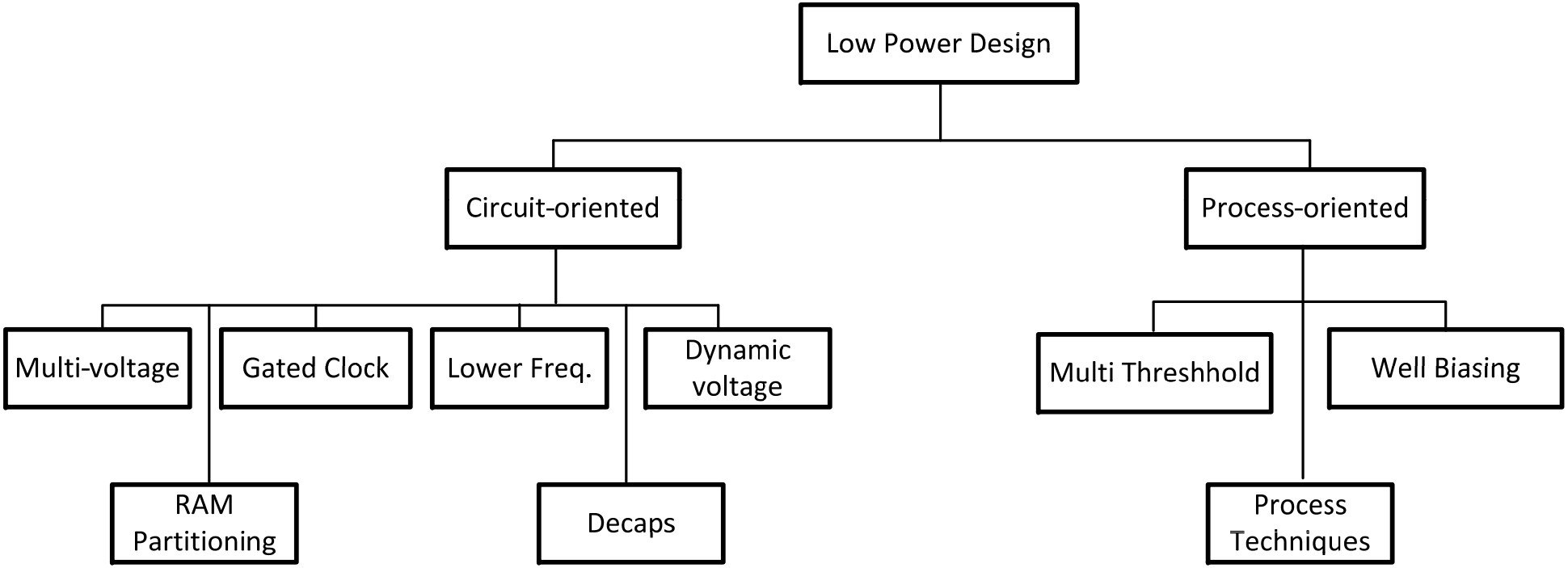
- **Circuit-oriented techniques:**
  - Multi-voltage Design
  - Gated Clock
  - Lower Frequency
  - Utilizing Decaps
  - Dynamic Voltage Scaling
  - RAM Partitioning

Low Power Design Techniques

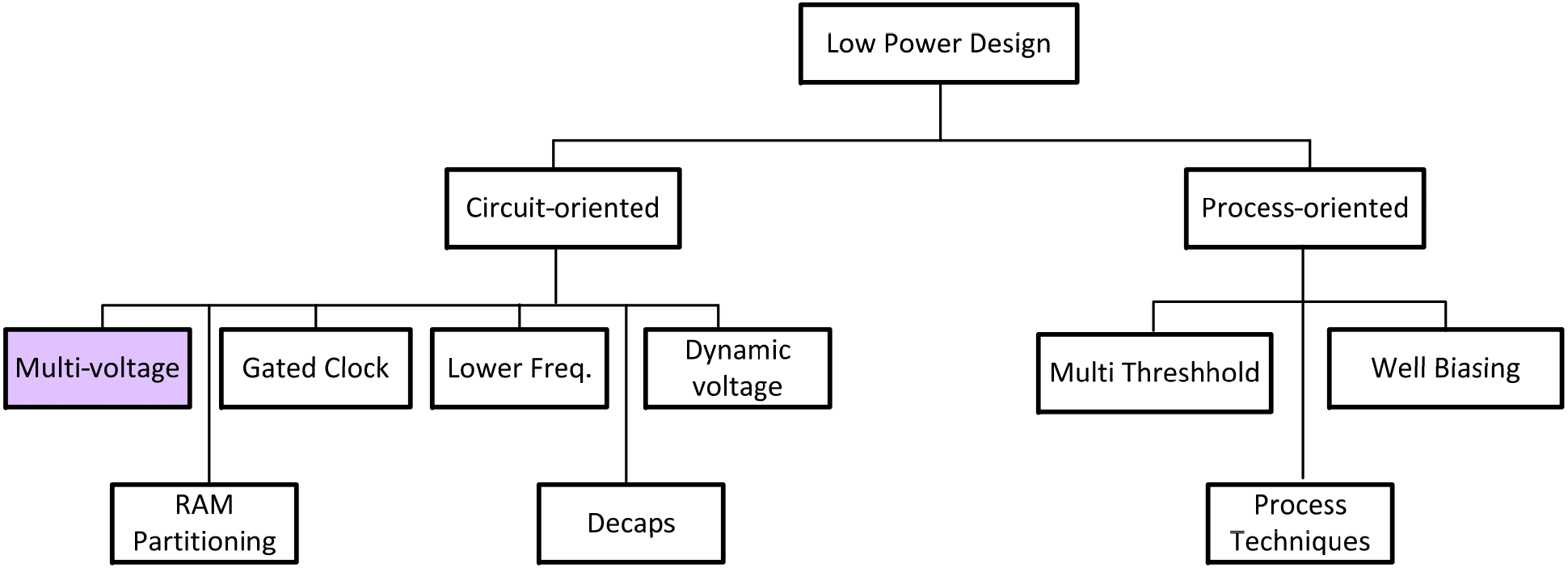
- **Two major types of techniques to lower the dissipated power:**
  - Circuit-oriented techniques
  - Fabrication-oriented techniques

- **Process-oriented techniques:**
  - Multi-threshold Design
  - Well Biasing
  - Process Techniques

Low Power Design Techniques



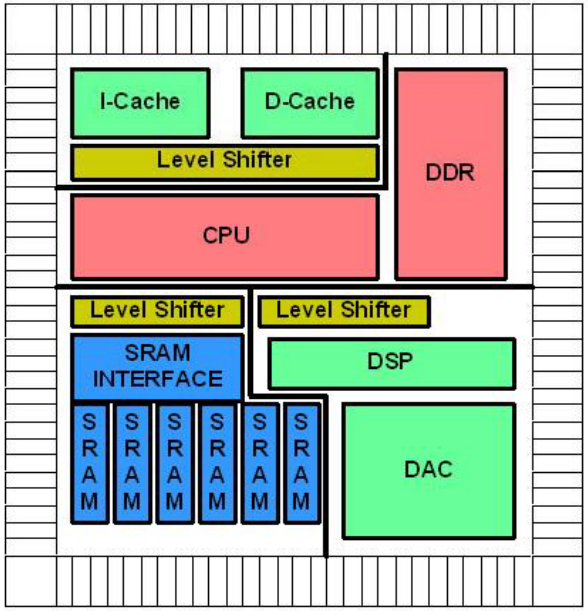
Low Power Design: Multi-Voltage Design



Low Power Design: Multi-Voltage Design

- یکی از روشهای موثر در کاهش توان مصرفی این است که چیپ را به قسمتهای مختلف (Island) یا حوزه-های ولتاژی (Voltage Domains) تقسیم-بندی کنیم که هر یک از این قسمتها دارای ولتاژهای متفاوتی هستند. در این روش از سلولهای کم ولتاژ (Low-voltage) برای کاهش فضای بحرانی طرح، از سلولهای با ولتاژ اسمی (Nominal voltage) برای مناطق بحرانی و از سلولهای با ولتاژ بالا (High voltage) برای مناطق بسیار بحرانی استفاده می-شود

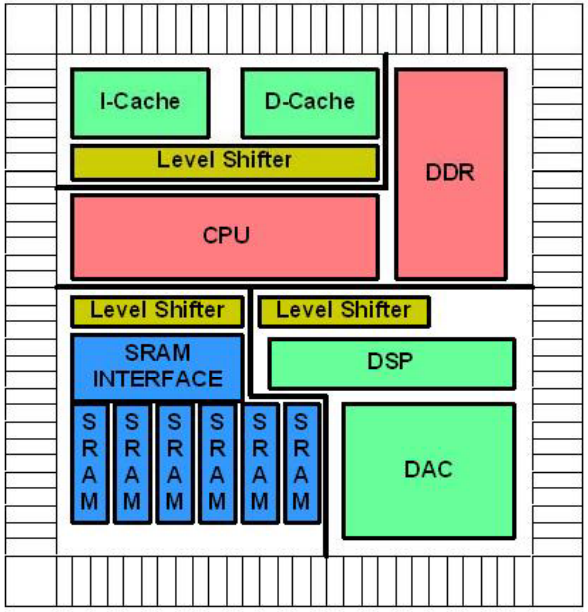
Multi-Voltage Design Example



Low Power Design: Multi-Voltage Design

- جزیره-های ولتاژی زمانیکه استفاده نمی-شوند می-توانند بطور کامل خاموش باشند .مناطق با ولتاز بالا که جزیره-های توان (Power Islands) نامیده می-شوند باید حدالمقدور کمتر در طرح استفاده شوند. Level Shifterها و سلولهای ایزولاسیون (Clamps) می توانند برای تولید سیگنالهایی با ولتاژ پایین تا ولتاژ بالا و بر عکس استفاده شوند. این عملیات نباید بر روی نتهای Global که چندین جزیره ولتاژی را پیمایش می کنند انجام شود

Multi-Voltage Design Example

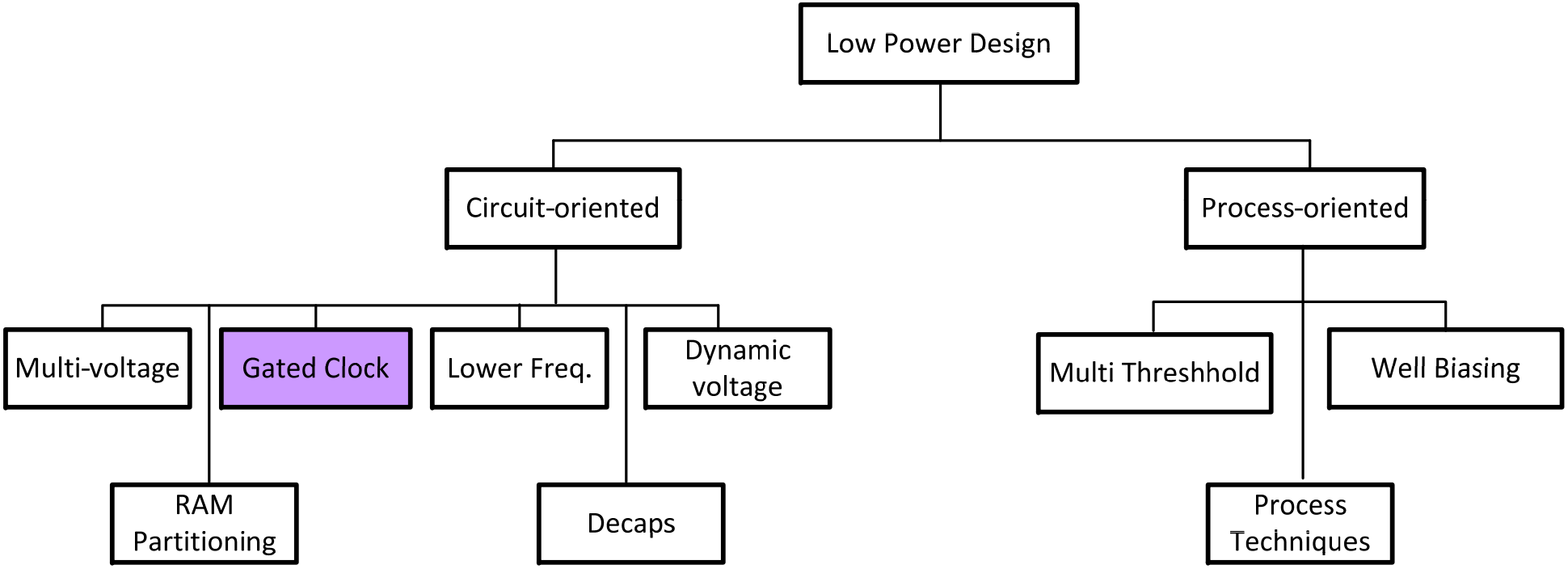


Low Power Design: Multi-Voltage Design

- استفاده از طراحی چند ولتاژی پیامدهایی را در بر دارد .

  - طراحی شبکه توان پیچیده می شود.
  - Level Shifter های ولتاژ و سلولهای ایزولاسیون (Clamps) باید بصورت دستی به طرح اضافه شوند.
  - Level Shifter ها فضای زیادی را اشغال می کنند.
  - به چندین مرحله آنالیز با حفظ همبستگی و دقت حوزه-های توان نیاز است .

Low Power Design: Clock Control

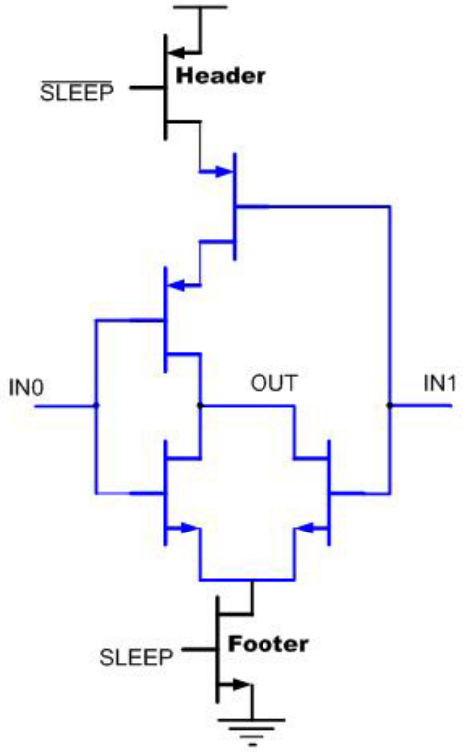


Low Power Design: Clock Control

- کنترل فرکانس کلاک و گیت کردن آن یکی دیگر از روشهای کاهش توان مصرفی است. توزیع کلاک می تواند ۲۰ تا ۳۰ درصد توان کل چیپ را مصرف کند.
- شما می توانید از کلاکهایی با فرکانس پایین که توان کمتری مصرف می کنند برای کنترل سوئیچینگ سیگنالهایی در طرح که به سرعت بالا نیاز ندارند، استفاده کنید.
- با گیت کردن کلاک در تمام بلوکهای طرح که از یک کلاک استفاده می کنند، می توان از روشن شدن غیر ضروری مدار در هنگام سوئیچینگ کلاک جلوگیری کنید. به این ترتیب می توان توان دینامیک را کاهش داد.
- دو برابر یا سه برابر کردن عرض سیمهای کلاک برای کاهش مقاومت Clock Slew باعث کاهش جریان Crossbar می شود. این افزایش فضا باعث کاهش خازن Couple بر روی نت کلاک می شود.
- در نهایت شما می توانید در طراحی چند ولتاژی، در مناطقی که ولتاژ پایین دارند از کلاک کندتر استفاده کنید.

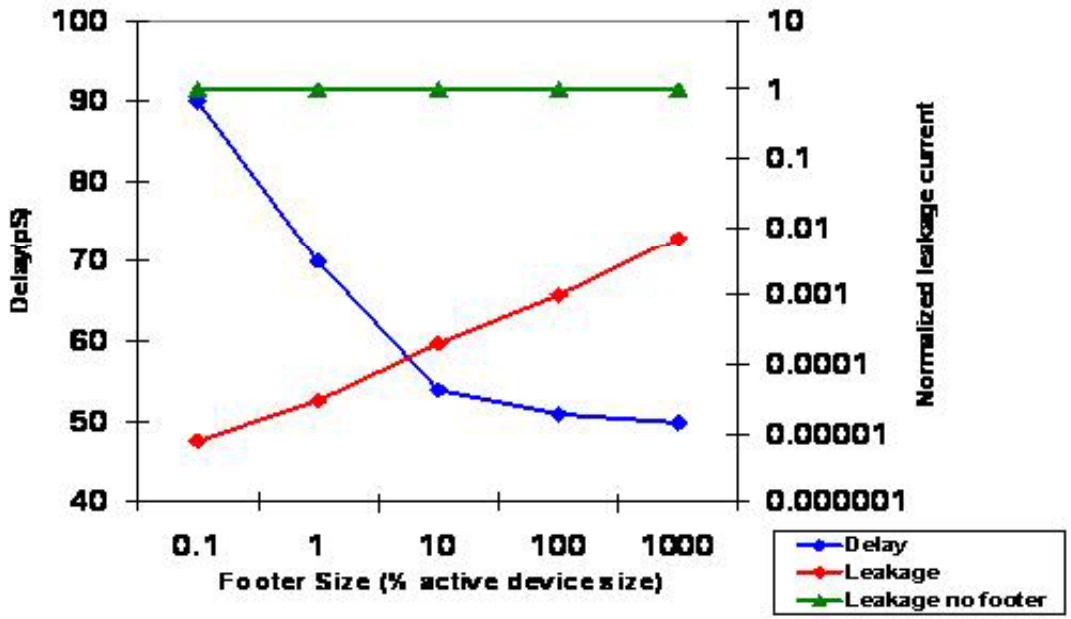
Low Power Design: Clock Control/ Sleep Mode

- شما می توانید بخشهایی از طرح را در صورتی که به آنها نیازی نباشد خاموش نگه دارید. همانطور که در شکل زیر نشان داده شده است، ترانزیستورهای Header وFooter با سیگنال SLEEP کنترل می شوند .

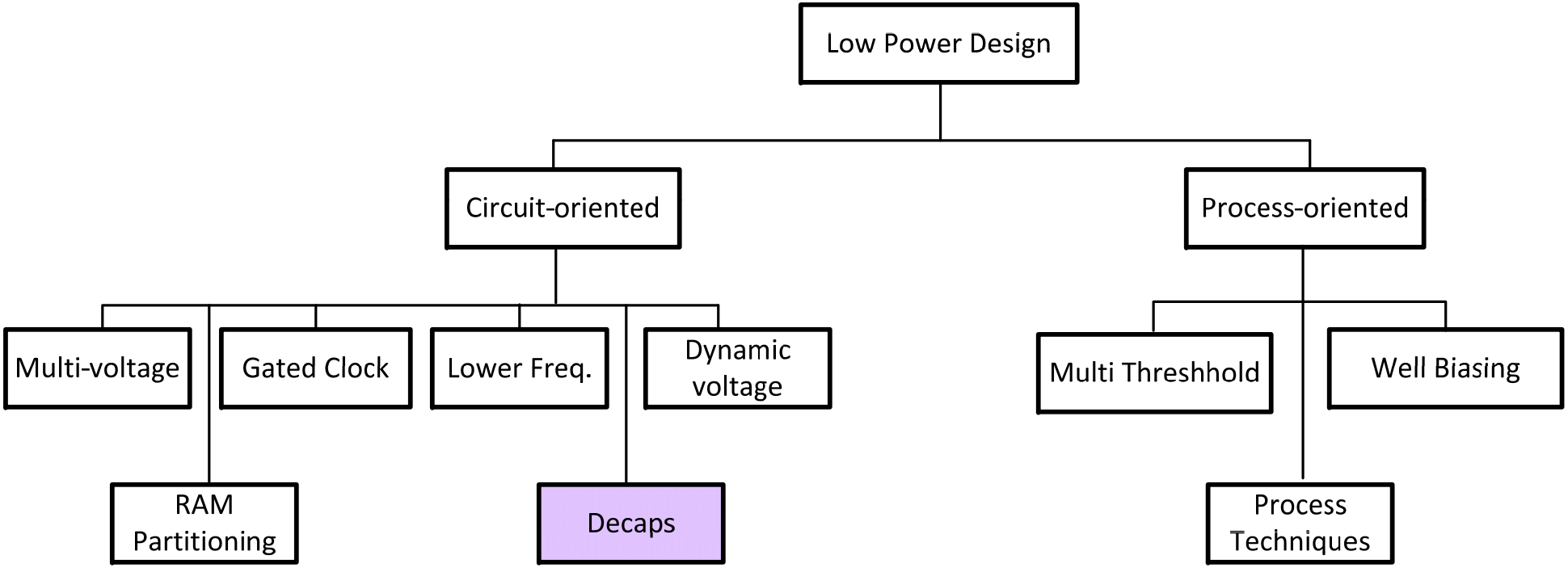


Low Power Design: Clock Control/ Sleep Mode

- یک Tradeoff بین سایز Header و Footer و جریان نشتی وجود دارد. افزایش مساحت، جریان نشتی را کاهش می دهد



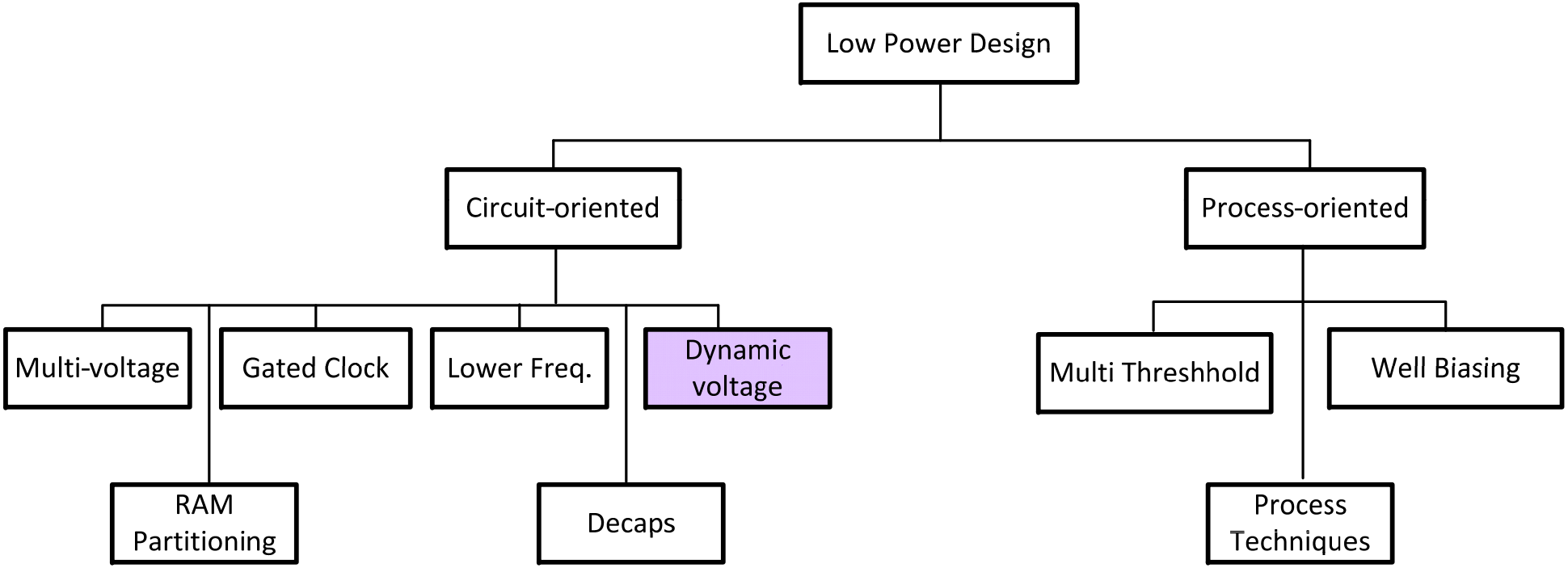
Low Power Design: Decap Insertion



Low Power Design: Decap Insertion

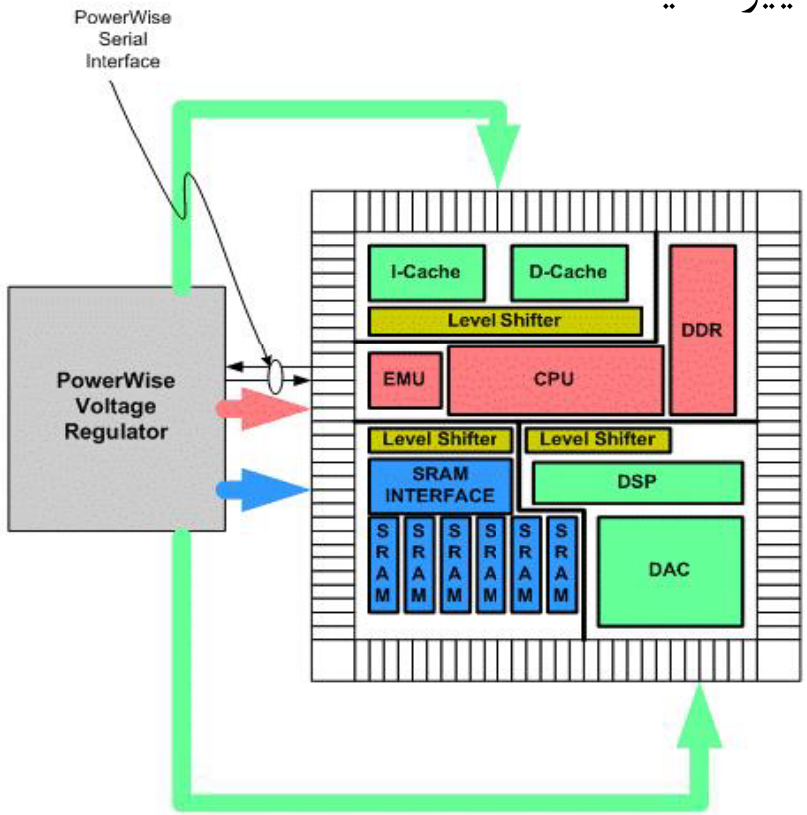
- قبل از پروسه 90nm ، در طراحی ها بطور معمول تعداد قابل توجهی خازن Decoupling بین ریلهای Power و Ground اضافه می شد تا به هموار شدن ناپایداریها کمک کند.
- به دلیل افزایش خازن نشتی گیت در پروسه 90nm هر خازن Decoupling نشتی کلی طرح را افزایش می دهد که به تبع آن توان مصرفی افزایش می یابد. لذا برای کاهش توان مصرفی، لازم است که اندازه بهینه و مکان خازنهای Decoupling را برای مینیمم کردن تعداد خازنهای اضافه شده محاسبه کنیم.
- آنالیز ریل توان دینامیک، اطلاعات لازم برای فهمیدن اینکه چگونه می توان تعداد موثر خازنها را دانست، در اختیار ما قرار میدهد. بنابراین می توان توان مصرفی را به حداقل ممکن رساند.

Low Power Design: Dynamic Voltage Scaling

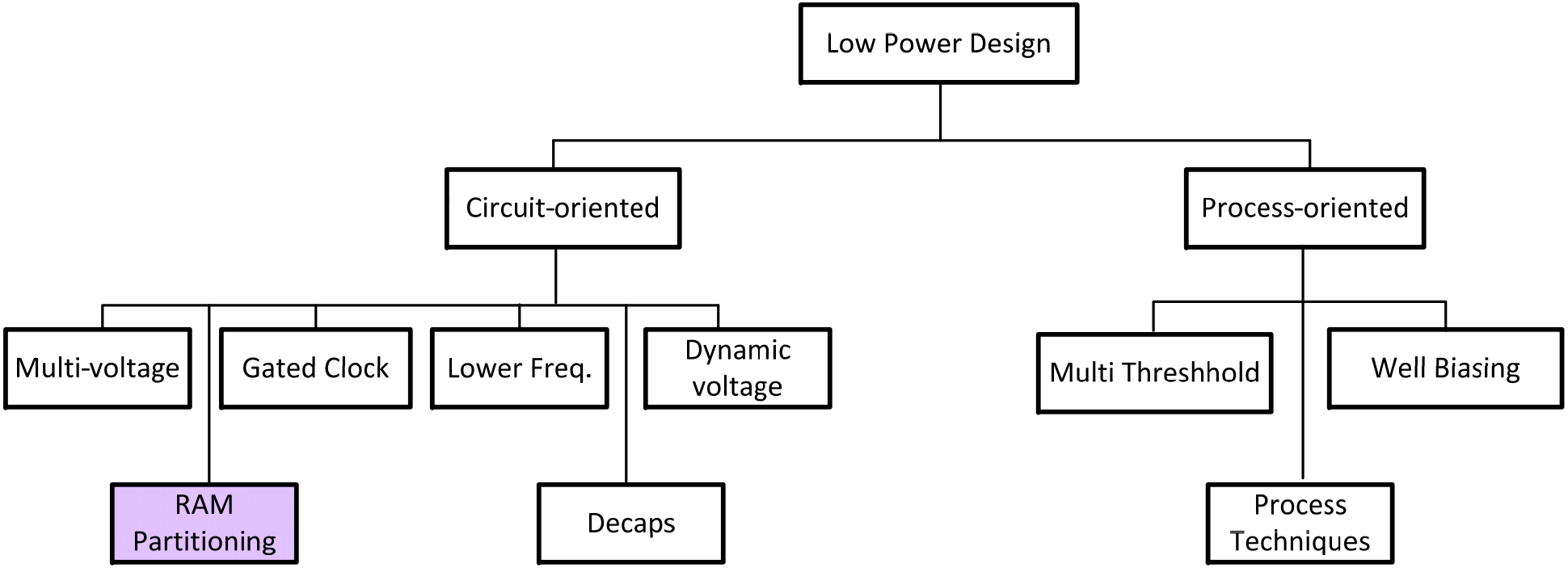


Low Power Design: Dynamic Voltage Scaling

- استفاده از یک واسط سریال برای کنترل ولتاژ رگلاتورها (Power Wise) که به شما این امکان را می دهد که ولتاژ را به حد نیاز کاهش دهید.
- واحد مدیریت انرژی (EMU) بوسیله رگولاتور ولتاژ را کنترل می کند بنابراین شما می توانید سطح ولتاژ را بر اساس نیاز خود تغییر دهید.



Low Power Design: RAM Partitioning

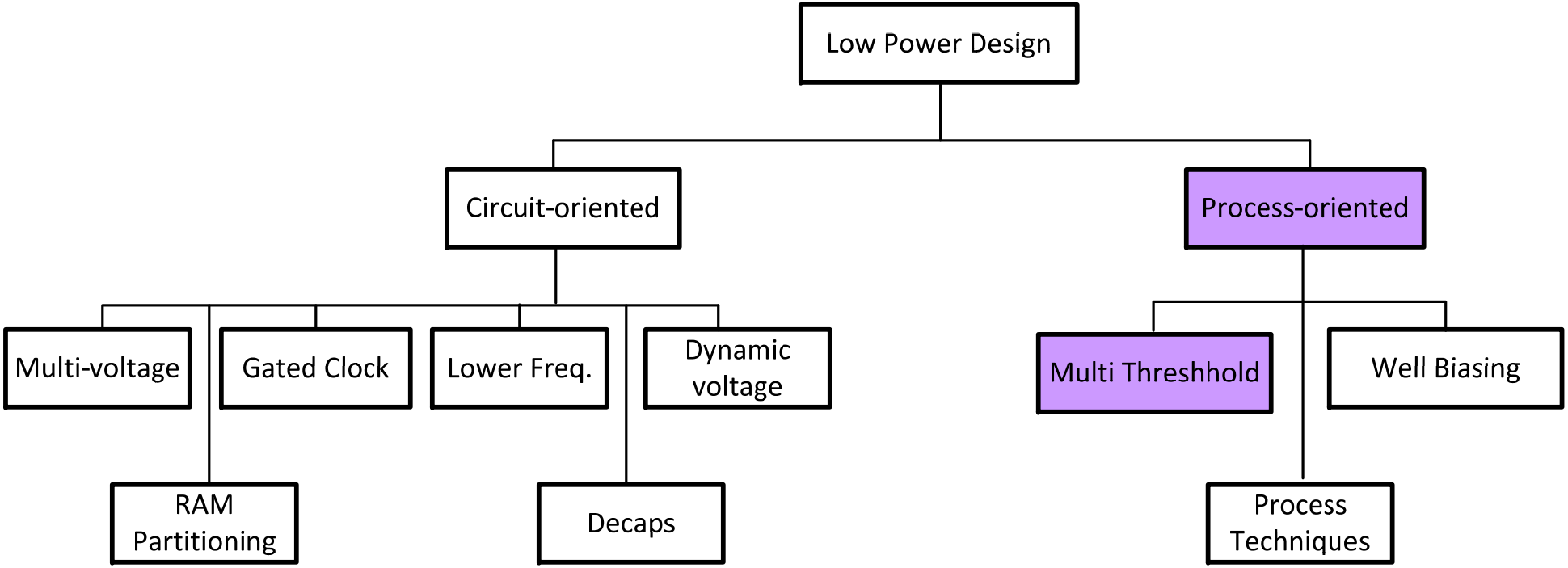


Low Power Design: RAM Partitioning

- بیشترین توان دینامیک در RAMها در زمان Pre-charge و دشارژ بیتهای خطوط حافظه مصرف می شود.

- حافظه هایی که تعداد خطوط کمتری دارند توان دینامیک کمتری دارند.
  - یک 1024k × 32 RAM را می توان به چهار 256 × 32 RAM تقسیم کرد و در نتیجه توان دینامیک را کاهش داد.

Low Power Design: Multi-Threshold



Low Power Design: Multi-Threshold

- یکی دیگر از روشهای کاهش توان مصرفی، استفاده از پروسه CMOS چند آستانه ای (MTCMOS) برای کاهش نشتی است.
- در این راهکار می توان از ابزارهای سنتز فیزیکال که سلولهای با ولتاژ آستانه بالا را که نشتی کم و سرعت کمتری دارد را با سلولهای با آستانه پایین که نشتی بالا و سرعت بالا دارند برای بلوکهایی که سرعت در آنها اهمیت چندانی ندارد، معاوضه کرد.
- سلولهای آستانه پایین در مسیرهای بحرانی و سلولهای آستانه بالا در مسیرهای غیر بحرانی توسط ابزار سنتزکننده جایگذاری می شوند. بسیاری از تولیدکننده های کتابخانه، سه نسخه از هر کتابخانه را می دهند.

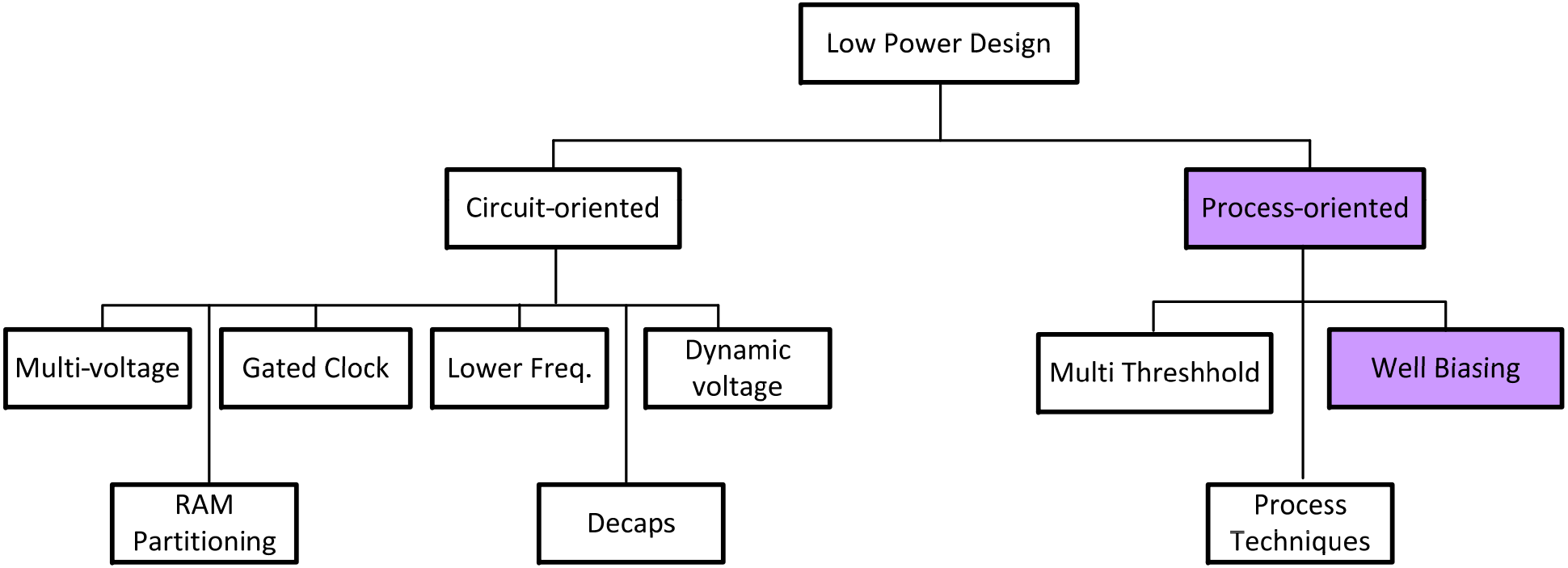
	90 Nanometers			130 Nanometers	
Voltage	LOW	Standard	High	LOW	Standard
Leakage(Static) (pA/μ)	100	10	1.5	10	0.25
$I_{d\text{-}sat}$	755	640	520	590	535

Low Power Design: Multi-Threshold

- طراحی چند آستانه ای پیچیدگی فرایند ساخت را افزایش می دهد زیرا به Mask های بیشتری نیاز دارد.
- ولتاژ آستانه، ولتاژ ورودی است که باعث سوئیچ یک ترانزیستور می شود. اگر شما سلولهایی با ولتاژ آستانه پایین در اختیار دارید، سرعت سوئیچینگ شما افزایش می یابد ولی در عین حال جریان نشتی استاتیک نیز افزایش می یابد .

	90 Nanometers			130 Nanometers	
Voltage	LOW	Standard	High	LOW	Standard
Leakage(Static) (pA/μ)	100	10	1.5	10	0.25
$I_{d\text{-}sat}$	755	640	520	590	535

Low Power Design: Well Biasing



Low Power Design: Well Biasing

- جریان نشتی می تواند ۱۰ تا ۲۰ برابر با تغییر ولتاژ بدنه کاهش یابد.
- افزایش ولتاژ بدنه اثر منفی بر روی I_{ds} (جریان سورس به درین) می گذارد و C_{OX} (جزء اصلی خازن گیت) را افزایش می دهد.
- تغییر ولتاژ Bias می تواند منجر به کاهش نشتی شود بدون اینکه بر روی کارایی تاثیر گذارد. این روش می تواند در مد Sleep مورد استفاده قرار گیرد.
- Biasing یک Substrate از Biasing یک nwell بسیار مشکل تر است.

Low Power Design: Well Biasing

See Voltage storm manual to complete this slide series.