Basic BJT Amplifiers

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In the previous chapter, we described the structure and operation of the bipolar junction transistor, and analyzed and designed the dc response of circuits containing these devices. In this chapter, we emphasize the use of the bipolar transistor in linear amplifier applications. Linear amplifiers imply that, for the most part, we are dealing with analog signals. The magnitude of an analog signal may have any value, within limits, and may vary continuously with respect to time. A linear amplifier then means that the output signal is equal to the input signal multiplied by a constant, where the magnitude of the constant of proportionality is, in general, greater than unity.

PREVIEW

In this chapter, we will:

- Understand the concept of an analog signal and the principle of a linear amplifier.
- Investigate the process by which a transistor circuit can amplify a small, time-varying input signal.
- Discuss the three basic transistor amplifier configurations.
- Analyze the common-emitter amplifier.
- Understand the concept of the ac load line and determine the maximum symmetrical swing of the output signal.
- Analyze the emitter-follower amplifier.
- Analyze the common-base amplifier.
- Compare the general characteristics of the three basic amplifier configurations.
- Analyze multitransistor or multistage amplifiers.
- Understand the concept of signal power gain in an amplifier circuit.
- Incorporate the bipolar transistor in a design application of a multistage transistor amplifier circuit configuration to provide a specified output signal power.

6.1 ANALOG SIGNALS AND LINEAR AMPLIFIERS

Objective: • Understand the concept of an analog signal and the principle of a linear amplifier.

In this chapter, we will be considering **signals, analog** circuits, and **amplifiers.** A signal contains some type of information. For example, sound waves produced by a speaking human contain the information the person is conveying to another person. Our physical senses, such as hearing, vision, and touch, are naturally analog. Analog signals can represent parameters such as temperature, pressure, and wind velocity. Here, we are interested in electrical signals, such as the output signal from a compact disc, a signal from a microphone, or a signal from a heart rate monitor. The electrical signals are in the form of time-varying currents and voltages.

The magnitude of an **analog signal** can take on any value within limits and may vary continuously with time. Electronic circuits that process analog signals are called **analog circuits.** One example of an analog circuit is a linear amplifier. A **linear amplifier** magnifies an input signal and produces an output signal whose magnitude is larger and directly proportional to the input signal.

In many modern day systems, signals are processed, transmitted, or received in digital form. In order to produce an analog signal, these digital signals need to be processed through a digital-to-analog (D/A) converter. D/A and A/D (analog-to-digital) converters are considered in Chapter 16. In this chapter, we will assume that we already have an analog signal that needs to be amplified.

Time-varying signals from a particular source very often need to be amplified before the signal is capable of being "useful." For example, Figure 6.1 shows a signal source that is the output of a compact disc system. We assume the signal source is the output of the D/A converter and this signal consists of a small time-varying voltage and current, which means the signal power is relatively small. The power required to drive the speakers is larger than the output signal from the compact disc, so the compact disc signal must be amplified before it is capable of driving the speakers in order that sound can be heard. Other examples of signals that must be amplified before they are capable of driving loads include the output of a microphone, voice signals received on earth from an orbiting manned shuttle, video signals from an orbiting weather satellite, and the output of an EKG.

Also shown in Figure 6.1 is a dc voltage source connected to the amplifier. The amplifier contains transistors that must be biased in the forward-active region so that the transistors can act as amplifying devices. We want the output signal to be linearly proportional to the input signal so that the output of the speakers is an exact (as much

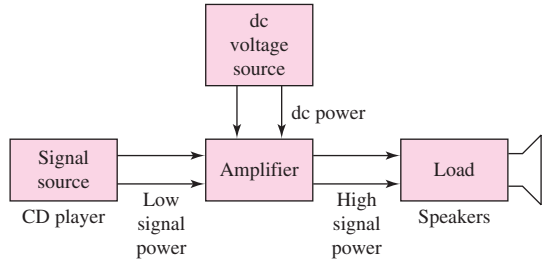


Figure 6.1 Block diagram of a compact disc player system

as possible) reproduction of the signal generated from the compact disc. Therefore, we want the amplifier to be a **linear** amplifier.

Figure 6.1 suggests that there are two types of analyses of the amplifier that we must consider. The first is a dc analysis because of the applied dc voltage source, and the second is a time-varying or ac analysis because of the time-varying signal source. A linear amplifier means that the superposition principle applies. The principle of superposition states: *The response of a linear circuit excited by multiple independent input signals is the sum of the responses of the circuit to each of the input signals alone.*

For the linear amplifier, then, the dc analysis can be performed with the ac source set to zero. This analysis, called a *large signal analysis,* establishes the *Q*-point of the transistors in the amplifier. This analysis and design was the primary objective of the previous chapter. The ac analysis, called a *small-signal analysis,* can be performed with the dc source set to zero. The total response of the amplifier circuit is the sum of the two individual responses.

6.2 THE BIPOLAR LINEAR AMPLIFIER

Objective: • Investigate the process by which a single-transistor circuit can amplify a small, time-varying input signal and develop the small-signal models of the transistor that are used in the analysis of linear amplifiers.

The transistor is the heart of an amplifier. In this chapter, we will consider bipolar transistor amplifiers. Bipolar transistors have traditionally been used in linear amplifier circuits because of their relatively high gain.

We begin our discussion by considering the same bipolar circuit that was discussed in the last chapter. Figure 6.2(a) shows the circuit where the input signal v_I

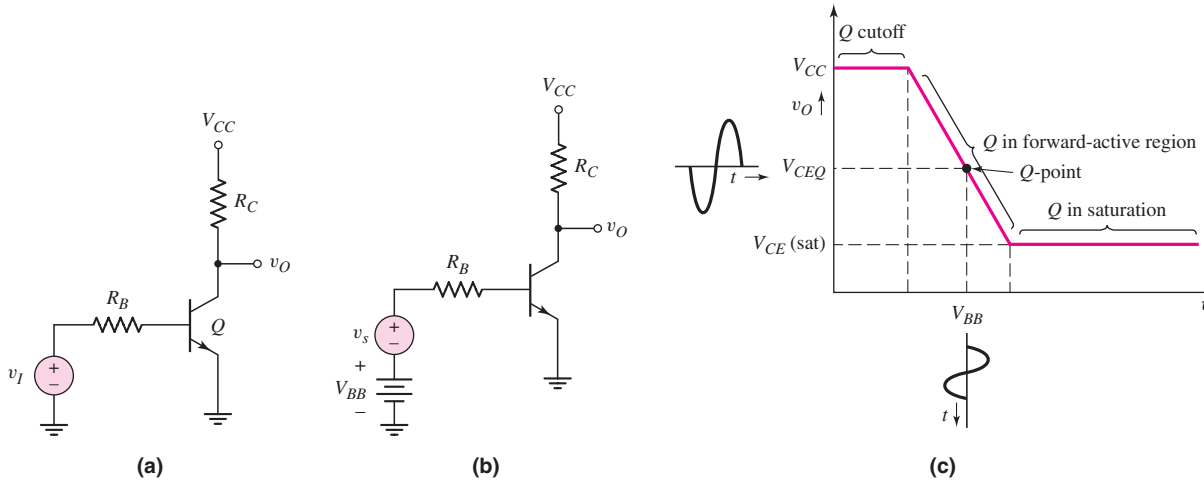


Figure 6.2 (a) Bipolar transistor inverter circuit, (b) inverter circuit showing both dc bias and ac signal sources in the base circuit, and (c) transistor inverter voltage transfer characteristics showing desired *Q*-point

contains both a dc and an ac signal. Figure 6.2(b) shows the same circuit where V_{BB} is a dc voltage to bias the transistor at a particular Q-point and v_s is the ac signal that is to be amplified. Figure 6.2(c) shows the voltage transfer characteristics that were developed in Chapter 5. To use the circuit as an amplifier, the transistor needs to be biased with a dc voltage at a quiescent point (Q-point), as shown in the figure, such that the transistor is biased in the forward-active region. This dc analysis or design of the circuit was the focus of our attention in Chapter 5. If a time-varying (e.g., sinusoidal) signal is superimposed on the dc input voltage, V_{BB}, the output voltage will change along the transfer curve producing a time-varying output voltage. If the time-varying output voltage is directly proportional to and larger than the time-varying input voltage, then the circuit is a linear amplifier. From this figure, we see that if the transistor is not biased in the active region (biased either in cutoff or saturation), the output voltage does not change with a change in the input voltage. Thus, we no longer have an amplifier.

In this chapter, we are interested in the ac analysis and design of bipolar transistor amplifiers, which means that we must determine the relationships between the time-varying output and input signals. We will initially consider a graphical technique that can provide an intuitive insight into the basic operation of the circuit. We will then develop a small-signal equivalent circuit that will be used in the mathematical analysis of the ac signals. In general, we will be considering a steady-state, sinusoidal analysis of circuits. We will assume that any time-varying signal can be written as a sum of sinusoidal signals of different frequencies and amplitudes (Fourier series), so that a sinusoidal analysis is appropriate.

We will be dealing with time-varying as well as dc currents and voltages in this chapter. Table 6.1 gives a summary of notation that will be used. This notation was discussed in the Prologue, but is repeated here for convenience. A lowercase letter with an uppercase subscript, such as i_B or v_{BE}, indicates *total instantaneous values*.

Table 6.1 Summary of notation

Variable	Meaning
i_B, v_{BE}	Total instantaneous values
I_B, V_{BE}	DC values
i_b, v_{be}	Instantaneous ac values
I_b, V_{be}	Phasor values

An uppercase letter with an uppercase subscript, such as I_B or V_{BE}, indicates *dc quantities*. A lowercase letter with a lowercase subscript, such as i_b or v_{be}, indicates instantaneous values of *ac signals*. Finally, an upper-case letter with a lowercase subscript, such as I_b or V_{be}, indicates *phasor quantities*. The phasor notation, which was reviewed in the Prologue becomes especially important in Chapter 7 during the discussion of frequency response. However, the phasor notation will be generally used in this chapter in order to be consistent with the overall ac analysis.

6.2.1 Graphical Analysis and ac Equivalent Circuit

Figure 6.3 shows the same basic bipolar inverter circuit that has been discussed, but now includes a sinusoidal signal source in series with the dc source as was shown in Figure 6.2(b).

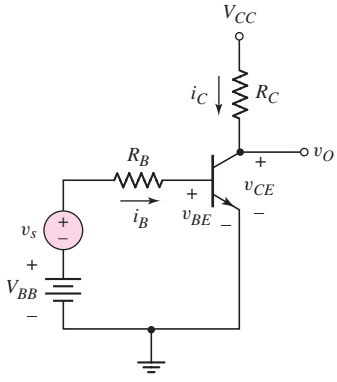


Figure 6.3 A common-emitter circuit with a time-varying signal source in series with the base dc source

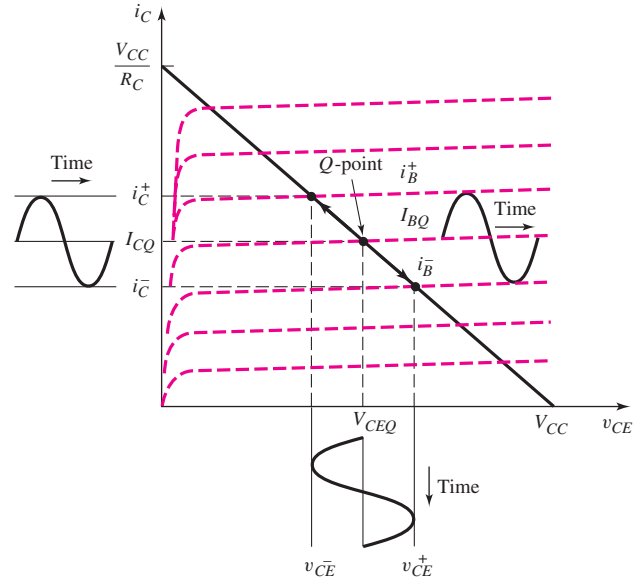


Figure 6.4 Common-emitter transistor characteristics, dc load line, and sinusoidal variation in base current, collector current, and collector–emitter voltage

Figure 6.4 shows the transistor characteristics, the dc load line, and the Q-point. The sinusoidal signal source, v_s, will produce a time-varying or ac base current superimposed on the quiescent base current as shown in the figure. The time-varying base current will induce an ac collector current superimposed on the quiescent collector current. The ac collector current then produces a time-varying voltage across R_C, which induces an ac collector–emitter voltage as shown in the figure. The ac collector–emitter voltage, or output voltage, in general, will be larger than the sinusoidal input signal, so that the circuit has produced signal amplification—that is, the circuit is an amplifier.

We need to develop a mathematical method or model for determining the relationships between the sinusoidal variations in currents and voltages in the circuit. As already mentioned, a linear amplifier implies that superposition applies so that the dc and ac analyses can be performed separately. To obtain a linear amplifier, the time-varying or ac currents and voltages must be small enough to ensure a linear relation between the ac signals. To meet this objective, the time-varying signals are assumed to be *small signals,* which means that the amplitudes of the ac signals are small enough to yield linear relations. The concept of "small enough," or small signal, will be discussed further as we develop the small-signal equivalent circuits.

A time-varying signal source, v_s, in the base of the circuit in Figure 6.3 generates a time-varying component of base current, which implies there is also a time-varying component of base–emitter voltage. Figure 6.5 shows the exponential relationship between base-current and base–emitter voltage. If the magnitudes of the time-varying signals that are superimposed on the dc quiescent point are small, then we can develop a linear relationship between the ac base–emitter voltage and ac base current. This relationship corresponds to the slope of the curve at the Q-point.

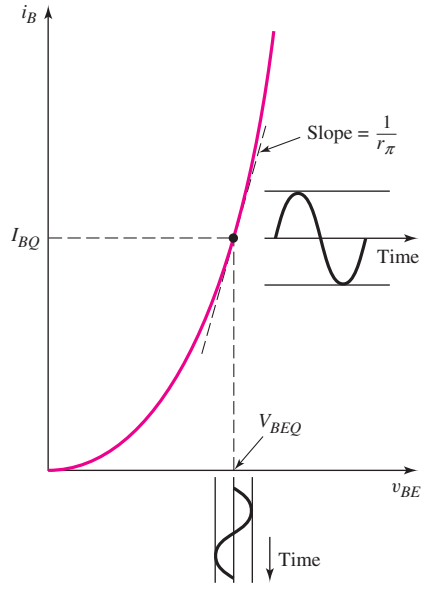


Figure 6.5 Base current versus base-emitter voltage characteristic with superimposed sinusoidal signals. Slope at the Q-point is inversely proportional to r_π, a small-signal parameter.

Using Figure 6.5, we can now determine one quantitative definition of small signal. From the discussion in Chapter 5, in particular, Equation (5.6), the relation between base–emitter voltage and base current can be written as

$$i_B = \frac{I_S}{\beta} \cdot \exp\left(\frac{v_{BE}}{V_T}\right) \tag{6.1}$$

If v_{BE} is composed of a dc term with a sinusoidal component superimposed, i.e., $v_{BE} = V_{BEQ} + v_{be}$, then

$$i_B = \frac{I_S}{\beta} \cdot \exp\left(\frac{V_{BEQ} + v_{be}}{V_T}\right) = \frac{I_S}{\beta} \cdot \exp\left(\frac{V_{BEQ}}{V_T}\right) \cdot \exp\left(\frac{v_{be}}{V_T}\right) \tag{6.2}$$

where V_{BEQ} is normally referred to as the base–emitter turn-on voltage, $V_{BE}(\text{on})$. The term $[I_S/\beta] \cdot \exp(V_{BEQ}/V_T)$ is the quiescent base current, so we can write

$$i_B = I_{BQ} \cdot \exp\left(\frac{v_{be}}{V_T}\right) \tag{6.3}$$

The base current, given in this form, is not linear and cannot be written as an ac current superimposed on a dc quiescent value. However, if $v_{be} \ll V_T$, then we can expand the exponential term in a Taylor series, keeping only the **linear term.** This approximation is what is meant by **small signal.** We then have

$$i_B \cong I_{BQ}\left(1 + \frac{v_{be}}{V_T}\right) = I_{BQ} + \frac{I_{BQ}}{V_T} \cdot v_{be} = I_{BQ} + i_b \tag{6.4(a)}$$

where i_b is the time-varying (sinusoidal) base current given by

$$i_b = \left(\frac{I_{BQ}}{V_T}\right) v_{be} \tag{6.4(b)}$$

The sinusoidal base current, i_b, is linearly related to the sinusoidal base–emitter voltage, v_{be}. In this case, the term small-signal refers to the condition in which v_{be} is sufficiently small for the linear relationships between i_b and v_{be} given by Equation (6.4(b)) to be valid. As a general rule, if v_{be} is less than l0 mV, then the exponential relation given by Equation (6.3) and its linear expansion in Equation (6.4(a)) agree within approximately 10 percent. Ensuring that $v_{be} < 10$ mV is another useful rule of thumb in the design of linear bipolar transistor amplifiers.

If the v_{be} signal is assumed to be sinusoidal, but if its magnitude becomes too large, then the output signal will no longer be a pure sinusoidal voltage but will become distorted and contain harmonics (see box "Harmonic Distortion").

Harmonic Distortion

If an input sinusoidal signal becomes too large, the output signal may no longer be a pure sinusoidal signal because of nonlinear effects. A nonsinusoidal output signal may be expanded into a Fourier series and written in the form

$$\underset{\text{dc}}{v_O(t) = V_O} + \underset{\substack{\text{desired}\\ \text{linear output}}}{V_1 \sin(\omega t + \phi_1)} + \underset{\substack{\text{2nd harmonic}\\ \text{distortion}}}{V_2 \sin(2\omega t + \phi_2)} + \underset{\substack{\text{3rd harmonic}\\ \text{distortion}}}{V_3 \sin(3\omega t + \phi_3)} + \cdots \tag{6.5}$$

The signal at the frequency ω is the desired linear output signal for a sinusoidal input signal at the same frequency.

The time-varying input base-emitter voltage is contained in the exponential term given in Equation (6.3). Expanding the exponential function into a Taylor series, we find

$$e^x = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \cdots \tag{6.6}$$

where, from Equation (6.3), we have $x = v_{be}/V_T$. If we assume the input signal is a sinusoidal function, then we can write

$$x = \frac{v_{be}}{V_T} = \frac{V_\pi}{V_T} \sin \omega t \tag{6.7}$$

The exponential function can then be written as

$$e^x = 1 + \frac{V_\pi}{V_T} \sin \omega t + \frac{1}{2} \cdot \left(\frac{V_\pi}{V_T}\right)^2 \sin^2 \omega t + \frac{1}{6} \cdot \left(\frac{V_\pi}{V_T}\right)^3 \sin^3 \omega t + \cdots \tag{6.8}$$

From trigonometric identities, we can write

$$\sin^2 \omega t = \frac{1}{2}[1 - \cos(2\omega t)] = \frac{1}{2}[1 - \sin(2\omega t + 90^\circ)] \tag{6.9a}$$

and

$$\sin^3 \omega t = \frac{1}{4}[3 \sin \omega t - \sin(3\omega t)] \tag{6.9b}$$

Substituting Equations (6.9a) and (6.9b) into Equation (6.8), we obtain

$$e^x = \left[1 + \frac{1}{4}\left(\frac{V_\pi}{V_T}\right)^2\right] + \frac{V_\pi}{V_T}\left[1 + \frac{1}{8}\left(\frac{V_\pi}{V_T}\right)^2\right]\sin\omega t$$
$$-\frac{1}{4}\left(\frac{V_\pi}{V_T}\right)^2 \sin(2\omega t + 90^\circ) - \frac{1}{24}\left(\frac{V_\pi}{V_T}\right)^3 \sin(3\omega t) + \cdots \quad \textbf{(6.10)}$$

Comparing Equation (6.10) to Equation (6.8), we find the coefficients as

$$V_O = \left[1 + \frac{1}{4}\left(\frac{V_\pi}{V_T}\right)^2\right] \quad V_1 = \frac{V_\pi}{V_T}\left[1 + \frac{1}{8}\left(\frac{V_\pi}{V_T}\right)^2\right]$$
$$V_2 = -\frac{1}{4}\left(\frac{V_\pi}{V_T}\right)^2 \qquad V_3 = -\frac{1}{24}\left(\frac{V_\pi}{V_T}\right)^3 \quad \textbf{(6.11)}$$

We see that as (V_π / V_T) increases, the second and third harmonic terms become non-zero. In addition, the dc and first harmonic coefficients also become nonlinear. A figure of merit is called the percent total harmonic distortion (THD) and is defined as

$$\text{THD}(\%) = \frac{\sqrt{\sum_2^\infty V_n^2}}{V_1} \times 100\% \quad \textbf{(6.12)}$$

Considering only the second and third harmonic terms, the THD is plotted in Figure 6.6. We see that, for $V_\pi \leq 10$ mV, the THD is less than 10 percent. This total harmonic distortion value may seem excessive, but as we will see later in Chapter 12, distortion can be reduced when feedback circuits are used.

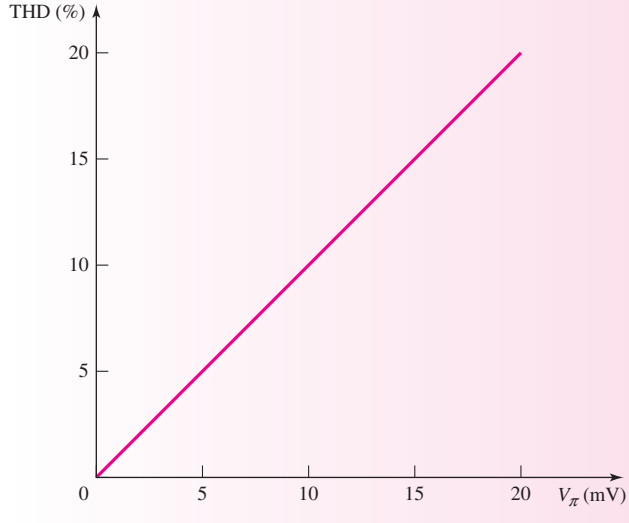


Figure 6.6 Total harmonic distortion of the function e^{v_{BE}/V_T}, where $v_{BE} = V_\pi \sin\omega t$, as a function of V_π

From the concept of small signal, all the time-varying signals shown in Figure 6.4 will be linearly related and are superimposed on dc values. We can write (refer to notation given in Table 6.1)

$$i_B = I_{BQ} + i_b \tag{6.13(a)}$$

$$i_C = I_{CQ} + i_c \tag{6.13(b)}$$

$$v_{CE} = V_{CEQ} + v_{ce} \tag{6.13(c)}$$

and

$$v_{BE} = V_{BEQ} + v_{be} \tag{6.13(d)}$$

If the signal source, v_s, is zero, then the base–emitter and collector–emitter loop equations are

$$V_{BB} = I_{BQ}R_B + V_{BEQ} \tag{6.14(a)}$$

and

$$V_{CC} = I_{CQ}R_C + V_{CEQ} \tag{6.14(b)}$$

Taking into account the time-varying signals, we find the base–emitter loop equation is

$$V_{BB} + v_s = i_B R_B + v_{BE} \tag{6.15(a)}$$

or

$$V_{BB} + v_s = (I_{BQ} + i_b)R_B + (V_{BEQ} + v_{be}) \tag{6.15(b)}$$

Rearranging terms, we find

$$V_{BB} - I_{BQ}R_B - V_{BEQ} = i_b R_B + v_{be} - v_s \tag{6.15(c)}$$

From Equation (6.14(a)), the left side of Equation (6.15(c)) is zero. Equation (6.15 (c)) can then be written as

$$v_s = i_b R_B + v_{be} \tag{6.16}$$

which is the base–emitter loop equation with all dc terms set equal to zero.

Taking into account the time-varying signals, the collector–emitter loop equation is

$$V_{CC} = i_C R_C + v_{CE} = (I_{CQ} + i_c)R_C + (V_{CEQ} + v_{ce}) \tag{6.17(a)}$$

Rearranging terms, we find

$$V_{CC} - I_{CQ}R_C - V_{CEQ} = i_c R_C + v_{ce} \tag{6.17(b)}$$

From Equation (6.14(b)), the left side of Equation (6.17(b)) is zero. Equation (6.17(b)) can be written as

$$i_c R_C + v_{ce} = 0 \tag{6.18}$$

which is the collector–emitter loop equation with all dc terms set equal to zero.

Equations (6.16) and (6.18) relate the ac parameters in the circuit. These equations can be obtained directly by setting all dc currents and voltages equal to zero, so the dc voltage sources become short circuits and any dc current sources would become open circuits. *These results are a direct consequence of applying superposition to a linear circuit.* The resulting BJT circuit, shown in Figure 6.7, is called the *ac*

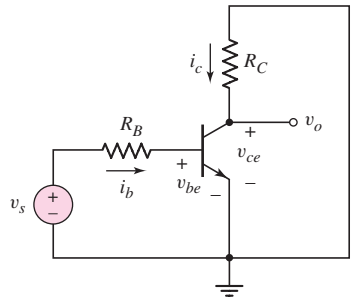


Figure 6.7 The ac equivalent circuit of the common-emitter circuit shown in Figure 6.3. The dc voltage sources have been set equal to zero.

equivalent circuit, and all currents and voltages shown are time-varying signals. We should stress that this circuit is an equivalent circuit. We are implicitly assuming that the transistor is still biased in the forward-active region with the appropriate dc voltages and currents.

Another way of looking at the ac equivalent circuit is as follows. In the circuit in Figure 6.3, the base and collector currents are composed of ac signals superimposed on dc values. These currents flow through the V_{BB} and V_{CC} voltage sources, respectively. Since the voltages across these sources are assumed to remain constant, the sinusoidal currents do not produce any sinusoidal voltages across these elements. Then, since the sinusoidal voltages are zero, the equivalent ac impedances are zero, or short circuits. In other words, the dc voltage sources are ac short circuits in an equivalent ac circuit. We say that the node connecting R_C and V_{CC} is at signal ground.

6.2.2 Small-Signal Hybrid-π Equivalent Circuit of the Bipolar Transistor

We developed the ac equivalent circuit shown in Figure 6.7. We now need to develop a **small-signal equivalent circuit** for the transistor. One such circuit is the **hybrid-π** model, which is closely related to the physics of the transistor. This effect will become more apparent in Chapter 7 when a more detailed hybrid-π model is developed to take into account the frequency response of the transistor.

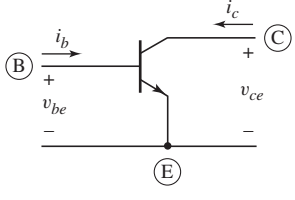


Figure 6.8 The BJT as a small-signal, two-port network

We can treat the bipolar transistor as a two-port network as shown in Figure 6.8. One element of the hybrid-π model has already been described. Figure 6.5 showed the base current versus base–emitter voltage characteristic, with small time-varying signals superimposed at the Q-point. Since the sinusoidal signals are small, we can treat the slope at the Q-point as a constant, which has units of conductance. The inverse of this conductance is the small-signal resistance defined as r_π. We can then relate the small-signal input base current to the small-signal input voltage by

$$v_{be} = i_b r_\pi \tag{6.19}$$

where $1/r_\pi$ is equal to the slope of the i_B–v_{BE} curve, as shown in Figure 6.5. From Equation (6.2), we then find r_π from

$$\frac{1}{r_\pi} = \left.\frac{\partial i_B}{\partial v_{BE}}\right|_{Q\text{-}pt} = \left.\frac{\partial}{\partial v_{BE}}\left[\frac{I_S}{\beta}\cdot\exp\left(\frac{v_{BE}}{V_T}\right)\right]\right|_{Q\text{-}pt} \tag{6.20(a)}$$

or

$$\frac{1}{r_\pi} = \frac{1}{V_T} \cdot \left[\frac{I_S}{\beta} \cdot \exp\left(\frac{v_{BE}}{V_T}\right)\right]\Bigg|_{Q\text{-}pt} = \frac{I_{BQ}}{V_T} \tag{6.20(b)}$$

Then

$$\frac{v_{be}}{i_b} = r_\pi = \frac{V_T}{I_{BQ}} = \frac{\beta V_T}{I_{CQ}} \tag{6.21}$$

The resistance r_π is called the **diffusion resistance** or base–emitter input resistance. We note that r_π is a function of the Q-point parameters.

We can consider the output terminal characteristics of the bipolar transistor. If we initially consider the case in which the output collector current is independent of the collector–emitter voltage, then the collector current is a function only of the base–emitter voltage, as discussed in Chapter 5. We can then write

$$\Delta i_C = \frac{\partial i_C}{\partial v_{BE}}\Bigg|_{Q\text{-}pt} \cdot \Delta v_{BE} \tag{6.22(a)}$$

or

$$i_c = \frac{\partial i_C}{\partial v_{BE}}\Bigg|_{Q\text{-}pt} \cdot v_{be} \tag{6.22(b)}$$

From Chapter 5, in particular Equation (5.2), we had written

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right) \tag{6.23}$$

Then

$$\frac{\partial i_C}{\partial v_{BE}}\Bigg|_{Q\text{-}pt} = \frac{1}{V_T} \cdot I_S \exp\left(\frac{v_{BE}}{V_T}\right)\Bigg|_{Q\text{-}pt} = \frac{I_{CQ}}{V_T} \tag{6.24}$$

The term $I_S \exp(v_{BE}/V_T)$ evaluated at the Q-point is just the quiescent collector current. The term I_{CQ}/V_T is a conductance. Since this conductance relates a current in the collector to a voltage in the B–E circuit, the parameter is called a **transconductance** and is written

$$g_m = \frac{I_{CQ}}{V_T} \tag{6.25}$$

The small-signal transconductance is also a function of the Q-point parameters and is directly proportional to the dc bias current. The variation of transconductance with quiescent collector current will prove to be useful in amplifier design.

Using these new parameters, we can develop a simplified small-signal hybrid-π equivalent circuit for the npn bipolar transistor, as shown in Figure 6.9. The phasor components are given in parentheses. This circuit can be inserted into the ac equivalent circuit previously shown in Figure 6.7.

We can develop a slightly different form for the output of the equivalent circuit. We can relate the small-signal collector current to the small-signal base current as

$$\Delta i_C = \frac{\partial i_C}{\partial i_B}\Bigg|_{Q\text{-}pt} \cdot \Delta i_B \tag{6.26(a)}$$

or

$$i_c = \frac{\partial i_C}{\partial i_B}\Bigg|_{Q\text{-}pt} \cdot i_b \tag{6.26(b)}$$

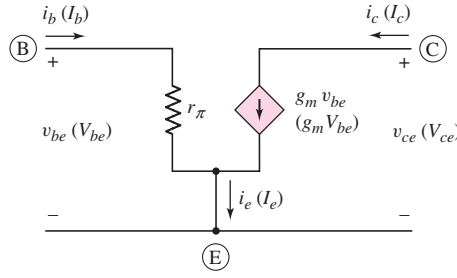


Figure 6.9 A simplified small-signal hybrid-π equivalent circuit for the npn transistor. The ac signal currents and voltages are shown. The phasor signals are shown in parentheses.

where

$$\left.\frac{\partial i_C}{\partial i_B}\right|_{Q\text{-}pt} \equiv \beta \tag{6.26(c)}$$

and is called an incremental or ac common-emitter current gain. We can then write

$$i_c = \beta i_b \tag{6.27}$$

The small-signal equivalent circuit of the bipolar transistor in Figure 6.10 uses this parameter. The parameters in this figure are also given as phasors. This circuit can also be inserted in the ac equivalent circuit given in Figure 6.7. Either equivalent circuit, Figure 6.9 or 6.10, may be used. We will use both circuits in the examples that follow in this chapter.

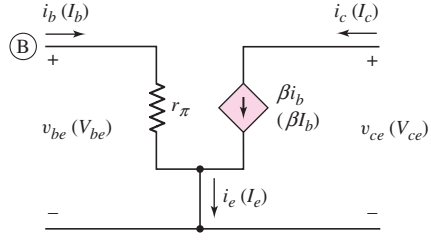


Figure 6.10 BJT small-signal equivalent circuit using the common-emitter current gain. The ac signal currents and voltages are shown. The phasor signals are shown in parentheses.

Common-Emitter Current Gain

The common-emitter current gain defined in Equation (6.26(c)) is actually defined as an ac beta and does not include dc leakage currents. We discussed the common-emitter current gain in Chapter 5. We defined a dc beta as the ratio of a dc collector current to the corresponding dc base current. In this case leakage currents are included. However, we will assume in this text that leakage currents are negligible so that the two definitions of beta are equivalent.

The small-signal hybrid-π parameters r_π and g_m were defined in Equations (6.21) and (6.25). If we multiply r_π and g_m, we find

$$r_\pi g_m = \left(\frac{\beta V_T}{I_{CQ}}\right) \cdot \left(\frac{I_{CQ}}{V_T}\right) = \beta \tag{6.28}$$

In general, we will assume that the common-emitter current gain β is a constant for a given transistor. However, we must keep in mind that β may vary from one device

to another and that β does vary with collector current. This variation with I_C will be specified on data sheets for specific discrete transistors.

Small-Signal Voltage Gain

Continuing our discussion of equivalent circuits, we may now insert the bipolar, equivalent circuit in Figure 6.9, for example, into the ac equivalent circuit in Figure 6.7. The result is shown in Figure 6.11. Note that we are using the phasor notation. When incorporating the small-signal hybrid-π model of the transistor (Figure 6.9) into the ac equivalent circuit (Figure 6.7), it is generally helpful to start with the three terminals of the transistor as shown in Figure 6.11. Then sketch the hybrid-π equivalent circuit between these three terminals. Finally, connect the remaining circuit elements, such as R_B and R_C, to the transistor terminals. As the circuits become more complex, this technique will minimize errors in developing the small-signal equivalent circuit.

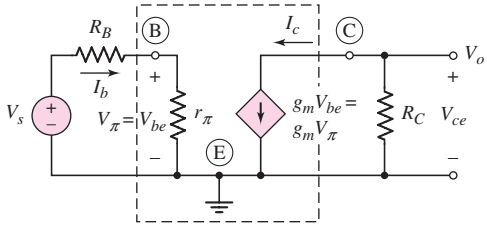


Figure 6.11 The small-signal equivalent circuit of the common-emitter circuit shown in Figure 6.3. The small-signal hybrid-π model of the npn bipolar transistor is shown within the dotted lines.

The **small-signal voltage gain,** $A_v = V_o/V_s$, of the circuit is defined as the ratio of output signal voltage to input signal voltage. We may note a new variable in Figure 6.11. The conventional phasor notation for the small-signal base-emitter voltage is V_π, called the control voltage. The dependent current source is then given by $g_m V_\pi$. The dependent current $g_m V_\pi$ flows through R_C, producing a negative collector–emitter voltage, or

$$V_o = V_{ce} = -(g_m V_\pi) R_C \tag{6.29}$$

and, from the input portion of the circuit, we find

$$V_\pi = \left(\frac{r_\pi}{r_\pi + R_B}\right) \cdot V_s \tag{6.30}$$

The small-signal voltage gain is then

$$A_v = \frac{V_o}{V_s} = -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B}\right) \tag{6.31}$$

EXAMPLE 6.1

Objective: Calculate the small-signal voltage gain of the bipolar transistor circuit shown in Figure 6.3.

Assume the transistor and circuit parameters are: $\beta = 100$, $V_{CC} = 12$ V, $V_{BE} = 0.7$ V, $R_C = 6$ kΩ, $R_B = 50$ kΩ, and $V_{BB} = 1.2$ V.

DC Solution: We first do the dc analysis to find the Q-point values. We obtain

$$I_{BQ} = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{1.2 - 0.7}{50} \Rightarrow 10\ \mu\text{A}$$

so that

$$I_{CQ} = \beta I_{BQ} = (100)(10\ \mu\text{A}) \Rightarrow 1\ \text{mA}$$

Then,

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12 - (1)(6) = 6\ \text{V}$$

Therefore, the transistor is biased in the forward-active mode, as can be seen from Figure 5.25 in Chapter 5. In particular, for the npn transistor, $V_{BE} > 0$ and $V_{BC} < 0$ for the forward-active mode.

AC Solution: The small-signal hybrid-π parameters are

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{1} = 2.6\ \text{k}\Omega$$

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1}{0.026} = 38.5\ \text{mA/V}$$

The small-signal voltage gain is determined using the small-signal equivalent circuit shown in Figure 6.11. From Equation (6.31), we find

$$A_v = \frac{V_o}{V_s} = -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B}\right)$$

or

$$= -(38.5)(6)\left(\frac{2.6}{2.6 + 50}\right) = -11.4$$

Comment: We see that the magnitude of the sinusoidal output voltage is 11.4 times the magnitude of the sinusoidal input voltage. We will see that other circuit configurations result in even larger small-signal voltage gains.

Discussion: We may consider a specific sinusoidal input voltage. Let

$$v_s = 0.25 \sin \omega t\ \text{V}$$

The sinusoidal base current is given by

$$i_b = \frac{v_s}{R_B + r_\pi} = \frac{0.25 \sin \omega t}{50 + 2.6} \rightarrow 4.75 \sin \omega t\ \mu\text{A}$$

The sinusoidal collector current is

$$i_c = \beta i_b = (100)(4.75 \sin \omega t) \rightarrow 0.475 \sin \omega t\ \text{mA}$$

and the sinusoidal collector-emitter voltage is

$$v_{ce} = -i_c R_C = -(0.475)(6) \sin \omega t = -2.85 \sin \omega t\ \text{V}$$

Figure 6.12 shows the various currents and voltages in the circuit. These include the sinusoidal signals superimposed on the dc values. Figure 6.12(a) shows the sinusoidal

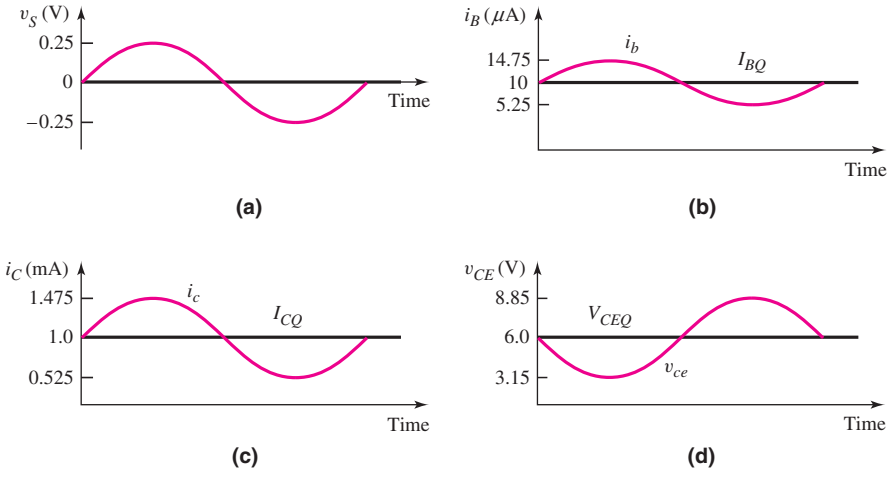


Figure 6.12 The dc and ac signals in the common-emitter circuit: (a) input voltage signal, (b) input base current, (c) output collector current, and (d) output collector-emitter voltage. The ac output voltage is 180° out of phase with respect to the input voltage signal.

input voltage, and Figure 6.12(b) shows the sinusoidal base current superimposed on the quiescent value. The sinusoidal collector current superimposed on the dc quiescent value is shown in Figure 6.12(c). Note that, as the base current increases, the collector current increases.

Figure 6.12(d) shows the sinusoidal component of the C–E voltage superimposed on the quiescent value. As the collector current increases, the voltage drop across R_C increases so that the C–E voltage decreases. Consequently, the sinusoidal component of the output voltage is 180 degrees out of phase with respect to the input signal voltage. The minus sign in the voltage gain expression represents this 180-degree **phase shift.** In summary, the signal was both amplified and inverted by this amplifier.

Analysis Method: To summarize, the analysis of a BJT amplifier proceeds as shown in the box "Problem Solving Method: Bipolar AC Analysis."

EXERCISE PROBLEM

Ex 6.1: The circuit parameters in Figure 6.3 are $V_{CC} = 5$ V, $V_{BB} = 2$ V, $R_B = 650\ \text{k}\Omega$, and $R_C = 15\ \text{k}\Omega$. The transistor parameters are $\beta = 100$ and $V_{BE}(\text{on}) = 0.7$ V. (a) Determine the Q-point values I_{CQ} and V_{CEQ}. (b) Find the small-signal hybrid-π parameters g_m and r_π. (c) Calculate the small-signal voltage gain. (Ans. (a) $I_{CQ} = 0.2$ mA, $V_{CEQ} = 2$ V; (b) $g_m = 7.69$ mA/V, $r_\pi = 13\ \text{k}\Omega$; (c) $A_v = -2.26$)

Problem-Solving Technique: Bipolar AC Analysis

Since we are dealing with linear amplifier circuits, superposition applies, which means that we can perform the dc and ac analyses separately. The analysis of the BJT amplifier proceeds as follows:

1. Analyze the circuit with only the dc sources present. This solution is the dc or quiescent solution, which uses the dc signal models for the elements, as listed

in Table 6.2. The transistor must be biased in the forward-active region in order to produce a linear amplifier.

2. Replace each element in the circuit with its small-signal model, as shown in Table 6.2. The small-signal hybrid-π model applies to the transistor although it is not specifically listed in the table.
3. Analyze the small-signal equivalent circuit, setting the dc source components equal to zero, to produce the response of the circuit to the time-varying input signals only.

Table 6.2 Transformation of elements in dc and small-signal analysis

Element	*I–V* relationship	DC model	AC model
Resistor	$I_R = \dfrac{V}{R}$	R	R
Capacitor	$I_C = sCV$	Open	C
Inductor	$I_L = \dfrac{V}{sL}$	Short	L
Diode	$I_D = I_S(e^{v_D/V_T} - 1)$	$+V_\gamma - r_f$	$r_d = V_T/I_D$
Independent voltage source	$V_S =$ constant	$+V_S-$	Short
Independent current source	$I_S =$ constant	I_S	Open

Table suggested by Richard Hester of Iowa State University.

In Table 6.2, the dc model of the resistor is a resistor, the capacitor model is an open circuit, and the inductor model is a short circuit. The forward-biased diode model includes the cut-in voltage V_γ and the forward resistance r_f.

The small-signal models of R, L, and C remain the same. However, if the signal frequency is sufficiently high, the impedance of a capacitor can be approximated by a short circuit. The small-signal, low-frequency model of the diode becomes the diode diffusion resistance r_d. Also, the independent dc voltage source becomes a short circuit, and the independent dc current source becomes an open circuit.

6.2.3 Hybrid-π Equivalent Circuit, Including the Early Effect

So far in the small-signal equivalent circuit, we have assumed that the collector current is independent of the collector–emitter voltage. We discussed the Early effect in the last chapter in which the collector current does vary with collector–emitter voltage. Equation (5.16) in the previous chapter gives the relation

$$i_C = I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]\cdot\left(1+\frac{v_{CE}}{V_A}\right) \qquad \textbf{(5.16)}$$

where V_A is the Early voltage and is a positive number. The equivalent circuits in Figures 6.9 and 6.10 can be expanded to take into account the Early voltage.

The output resistance r_o is defined as

$$r_o = \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{Q\text{-}pt} \tag{6.32}$$

Using Equations (5.16) and (6.32), we can write

$$\frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{Q\text{-}pt} = \left.\frac{\partial}{\partial v_{CE}}\left\{I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\left(1+\frac{v_{CE}}{V_A}\right)\right]\right\}\right|_{Q\text{-}pt} \tag{6.33(a)}$$

or

$$\frac{1}{r_o} = I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]\cdot\left.\frac{1}{V_A}\right|_{Q\text{-}pt} \cong \frac{I_{CQ}}{V_A} \tag{6.33(b)}$$

Then

$$r_o = \frac{V_A}{I_{CQ}} \tag{6.34}$$

and is called the **small-signal transistor output resistance.**

This resistance can be thought of as an equivalent Norton resistance, which means that r_o is in parallel with the dependent current sources. Figure 6.13(a) and (b) show the modified bipolar equivalent circuits including the output resistance r_o.

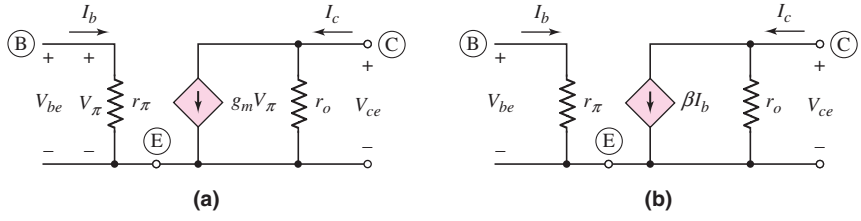


Figure 6.13 Expanded small-signal model of the BJT, including output resistance due to the Early effect, for the case when the circuit contains the (a) transconductance and (b) current gain parameters

EXAMPLE 6.2

Objective: Determine the small-signal voltage gain, including the effect of the transistor output resistance r_o.

Reconsider the circuit shown in Figure 6.3, with the parameters given in Example 6.1. In addition, assume the Early voltage is $V_A = 50$ V.

Solution: The small-signal output resistance r_o is determined to be

$$r_o = \frac{V_A}{I_{CQ}} = \frac{50}{1\text{ mA}} = 50\,\text{k}\Omega$$

Applying the small-signal equivalent circuit in Figure 6.13 to the ac equivalent circuit in Figure 6.7, we see that the output resistance r_o is in parallel with R_C. The small-signal voltage gain is therefore

$$A_v = \frac{V_o}{V_s} = -g_m(R_C \| r_o)\left(\frac{r_\pi}{r_\pi + R_B}\right) = -(38.5)(6\|50)\left(\frac{2.6}{2.6+50}\right) = -10.2$$

Comment: Comparing this result to that of Example 6.1, we see that r_o reduces the magnitude of the small-signal voltage gain. In many cases, the magnitude of r_o is much larger than that of R_C, which means that the effect of r_o is negligible.

EXERCISE PROBLEM

Ex 6.2: For the circuit in Figure 6.3 let $\beta = 150$, $V_A = 200$ V, $V_{CC} = 7.5$ V, $V_{BE}(\text{on}) = 0.7$ V, $R_C = 15$ kΩ, $R_B = 100$ kΩ, and $V_{BB} = 0.92$ V. (a) Determine the small-signal hybrid-π parameters r_π, g_m, and r_o. (b) Find the small-signal voltage gain $A_v = V_o/V_s$. (Ans. (a) $g_m = 12.7$ mA/V, $r_\pi = 11.8$ kΩ, $r_o = 606$ kΩ (b) $A_v = -19.6$)

The hybrid-π model derives its name, in part, from the hybrid nature of the parameter units. The four parameters of the equivalent circuits shown in Figures 6.13(a) and 6.13(b) are: input resistance r_π (ohms), current gain β (dimensionless), output resistance r_o (ohms), and transconductance g_m (mhos).

Up to this point, we have considered only circuits with npn bipolar transistors. However, the same basic analysis and equivalent circuit also applies to the pnp transistor. Figure 6.14(a) shows a circuit containing a pnp transistor. Here again, we see the change of current directions and voltage polarities compared to the circuit containing the npn transistor. Figure 6.14(b) is the ac equivalent circuit, with the dc voltage sources replaced by an ac short circuit, and all current and voltages shown are only the sinusoidal components.

The transistor in Figure 6.14(b) can now be replaced by either of the hybrid-π equivalent circuits shown in Figure 6.15. The hybrid-π equivalent circuit of the pnp

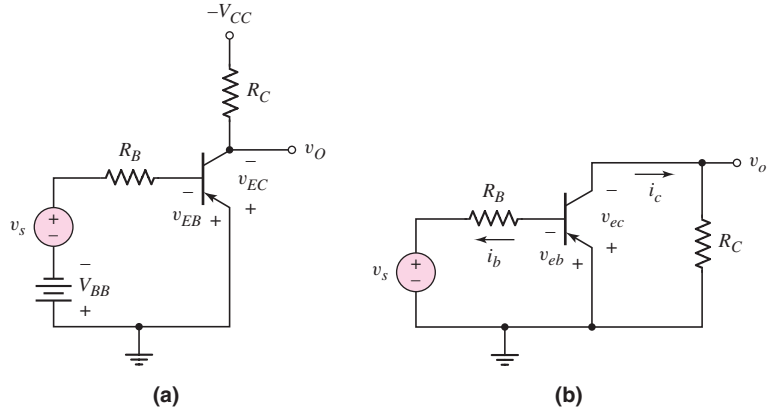


Figure 6.14 (a) A common-emitter circuit with a pnp transistor and (b) the corresponding ac equivalent circuit

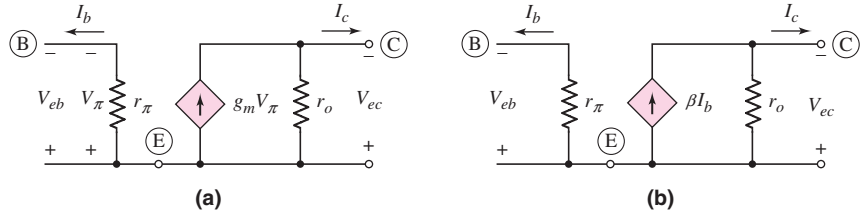


Figure 6.15 The small-signal hybrid-π equivalent circuit for the pnp transistor with the (a) transconductance and (b) current gain parameters. The ac voltage polarities and current directions are consistent with the dc parameters.

transistor is the same as that of the npn device, except that again all current directions and voltage polarities are reversed. The hybrid-π parameters are determined by using exactly the same equations as for the npn device; that is, Equation (6.21) for r_π, Equation (6.25) for g_m, and Equation (6.34) for r_o.

We can note that, in the small-signal equivalent circuits in Figure 6.15, if we define currents of opposite direction and voltages of opposite polarity, the equivalent circuit model is exactly the same as that of the npn bipolar transistor. Figure 6.16(a) is a repeat of Figure 6.15(a) showing the conventional voltage polarities and current directions in the hybrid-π equivalent circuit for a pnp transistor. Keep in mind that these voltages and currents are small-signal parameters. If the polarity of the input control voltage V_π is reversed, then the direction of the current from the dependent current source is also reversed. This change is shown in Figure 6.16(b). We may note that this small-signal equivalent circuit is the same as the hybrid-π equivalent circuit for the npn transistor.

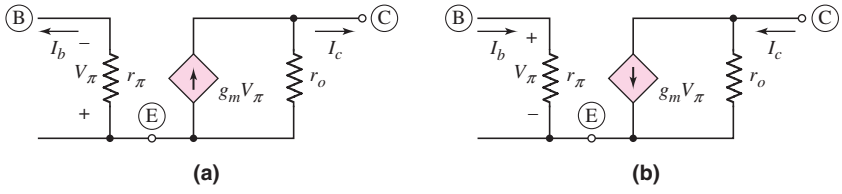


Figure 6.16 Small-signal hybrid-π models of the pnp transistor: (a) original circuit shown in Figure 6.15 and (b) equivalent circuit with voltage polarities and current directions reversed

However, the author prefers to use the models shown in Figure 6.15 because the current directions and voltage polarities are consistent with the pnp device.

Combining the hybrid-π model of the pnp transistor (Figure 6.15(a)) with the ac equivalent circuit (Figure 6.14(b)), we obtain the small-signal equivalent circuit shown in Figure 6.17. The output voltage is given by

$$V_o = (g_m V_\pi)(r_o \| R_C) \tag{6.35}$$

The control voltage V_π can be expressed in terms of the input signal voltage V_s using a voltage divider equation. Taking into account the polarity, we find

$$V_\pi = -\frac{V_s r_\pi}{R_B + r_\pi} \tag{6.36}$$

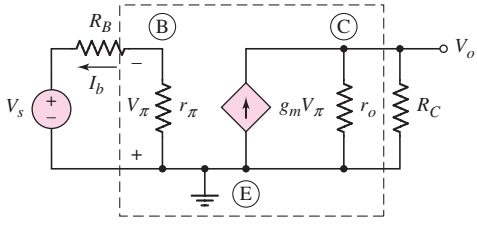


Figure 6.17 The small-signal equivalent circuit of the common-emitter circuit with a pnp transistor. The small-signal hybrid-π equivalent circuit model of the pnp transistor is shown within the dashed lines.

Combining Equations (6.35) and (6.36), we obtain the small-signal voltage gain:

$$A_v = \frac{V_o}{V_s} = \frac{-g_m r_\pi}{R_B + r_\pi}(r_o \| R_C) = \frac{-\beta}{R_B + r_\pi}(r_o \| R_C) \tag{6.37}$$

The expression for the small-signal voltage gain of the circuit containing a pnp transistor is exactly the same as that for the npn transistor circuit. Taking into account the reversed current directions and voltage polarities, the voltage gain still contains a negative sign indicating a 180-degree phase shift between the input and output signals.

EXAMPLE 6.3

Objective: Analyze a pnp amplifier circuit.

Consider the circuit shown in Figure 6.18. Assume transistor parameters of $\beta = 80$, $V_{EB}(\text{on}) = 0.7$ V, and $V_A = \infty$.

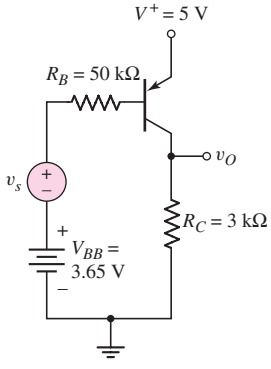


Figure 6.18 pnp common-emitter circuit for Example 6.3

Solution (DC Analysis): A dc KVL equation around the E–B loop yields

$$V^+ = V_{EB}(\text{on}) + I_{BQ}R_B + V_{BB}$$

or

$$5 = 0.7 + I_{BQ}(50) + 3.65$$

which yields

$$I_{BQ} = 13\ \mu\text{A}$$

Then

$$I_{CQ} = 1.04\ \text{mA} \qquad I_{EQ} = 1.05\ \text{mA}$$

A dc KVL equation around the E–C loop yields

$$V^+ = V_{ECQ} + I_{CQ}R_C$$

or

$$5 = V_{ECQ} + (1.04)(3)$$

We find

$$V_{ECQ} = 1.88\ \text{V}$$

The transistor is therefore biased in the forward-active mode.

Solution (AC Analysis): The small-signal hybrid-π parameters are found to be

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.04}{0.026} = 40\ \text{mA/V}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(80)(0.026)}{1.04} = 2\ \text{k}\Omega$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{\infty}{1.04} = \infty$$

The small-signal equivalent circuit is the same as shown in Figure 6.17. With $r_o = \infty$, the small-signal output voltage is

$$V_o = (g_m V_\pi)R_C$$

and we have

$$V_\pi = -\left(\frac{r_\pi}{r_\pi + R_B}\right) \cdot V_s$$

Noting that $\beta = g_m r_\pi$, we find the small-signal voltage gain to be

$$A_v = \frac{V_o}{V_s} = \frac{-\beta R_C}{r_\pi + R_B} = \frac{-(80)(3)}{2 + 50}$$

or

$$A_v = -4.62$$

Comment: We again note the $-180°$ phase shift between the output and input signals. We may also note that the base resistance R_B in the denominator substantially reduces the magnitude of the small-signal voltage gain. We can also note that placing the pnp transistor in this configuration allows us to use positive power supplies.

EXERCISE PROBLEM

Ex 6.3: For the circuit in Figure 6.14(a), let $\beta = 90$, $V_A = 120$ V, $V_{CC} = 5$ V, $V_{EB}(\text{on}) = 0.7$ V, $R_C = 2.5$ kΩ, $R_B = 50$ kΩ, and $V_{BB} = 1.145$ V. (a) Determine the small-signal hybrid-π parameters r_π, g_m, and r_o. (b) Find the small-signal voltage gain $A_v = V_o/V_s$. (Ans. (a) $g_m = 30.8$ mA/V, $r_\pi = 2.92$ kΩ, $r_o = 150$ kΩ (b) $A_v = -4.18$)

Test Your Understanding

TYU 6.1 A BJT with $\beta = 120$ and $V_A = 150$ V is biased such that $I_{CQ} = 0.25$ mA. Determine g_m, r_π, and r_o. (Ans. $g_m = 9.62$ mA/V, $r_\pi = 12.5$ kΩ, $r_o = 600$ kΩ)

TYU 6.2 The Early voltage of a BJT is $V_A = 75$ V. Determine the minimum required collector current such that the output resistance is at least $r_o = 200$ kΩ. (Ans. $I_{CQ} = 0.375$ mA)

*6.2.4 Expanded Hybrid-π Equivalent Circuit

Figure 6.19 shows an expanded hybrid-π equivalent circuit, which includes two additional resistances, r_b and r_μ.

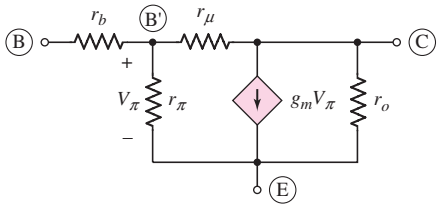


Figure 6.19 Expanded hybrid-π equivalent circuit

*Sections can be skipped without loss of continuity.

The parameter r_b is the **series resistance** of the semiconductor material between the external base terminal B and an idealized internal base region B′. Typically, r_b is a few tens of ohms and is usually much smaller than r_π; therefore, r_b is normally negligible (a short circuit) at low frequencies. However, at high frequencies, r_b may not be negligible, since the input impedance becomes capacitive, as we will see in Chapter 7.

The parameter r_μ is the **reverse-biased diffusion resistance** of the base–collector junction. This resistance is typically on the order of megohms and can normally be neglected (an open circuit). However, the resistance does provide some feedback between the output and input, meaning that the base current is a slight function of the collector–emitter voltage.

In this text, when we use the hybrid-π equivalent circuit model, we will neglect both r_b and r_μ, unless they are specifically included.

*6.2.5 Other Small-Signal Parameters and Equivalent Circuits

Other small-signal parameters can be developed to model the bipolar transistor or other transistors described in the following chapters.

One common equivalent circuit model for bipolar transistor uses the ***h*-parameters,** which relate the small-signal terminal currents and voltages of a two-port network. These parameters are normally given in bipolar transistor data sheets, and are convenient to determine experimentally at low frequency.

Figure 6.20(a) shows the small-signal terminal current and voltage phasors for a common-emitter transistor. If we assume the transistor is biased at a *Q*-point in the forward-active region, the linear relationships between the small-signal terminal currents and voltages can be written as

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \qquad \textbf{(6.38(a))}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \qquad \textbf{(6.38(b))}$$

These are the defining equations of the common–emitter *h*-parameters, where the subscripts are: *i* for input, *r* for reverse, *f* for forward, *o* for output, and *e* for common emitter.

These equations can be used to generate the small-signal *h*-parameter equivalent circuit, as shown in Figure 6.20(b). Equation (6.38(a)) represents a Kirchhoff voltage law equation at the input, and the resistance h_{ie} is in series with a dependent voltage source equal to $h_{re}V_{ce}$. Equation (6.38(b)) represents a Kirchhoff current law equation at the output, and the conductance h_{oe} is in parallel with a dependent current source equal to $h_{fe}I_b$.

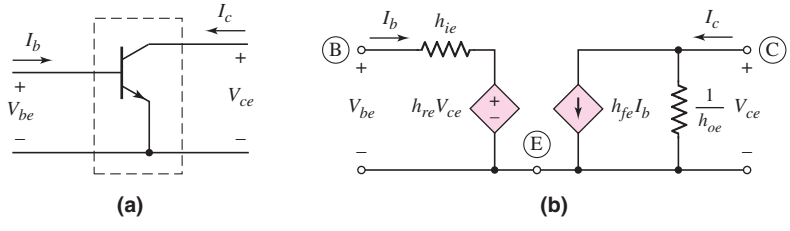


Figure 6.20 (a) Common-emitter npn transistor and (b) the *h*-parameter model of the common-emitter bipolar transistor

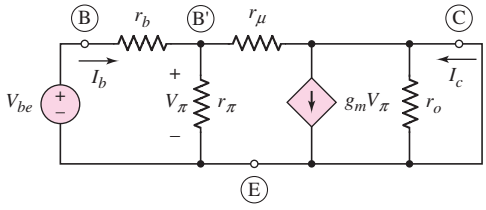


Figure 6.21 Expanded hybrid-π equivalent circuit with the output short-circuited

Since both the hybrid-π and h-parameters can be used to model the characteristics of the same transistor, these parameters are not independent. We can relate the hybrid-π and h-parameters using the equivalent circuit shown in Figure 6.19. The **small-signal input resistance** h_{ie}, from Equation (6.38(a)), can be written as

$$h_{ie} = \left.\frac{V_{be}}{I_b}\right|_{V_{ce}=0} \tag{6.39}$$

where the small-signal C–E voltage is held at zero. With the C–E voltage equal to zero, the circuit in Figure 6.19 is transformed to the one shown in Figure 6.21. From this figure, we see that

$$h_{ie} = r_b + r_\pi \| r_\mu \tag{6.40}$$

In the limit of a very small r_b and a very large r_μ, $h_{ie} \cong r_\pi$.

The parameter h_{fe} is the **small-signal current gain.** From Equation (6.38(b)), this parameter can be written as

$$h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0} \tag{6.41}$$

Since the collector–emitter voltage is again zero, we can use Figure 6.21, for which the short-circuit collector current is

$$I_c = g_m V_\pi \tag{6.42}$$

If we again consider the limit of a very small r_b and a very large r_μ, then

$$V_\pi = I_b r_\pi$$

and

$$h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0} = g_m r_\pi = \beta \tag{6.43}$$

Consequently, at low frequency, the small-signal current gain h_{fe} is essentially equal to β in most situations.

The parameter h_{re} is called the **voltage feedback ratio,** which, from Equation (6.38(a)), can be written as

$$h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0} \tag{6.44}$$

Since the input signal base current is zero, the circuit in Figure 6.19 transformed to that shown in Figure 6.22, from which we can see that

$$V_{be} = V_\pi = \left(\frac{r_\pi}{r_\pi + r_\mu}\right) \cdot V_{ce} \tag{6.45(a)}$$

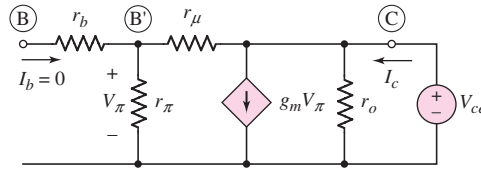


Figure 6.22 Expanded hybrid-π equivalent circuit with the input open-circuited

and

$$h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0} = \frac{r_\pi}{r_\pi + r_\mu} \tag{6.45(b))}$$

Since $r_\pi \ll r_\mu$, this can be approximated as

$$h_{re} \cong \frac{r_\pi}{r_\mu} \tag{6.46}$$

Since r_π is normally in the kilohm range and r_μ is in the megohm range, the value of h_{re} is very small and can usually be neglected.

The fourth h-parameter is the **small-signal output admittance** h_{oe}. From Equation (6.38(b)), we can write

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} \tag{6.47}$$

Since the input signal base current is again set equal to zero, the circuit in Figure 6.22 is applicable, and a Kirchhoff current law equation at the output node produces

$$I_c = g_m V_\pi + \frac{V_{ce}}{r_o} + \frac{V_{ce}}{r_\pi + r_\mu} \tag{6.48}$$

where V_π is given by Equation (6.45(a)). For $r_\pi \ll r_\mu$, Equation (6.48) becomes

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} = \frac{1+\beta}{r_\mu} + \frac{1}{r_o} \tag{6.49}$$

In the ideal case, r_μ is infinite, which means that $h_{oe} = 1/r_o$.

The h-parameters for a pnp transistor are defined in the same way as those for an npn device. Also, the small-signal equivalent circuit for a pnp transistor using h-parameters is identical to that of an npn device, except that the current directions and voltage polarities are reversed.

EXAMPLE 6.4

Objective: Determine the h-parameters of a specific transistor.

The 2N2222A transistor is a commonly used discrete npn transistor. Data for this transistor are shown in Figure 6.23. Assume the transistor is biased at $I_C = 1$ mA and let $T = 300$ K.

Solution: In Figure 6.23, we see that the small-signal current gain h_{fe} is generally in the range $100 < h_{fe} < 170$ for $I_C = 1$ mA, and the corresponding value of h_{ie} is generally between 2.5 and 5 kΩ. The voltage feedback ratio h_{re} varies between

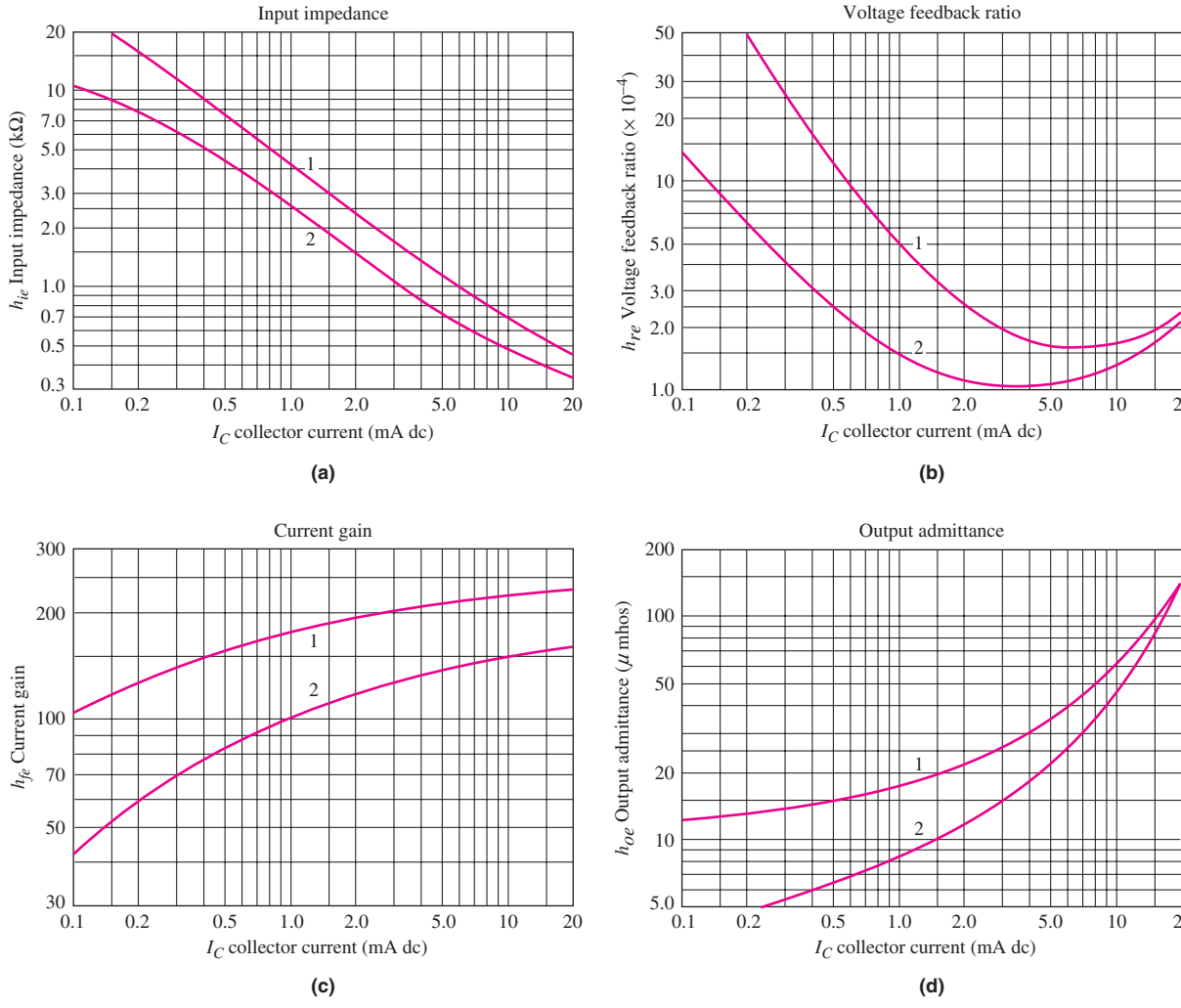


Figure 6.23 *h*-parameter data for the 2N2222A transistor. Curves 1 and 2 represent data from high-gain and low-gain transistors, respectively.

1.5×10^{-4} and 5×10^{-4}, and the output admittance h_{oe} is in the range $8 < h_{oe} < 18$ μmhos.

Comment: The purpose of this example is to show that the parameters of a given transistor type can vary widely. In particular, the current gain parameter can easily vary by a factor of two. These variations are due to tolerances in the initial semiconductor properties and in the production process variables.

Design Pointer: This example clearly shows that there can be a wide variation in transistor parameters. Normally, a circuit is designed using nominal parameter values, but the allowable variations must be taken into account. In Chapter 5, we noted how a variation in β affects the Q-point. In this chapter, we will see how the variations in small-signal parameters affect the small-signal voltage gain and other characteristics of a linear amplifier.

EXERCISE PROBLEM

Ex 6.4: Repeat Example 6.4 if the quiescent collector current is (a) $I_{CQ} = 0.2$ mA and (b) $I_{CQ} = 5$ mA. [Ans. (a) $7.8 < h_{ie} < 15$ kΩ, $6.2 \times 10^{-4} < h_{re} < 50 \times 10^{-4}$, $60 < h_{fe} < 125$, $5 < h_{oe} < 13$ μmhos; (b) $0.7 < h_{ie} < 1.1$ kΩ, $1.05 \times 10^{-4} < h_{re} < 1.6 \times 10^{-4}$, $140 < h_{fe} < 210$, $22 < h_{oe} < 35$ μmhos)

In the previous discussion, we indicated that the h-parameters h_{ie} and $1/h_{oe}$ are essentially equivalent to the hybrid-π parameters r_π and r_o, respectively, and that h_{fe} is essentially equal to β. The transistor circuit response is independent of the transistor model used. This reinforces the concept of a relationship between hybrid-π parameters and h-parameters. In fact, this is true for any set of small-signal parameters; that is, any given set of small-signal parameters is related to any other set of parameters.

Data Sheet

In the previous example, we showed some data for the 2N2222 discrete transistor. Figure 6.24 shows additional data from the data sheet for this transistor. Data sheets contain a lot of information, but we can begin to discuss some of the data at this time.

The first set of parameters pertains to the transistor in cutoff. The first two parameters listed are $V_{(BR)CEO}$ and $V_{(BR)CBO}$, which are the collector–emitter breakdown voltage with the base terminal open and the collector–base breakdown voltage with the emitter open. These parameters were discussed in Section 5.1.6 in the last chapter. In that section, we argued that $V_{(BR)CBO}$ was larger than $V_{(BR)CEO}$, which is supported by the data shown. These two voltages are measured at a specific current in the breakdown region. The third parameter, $V_{(BR)EBO}$, is the emitter–base breakdown voltage, which is substantially less than the collector–base or collector–emitter breakdown voltages.

The current I_{CBO} is the reverse-biased collector–base junction current with the emitter open ($I_E = 0$). This parameter was also discussed in Section 5.1.6. In the data sheet, this current is measured at two values of collector–base voltage and at two temperatures. The reverse-biased current increases with increasing temperature, as we would expect. The current I_{EBO} is the reverse-biased emitter–base junction current with the collector open ($I_C = 0$). This current is also measured at a specific reverse-bias voltage. The other two current parameters, I_{CEX} and I_{BL}, are the collector current and base current measured at given specific cutoff voltages.

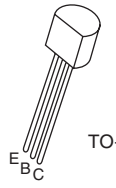
The next set of parameters applies to the transistor when it is turned on. As was shown in Example 6.4, the data sheets give the h-parameters of the transistor. The first parameter, h_{FE}, is the dc common-emitter current gain and is measured over a wide range of collector current. We discussed, in Section 5.4.2, stabilizing the Q-point against variations in current gain. The data presented in the data sheet show that the current gain for a given transistor can vary significantly, so that stabilizing the Q-point is indeed an important issue.

We have used $V_{CE}(\text{sat})$ as one of the piecewise linear parameters when a transistor is driven into saturation and have always assumed a particular value in our analysis or design. This parameter, listed in the data sheet, is not a constant but varies with collector current. If the collector becomes relatively large, then the collector–emitter saturation voltage also becomes relatively large. The larger $V_{CE}(\text{sat})$ value would need to be taken into account in large-current situations. The base–emitter voltage for a transistor driven into saturation, $V_{BE}(\text{sat})$, is also given. Up to this point

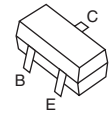
National Semiconductor

2N2222 2N2222A | PN2222 PN2222A | MMBT2222 MMBT2222A | MPQ2222


TO–18



TO–92



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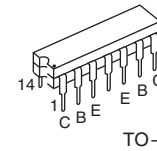
(SOT–23)



TO–116

NPN General Purpose Amplifier

Electrical Characteristics T_A = 25 °C unless otherwise noted

Symbol	Parameter		Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 1) (I_C = 10 mA, I_B = 0)	2222 2222A	30 40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	2222 2222A	60 75		V
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	2222 2222A	5.0 6.0		V
I_{CEX}	Collector Cutoff Current (V_{CE} = 60 V, V_{EB}(off) = 3.0 V)	2222A		10	nA
I_{CBO}	Collector Cutoff Current (V_{CB} = 50 V, I_E = 0) (V_{CB} = 60 V, I_E = 0) (V_{CB} = 50 V, I_E = 0, T_A = 150 °C) (V_{CB} = 60 V, I_E = 0, T_A = 150 °C)	 2222 2222A 2222 2222A		 0.01 0.01 10 10	μA
I_{EBO}	Emitter Cutoff Current (V_{EB} = 3.0 V, I_C = 0)	2222A		10	nA
I_{BL}	Base Cutoff Current (V_{CE} = 60 V, V_{EB}(off) = 3.0)	2222A		20	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (I_C = 0.1 mA, V_{CE} = 10 V) (I_C = 1.0 mA, V_{CE} = 10 V) (I_C = 10 mA, V_{CE} = 10 V) (I_C = 10 mA, V_{CE} = 10 V, T_A = −55 °C) (I_C = 150 mA, V_{CE} = 10 V) (Note 1) (I_C = 150 mA, V_{CE} = 1.0 V) (Note 1) (I_C = 500 mA, V_{CE} = 10 V) (Note 1)	 2222 2222A	 35 50 75 35 100 50 30 40	 300 	

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Figure 6.24 Basic data sheet for the 2N2222 bipolar transistor

2222/PN2222/MMBT2222/MPQ2222/2N2222A/PN2222A/MMBT2222A NPN General Purpose Amplifier

NPN General Purpose Amplifier (Continued)

Electrical Characteristics T_A = 25 °C unless otherwise noted (Continued)

Symbol	Parameter		Min	Max	Units
ON CHARACTERISTICS (Continued)					
V_{CE} (sat)	Collector-Emitter Saturation Voltage (Note 1) (I_C = 150 mA, I_B = 15 mA) (I_C = 500 mA, I_B = 50 mA)	2222 2222A 2222 2222A		0.4 0.3 1.6 1.0	V
V_{BE} (sat)	Base-Emitter Saturation Voltage (Note 1) (I_C = 150 mA, I_B = 15 mA) (I_C = 500 mA, I_B = 50 mA)	2222 2222A 2222 2222A	0.6 0.6	1.3 1.2 2.6 2.0	V
SMALL-SIGNAL CHARACTERISTICS					
f_T	Current Gain—Bandwidth Product (Note 3) (I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz)	2222 2222A	250 300		MHz
C_{obo}	Output Capacitance (Note 3) (V_{CB} = 10 V, I_E = 0, f = 100 kHz)			8.0	pF
C_{ibo}	Input Capacitance (Note 3) (V_{EB} = 0.5 V, I_C = 0, f = 100 kHz)	2222 2222A		30 25	pF
$rb'C_C$	Collector Base Time Constant (I_E = 20 mA, V_{CB} = 20 V, f = 31.8 MHz)	2222A		150	ps
NF	Noise Figure (I_C = 100 μA, V_{CE} = 10 V, R_S = 1.0 kΩ, f = 1.0 kHz)	2222A		4.0	dB
$Re(h_{ie})$	Real Part of Common-Emitter High Frequency Input Impedance (I_C = 20 mA, V_{CE} = 20 V, f = 300 MHz)			60	Ω
SWITCHING CHARACTERISTICS					
t_D	Delay Time	(V_{CC} = 30 V, V_{BE}(off) = 0.5 V, I_C = 150 mA, I_{B1} = 15 mA) except MPQ2222		10	ns
t_R	Rise Time			25	ns
t_S	Storage Time	(V_{CC} = 30 V, I_C = 150 mA, I_{B1} = I_{B2} = 15 mA) except MPQ2222		225	ns
t_F	Fall Time			60	ns

Note 1: Pulse Test: Pulse Width < 300 μs, Duty Cycle ≤ 2.0%.
Note 2: For characteristics curves, see Process 19.
Note 3: f_T is defined as the frequency at which h_{fe} extrapolates to unity.

Figure 6.24 (*continued*)

in the text, we have not been concerned with this parameter; however, the data sheet shows that the base–emitter voltage can increase significantly when a transistor is driven into saturation at high current levels.

The other parameters listed in the data sheet become more applicable later in the text when the frequency response of transistors is discussed. The intent of this short discussion is to show that we can begin to read through data sheets even though there are a lot of data presented.

The T-model: The hybrid-pi model can be used to analyze the time-varying characteristics of all transistor circuits. We have briefly discussed the h-parameter model of the transistor. The h-parameters of this model are often given in data sheets for discrete transistors. Another small-signal model of the transistor, the T-model, is shown in Figure 6.25. This model might be convenient to use in specific applications. However, to avoid introducing too much confusion, we will concentrate on using the hybrid-pi model in this text and leave the T-model to more advanced electronics courses.

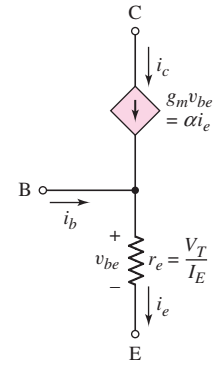


Figure 6.25 The T-model of an npn bipolar transistor

6.3 BASIC TRANSISTOR AMPLIFIER CONFIGURATIONS

Objective: • Discuss the three basic transistor amplifier configurations and discuss the four equivalent two-port networks.

As we have seen, the bipolar transistor is a three-terminal device. Three basic single-transistor amplifier configurations can be formed, depending on which of the three transistor terminals is used as signal ground. These three basic configurations are appropriately called **common emitter, common collector (emitter follower),** and **common base.** Which configuration or amplifier is used in a particular application depends to some extent on whether the input signal is a voltage or current and whether the desired output signal is a voltage or current. The characteristics of the three types of amplifiers will be determined to show the conditions under which each amplifier is most useful.

The input signal source can be modeled as either a Thevenin or Norton equivalent circuit. Figure 6.26(a) shows the Thevenin equivalent source that would represent a voltage signal, such as the output of a microphone. The voltage source v_s represents the voltage generated by the microphone. The resistance R_S is called the output resistance of the source and takes into account the change in output voltage as the source supplies current. Figure 6.26(b) shows the Norton equivalent source that

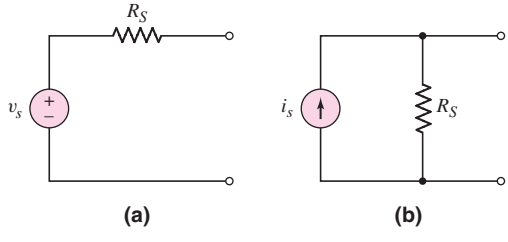
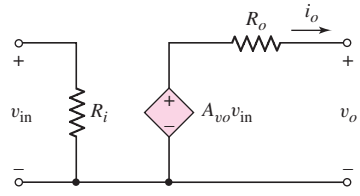
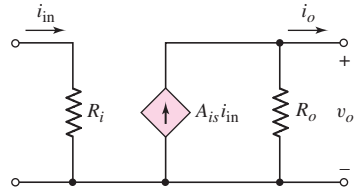
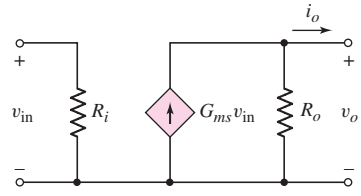
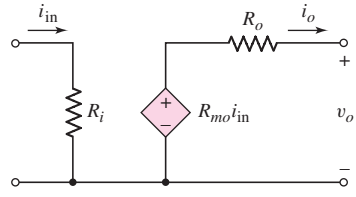


Figure 6.26. Input signal source modeled as (a) Thevenin equivalent circuit and (b) Norton equivalent circuit

Table 6.3 Four equivalent two-port networks

Type	Equivalent circuit	Gain property
Voltage amplifier		Output voltage proportional to input voltage
Current amplifier		Output current proportional to input current
Transconductance amplifier		Output current proportional to input voltage
Transresistance amplifier		Output voltage proportional to input current

would represent a current signal, such as the output of a photodiode. The current source i_s represents the current generated by the photodiode and the resistance R_S is the output resistance of this signal source.

Each of the three basic transistor amplifiers can be modeled as a two-port network in one of four configurations as shown in Table 6.3. We will determine the gain parameters, such as A_{vo}, A_{io}, G_{mo}, and R_{mo}, for each of the three transistor amplifiers. These parameters are important since they determine the amplification of the amplifier. However, we will see that the input and output resistances, R_i and R_o, are also important in the design of these amplifiers. Although one configuration shown in Table 6.3 may be preferable for a given application, any one of the four can be used to model a given amplifier. Since each configuration must produce the same terminal characteristics for a given amplifier, the various gain parameters are not independent, but are related to each other.

If we wish to design a voltage amplifier (preamp) so that the output voltage of a microphone, for example, is amplified, the total equivalent circuit may be that shown in Figure 6.27. The input voltage to the amplifier is given by

$$v_{\text{in}} = \frac{R_i}{R_i + R_S} \cdot v_s \tag{6.50}$$

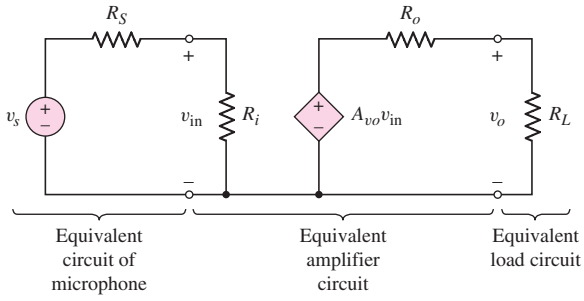


Figure 6.27 Equivalent preamplifier circuit

In general, we would like the input voltage v_{in} to the amplifier to be as nearly equal to the source voltage v_s as possible. This means, from Equation (6.50), that we need to design the amplifier such that the input resistance R_i is much larger than the signal source output resistance R_S. (The output resistance of an ideal voltage source is zero, but is not zero for most practical voltage sources.) To provide a particular voltage gain, the amplifier must have a gain parameter A_{vo} of a certain value. The output voltage supplied to the load (where the load may be a second power amplifier stage) is given by

$$v_o = \frac{R_L}{R_L + R_o} \cdot A_{vo} v_{in} \tag{6.51}$$

Normally, we would like the output voltage to the load to be equal to the Thevenin equivalent voltage generated by the amplifier. This means that we need $R_o \ll R_L$ for the voltage amplifier. So again, for a voltage amplifier, the output resistance should be very small. The input and output resistances are significant in the design of an amplifier.

For a current amplifier, we would like to have $R_i \ll R_S$ and $R_o \gg R_L$. We will see as we proceed through the chapter that each of the three basic transistor amplifier configurations exhibits characteristics that are desirable for particular applications.

We should note that, in this chapter, we will be primarily using the two-port equivalent circuits shown in Table 6.3 to model single-transistor amplifiers. However, these equivalent circuits are also used to model multitransistor circuits. This will become apparent as we get into Part 2 of the text.

6.4 COMMON-EMITTER AMPLIFIERS

Objective: • Analyze the common-emitter amplifier and become familiar with the general characteristics of this circuit.

In this section, we consider the first of the three basic amplifiers—the **common-emitter** circuit. We will apply the equivalent circuit of the bipolar transistor that was previously developed. In general, we will use the hybrid-π model throughout the text.

6.4.1 Basic Common-Emitter Amplifier Circuit

Figure 6.28 shows the basic common-emitter circuit with voltage-divider biasing. We see that the emitter is at ground potential—hence the name common emitter. The signal from the signal source is coupled into the base of the transistor through the coupling capacitor C_C, which provides dc isolation between the amplifier and the signal source. The dc transistor biasing is established by R_1 and R_2, and is not disturbed when the signal source is capacitively coupled to the amplifier.

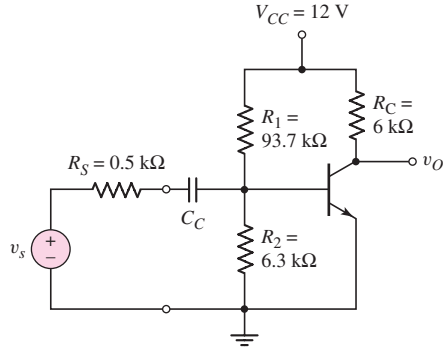


Figure 6.28 A common-emitter circuit with a voltage-divider biasing circuit and a coupling capacitor

If the signal source is a sinusoidal voltage at frequency f, then the magnitude of the capacitor impedance is $|Z_c| = [1/(2\pi f C_C)]$. For example, assume that $C_C = 10\ \mu$F and $f = 2$ kHz. The magnitude of the capacitor impedance is then

$$|Z_c| = \frac{1}{2\pi f C_C} = \frac{1}{2\pi(2 \times 10^3)(10 \times 10^{-6})} \cong 8\ \Omega \tag{6.52}$$

The magnitude of this impedance is much less than the Thevenin resistance at the capacitor terminals, which in this case is $R_1 \| R_2 \| r_\pi$. We can therefore assume that the capacitor is essentially a short circuit to signals with frequencies greater than 2 kHz. We are also neglecting any capacitance effects within the transistor. Using these results, our analyses in this chapter assume that the signal frequency is sufficiently high that any coupling capacitance acts as a perfect short circuit, and is also sufficiently low that the transistor capacitances can be neglected. Such frequencies are in the midfrequency range, or simply at the midband of the amplifier.

The small-signal equivalent circuit in which the coupling capacitor is assumed to be a short circuit is shown in Figure 6.29. The small-signal variables, such as the

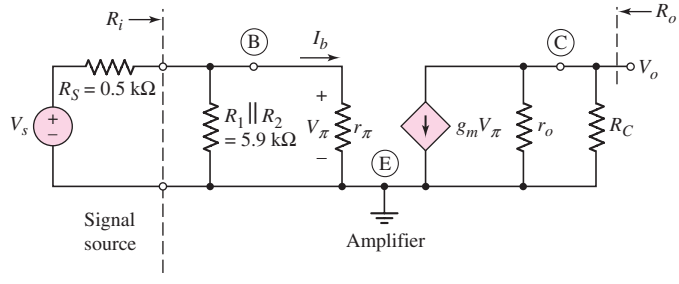


Figure 6.29 The small-signal equivalent circuit, assuming the coupling capacitor is a short circuit

input signal voltage and input base current, are given in phasor form. The control voltage V_π is also given as a phasor.

EXAMPLE 6.5

Objective: Determine the small-signal voltage gain, input resistance, and output resistance of the circuit shown in Figure 6.28.

Assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 100$ V.

DC Solution: We first perform a dc analysis to find the Q-point values. We find that $I_{CQ} = 0.95$ mA and $V_{CEQ} = 6.31$ V, which shows that the transistor is biased in the forward-active mode.

AC Solution: The small-signal hybrid-π parameters for the equivalent circuit are

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{(0.95)} = 2.74\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.95}{0.026} = 36.5\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.95} = 105\,\text{k}\Omega$$

Assuming that C_C acts as a short circuit, Figure 6.29 shows the small-signal equivalent circuit. The small-signal output voltage is

$$V_o = -(g_m V_\pi)(r_o \| R_C)$$

The dependent current $g_m V_\pi$ flows through the parallel combination of r_o and R_C, but in a direction that produces a negative output voltage. We can relate the control voltage V_π to the input voltage V_s by a voltage divider. We have

$$V_\pi = \left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_S}\right) \cdot V_s$$

We can then write the small-signal voltage gain as

$$A_v = \frac{V_o}{V_s} = -g_m \left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_S}\right)(r_o \| R_C)$$

or

$$A_v = -(36.5)\left(\frac{5.9 \| 2.74}{5.9 \| 2.74 + 0.5}\right)(105 \| 6) = -163$$

We can also calculate R_i, which is the resistance to the amplifier. From Figure 6.29, we see that

$$R_i = R_1 \| R_2 \| r_\pi = 5.9 \| 2.74 = 1.87\,\text{k}\Omega$$

The output resistance R_o is found by setting the independent source V_s equal to zero. In this case, there is no excitation to the input portion of the circuit so $V_\pi = 0$, which implies that $g_m V_\pi = 0$ (an open circuit). The output resistance looking back into the output terminals is then

$$R_o = r_o \| R_C = 105 \| 6 = 5.68\,\text{k}\Omega$$

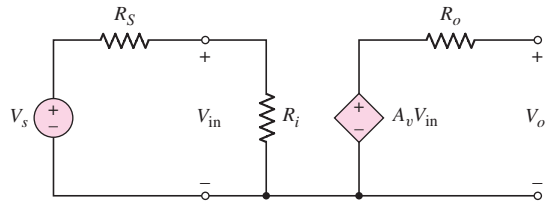


Figure 6.30 Two-port equivalent circuit for the amplifier in Example 6.5

Comment: In this circuit, the effective series resistance between the voltage source V_s and the base of the transistor is much less than that given in Example 6.1. For this reason, the magnitude of the voltage gain for the circuit given in Figure 6.28 is much larger than that found in Example 6.1.

Discussion: The two-port equivalent circuit along with the input signal source for the common-emitter amplifier analyzed in this example is shown in Figure 6.30. We can determine the effect of the source resistance R_S in conjunction with the amplifier input resistance R_i. Using a voltage-divider equation, we find the input voltage to the amplifier is

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_S}\right) V_s = \left(\frac{1.87}{1.87 + 0.5}\right) V_s = 0.789\, V_s$$

Because the input resistance to the amplifier is not very much greater than the signal source resistance, the actual input voltage to the amplifier is reduced to approximately 80 percent of the signal voltage. This is called a **loading effect.** The voltage V_{in} is a function of the amplifier connected to the source. In other amplifier designs, we will try to minimize the loading effect, or make $R_i \gg R_S$, which means that $V_{\text{in}} \cong V_s$.

EXERCISE PROBLEM

Ex 6.5: The circuit parameters in Figure 6.28 are changed to $V_{CC} = 5$ V, $R_1 = 35.2\,\text{k}\Omega$, $R_2 = 5.83\,\text{k}\Omega$, $R_C = 10\,\text{k}\Omega$, and $R_S = 0$. Assume the transistor parameters are the same as listed in Example 6.5. Determine the quiescent collector current and collector-emitter voltage, and find the small-signal voltage gain. (Ans. $I_{CQ} = 0.21$ mA, $V_{CEQ} = 2.9$ V, $A_v = -79.1$)

6.4.2 Circuit with Emitter Resistor

For the circuit in Figure 6.28, the bias resistors R_1 and R_2 in conjunction with V_{CC} produce a base current of 9.5 μA and a collector current of 0.95 mA, when the B–E turn-on voltage is assumed to be 0.7 V. If the transistor in the circuit is replaced by a new one with slightly different parameters so that the B–E turn-on voltage is 0.6 V instead of 0.7 V, then the resulting base current is 26 μA, which is sufficient to drive the transistor into saturation. Therefore, the circuit shown in Figure 6.28 is not practical. An improved dc biasing design includes an emitter resistor.

In the last chapter, we found that the Q-point was stabilized against variations in β if an emitter resistor were included in the circuit, as shown in Figure 6.31. We will find a similar property for the ac signals, in that the voltage gain of a circuit with R_E will be less dependent on the transistor current gain β. Even though the emitter of this circuit is not at ground potential, this circuit is still referred to as a common-emitter circuit.

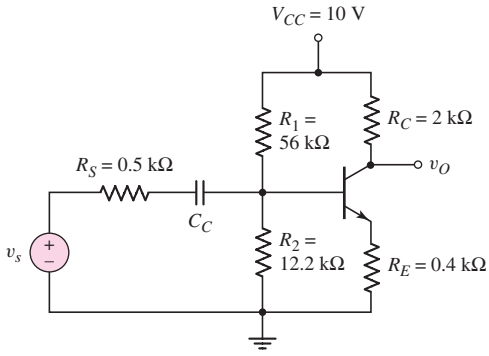


Figure 6.31 An npn common-emitter circuit with an emitter resistor, a voltage-divider biasing circuit, and a coupling capacitor

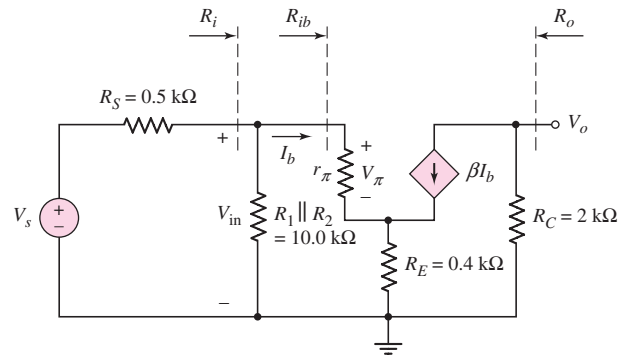


Figure 6.32 The small-signal equivalent circuit of the circuit shown in Figure 6.31

Assuming that C_C acts as a short circuit, Figure 6.32 shows the small-signal hybrid-π equivalent circuit. As we have mentioned previously, to develop the small-signal equivalent circuit, start with the three terminals of the transistor. Sketch the hybrid-π equivalent circuit between the three terminals and then sketch in the remaining circuit elements around these three terminals. In this case, we are using the equivalent circuit with the current gain parameter β, and we are assuming that the Early voltage is infinite so the transistor output resistance r_o can be neglected (an open circuit). The ac output voltage is

$$V_o = -(\beta I_b) R_C \tag{6.53}$$

To find the small-signal voltage gain, it is worthwhile finding the input resistance first. The resistance R_{ib} is the input resistance looking into the base of the transistor. We can write the following loop equation

$$V_{\text{in}} = I_b r_\pi + (I_b + \beta I_b) R_E \tag{6.54}$$

The input resistance R_{ib} is then defined as, and found to be,

$$R_{ib} = \frac{V_{\text{in}}}{I_b} = r_\pi + (1 + \beta) R_E \tag{6.55}$$

In the common-emitter configuration that includes an emitter resistance, the small-signal input resistance looking into the base of the transistor is r_π plus the emitter resistance multiplied by the factor $(1 + \beta)$. This effect is called the **resistance reflection rule.** We will use this result throughout the text without further derivation.

The input resistance to the amplifier is now

$$R_i = R_1 \| R_2 \| R_{ib} \tag{6.56}$$

We can again relate V_{in} to V_s through a voltage-divider equation as

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_S} \right) \cdot V_s \tag{6.57}$$

Combining Equations (6.53), (6.55), and (6.57), we find the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = \frac{-(\beta I_b) R_C}{V_s} = -\beta R_C \left(\frac{V_{\text{in}}}{R_{ib}} \right) \cdot \left(\frac{1}{V_s} \right) \tag{6.58(a)}$$

or

$$A_v = \frac{-\beta R_C}{r_\pi + (1+\beta)R_E}\left(\frac{R_i}{R_i + R_S}\right) \tag{6.58(b)}$$

From this equation, we see that if $R_i \gg R_S$ and if $(1+\beta)R_E \gg r_\pi$, then the small-signal voltage gain is approximately

$$A_v \cong \frac{-\beta R_C}{(1+\beta)R_E} \cong \frac{-R_C}{R_E} \tag{6.59}$$

Equations (6.58(b)) and (6.59) show that the voltage gain is less dependent on the current gain β than in the previous example, which means that there is a smaller change in voltage gain when the transistor current gain changes. The circuit designer now has more control in the design of the voltage gain, but this advantage is at the expense of a smaller gain.

In Chapter 5, we discussed the variation in the Q-point with variations or tolerances in resistor values. Since the voltage gain is a function of resistor values, it is also a function of the tolerances in those values. This must be considered in a circuit design.

EXAMPLE 6.6

Objective: Determine the small-signal voltage gain and input resistance of a common-emitter circuit with an emitter resistor.

For the circuit in Figure 6.31, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$.

DC Solution: From a dc analysis of the circuit, we can determine that $I_{CQ} = 2.16$ mA and $V_{CEQ} = 4.81$ V, which shows that the transistor is biased in the forward-active mode.

AC Solution: The small-signal hybrid-π parameters are determined to be

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{(2.16)} = 1.20\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{2.16}{0.026} = 83.1\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \infty$$

The input resistance to the base can be determined as

$$R_{ib} = r_\pi + (1+\beta)R_E = 1.20 + (101)(0.4) = 41.6\,\text{k}\Omega$$

and the input resistance to the amplifier is now found to be

$$R_i = R_1 \| R_2 \| R_{ib} = 10 \| 41.6 = 8.06\,\text{k}\Omega$$

Using the exact expression for the voltage gain, we find

$$A_v = \frac{-(100)(2)}{1.20 + (101)(0.4)}\left(\frac{8.06}{8.06 + 0.5}\right) = -4.53$$

If we use the approximation given by Equation (6.59), we obtain

$$A_v = \frac{-R_C}{R_E} = \frac{-2}{0.4} = -5.0$$

Comment: The magnitude of the small-signal voltage gain is substantially reduced when an emitter resistor is included. Also, Equation (6.59) gives a good first approximation for the gain, which means that it can be used in the initial design of a common-emitter circuit with an emitter resistor.

Discussion: The amplifier gain is nearly independent of changes in the current gain parameter β. This fact is shown in the following calculations:

β	A_v
50	−4.41
100	−4.53
150	−4.57

In addition to gaining an advantage in stability by including an emitter resistance, we also gain an advantage in the loading effect. We see that, for $\beta = 100$, the input voltage to the amplifier is

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_S}\right) \cdot V_s = (0.942)V_s$$

We see that V_{in} is much closer in value to V_s than in the previous example. There is less loading effect because the input resistance to the base of the transistor is higher when an emitter resistor is included.

The same equivalent circuit as shown in Figure 6.30 applies to this example also. The difference in the two examples is the values of input resistance and gain parameter.

EXERCISE PROBLEM

Ex 6.6: For the circuit in Figure 6.33, let $R_E = 0.6\,\text{k}\Omega$, $R_C = 5.6\,\text{k}\Omega$, $\beta = 120$, $V_{BE}(\text{on}) = 0.7$ V, $R_1 = 250\,\text{k}\Omega$, and $R_2 = 75\,\text{k}\Omega$. (a) For $V_A = \infty$, determine the small-signal voltage gain A_v. (b) Determine the input resistance looking into the base of the transistor. (Ans. (a) $A_v = -8.27$, (b) $R_{ib} = 80.1\ \text{k}\Omega$)

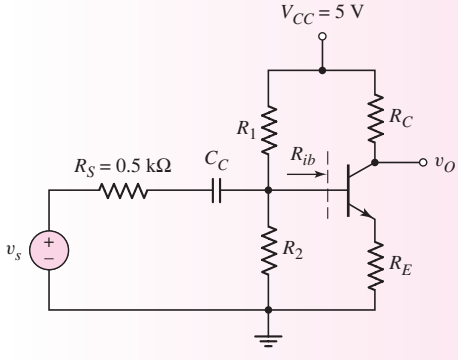


Figure 6.33 Figure for Exercise Ex6.6

COMPUTER ANALYSIS EXERCISE

PS 6.1: (a) Verify the results of Example 6.6 with a PSpice analysis. Use a standard 2N2222 transistor, for example. (b) Repeat part (a) for $R_E = 0.3\,\text{k}\Omega$.

EXAMPLE 6.7

Objective: Analyze a pnp transistor circuit.

Consider the circuit shown in Figure 6.34(a). Determine the quiescent parameter values and then the small-signal voltage gain. The transistor parameters are $V_{EB}(\text{on}) = 0.7$ V, $\beta = 80$, and $V_A = \infty$.

Solution (dc Analysis): The dc equivalent circuit with the Thevenin equivalent circuit of the base biasing is shown in Figure 6.34(b). We find

$$R_{TH} = R_1 \| R_2 = 40 \| 60 = 24\,\text{k}\Omega$$

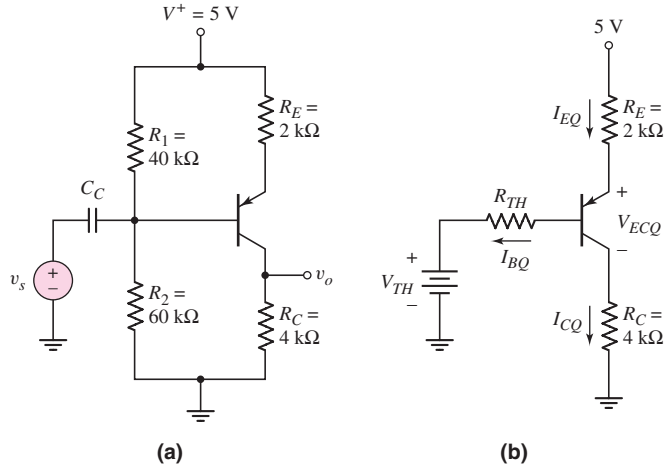


Figure 6.34 (a) pnp transistor circuit for Example 6.7 and (b) Thevenin equivalent circuit for Example 6.7

and

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) \cdot V^+ = \left(\frac{60}{60 + 40}\right)(5) = 3\,\text{V}$$

Writing a KVL equation around the E–B loop, assuming the transistor is biased in the forward-active mode, we find

$$V^+ = (1 + \beta) I_{BQ} R_E + V_{EB}(\text{on}) + I_{BQ} R_{TH} + V_{TH}$$

Solving for the base current, we obtain

$$I_{BQ} = \frac{V^+ - V_{EB}(\text{on}) - V_{TH}}{R_{TH} + (1 + \beta) R_E} = \frac{5 - 0.7 - 3}{24 + (81)(2)}$$

or

$$I_{BQ} = 0.00699\,\text{mA}$$

Then

$$I_{CQ} = \beta I_{BQ} = 0.559 \text{ mA}$$

and

$$I_{EQ} = (1 + \beta) I_{BQ} = 0.566 \text{ mA}$$

The quiescent emitter-collector voltage is

$$V_{ECQ} = V^+ - I_{EQ} R_E - I_{CQ} R_C = 5 - (0.566)(2) - (0.559)(4)$$

or

$$V_{ECQ} = 1.63 \text{ V}$$

Solution (ac analysis): The small-signal hybrid-π parameters are as follows:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(80)(0.026)}{0.559} = 3.72 \text{ k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.559}{0.026} = 21.5 \text{ mA/V}$$

and

$$r_o = \frac{V_A}{I_Q} = \infty$$

The small-signal equivalent circuit is shown in Figure 6.35. As noted before, we start with the three terminals of the transistor, sketch the hybrid-π equivalent circuit between these three terminals, and then put in the other circuit elements around the transistor.

The output voltage is

$$V_o = g_m V_\pi R_C$$

Writing a KVL equation from the input around the B–E loop, we find

$$V_s = -V_\pi - \left(\frac{V_\pi}{r_\pi} + g_m V_\pi \right) R_E$$

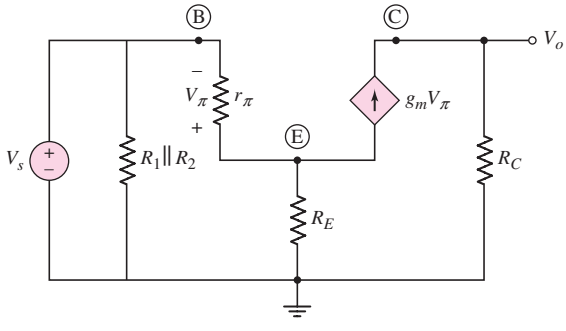


Figure 6.35 Small-signal equivalent circuit for circuit shown in Figure 6.34 (a) used in Example 6.7

The term in the parenthesis is the total current through the R_E resistor. Solving for V_π and recalling that $g_m r_\pi = \beta$, we obtain

$$V_\pi = \frac{-V_s}{1 + \left(\dfrac{1+\beta}{r_\pi}\right) R_E}$$

Substituting into the expression for the output voltage, we find the small-signal voltage gain as

$$A_v = \frac{V_o}{V_s} = \frac{-\beta R_C}{r_\pi + (1+\beta) R_E}$$

Then

$$A_v = \frac{-(80)(4)}{3.72 + (81)(2)} = -1.93$$

The negative sign indicates that the output voltage is 180 degrees out of phase with respect to the input voltage. This same result was found in common-emitter circuits using npn transistors.

Using the approximation given by Equation (6.59), we have

$$A_v \cong -\frac{R_C}{R_E} = -\frac{4}{2} = -2$$

This approximation is very close to the actual value of gain calculated.

Comment: In the previous chapter, we found that including an emitter resistor provided stability in the Q-point. However, we may note that in the small-signal analysis, the R_E resistor reduces the small-signal voltage gain substantially. There are almost always trade-offs to be made in electronic design.

EXERCISE PROBLEM

Ex 6.7: The transistor in the circuit shown in Figure 6.36 has parameters $\beta = 100$, $V_{EB}(\text{on}) = 0.7$ V, and $V_A = \infty$. Determine the quiescent collector current and emitter–collector voltage, and find the small-signal voltage gain. (Ans. $I_{CQ} = 1.74$ mA, $V_{ECQ} = 4.16$ V, $A_v = -2.56$)

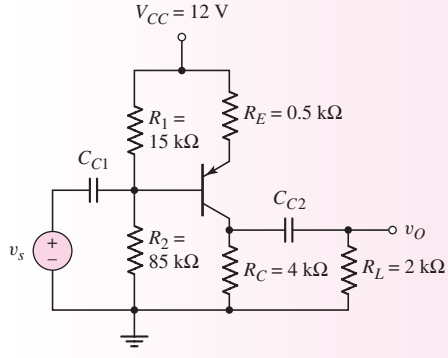


Figure 6.36 Figure for Exercise Ex6.7

Test Your Understanding

TYU 6.3 For the circuit shown in Figure 6.33, let $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Design a bias-stable circuit such that $I_{CQ} = 0.5\,\text{mA}$, $V_{CEQ} = 2.5\,\text{V}$, and $A_v = -8$. (Ans. To a good approximation: $R_C = 4.54\,\text{k}\Omega$, $R_E = 0.454\,\text{k}\Omega$, $R_1 = 24.1\,\text{k}\Omega$, and $R_2 = 5.67\,\text{k}\Omega$)

TYU 6.4 Assume a 2N2907A transistor is used in the circuit in Figure 6.36 and that the nominal dc transistor parameters are $\beta = 100$ and $V_{EB}(\text{on}) = 0.7\,\text{V}$. Determine the small-voltage gain, using the h-parameter model of the transistor. Find the minimum and maximum values of gain corresponding to the minimum and maximum h-parameter values. See Appendix C. For simplicity, assume $h_{re} = h_{oe} = 0$. (Ans. $A_v(\text{max}) = -2.59$, $A_v(\text{min}) = -2.49$)

TYU 6.5 Design the circuit in Figure 6.37 such that it is bias stable and the small-signal voltage gain is $A_v = -8$. Let $I_{CQ} = 0.6$ mA, $V_{ECQ} = 3.75$ V, $\beta = 100$, $V_{EB}(\text{on}) = 0.7$ V, and $V_A = \infty$. (Ans. To a good approximation: $R_C = 5.62\,\text{k}\Omega$, $R_E = 0.625\,\text{k}\Omega$, $R_1 = 7.41\,\text{k}\Omega$, and $R_2 = 42.5\,\text{k}\Omega$)

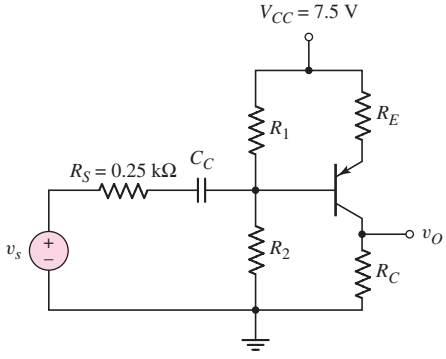


Figure 6.37 Figure for Exercise TYU6.5

TYU 6.6 For the circuit in Figure 6.31, the small-signal voltage gain is given approximately by $-R_C/R_E$. For the case of $R_C = 2\,\text{k}\Omega$, $R_E = 0.4\,\text{k}\Omega$, and $R_S = 0$, what must be the value of β such that the approximate value is within 5 percent of the actual value? (Ans. $\beta = 76$)

COMPUTER ANALYSIS EXERCISE

PS 6.2: Verify the results of Example 6.7 with a PSpice analysis. Use a standard transistor.

6.4.3 Circuit with Emitter Bypass Capacitor

There may be times when the emitter resistor must be large for the purposes of dc design, but degrades the small-signal voltage gain too severely. We can use an emitter bypass capacitor to effectively short out a portion or all of the emitter resistance as seen by the ac signals. Consider the circuit shown in Figure 6.38 biased with both

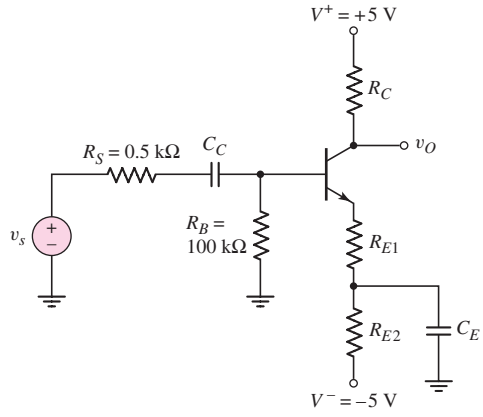


Figure 6.38 A bipolar circuit with an emitter resistor and an emitter bypass capacitor

positive and negative voltages. Both emitter resistors R_{E1} and R_{E2} are factors in the dc design of the circuit, but only R_{E1} is part of the ac equivalent circuit, since C_E provides a short circuit to ground for the ac signals. To summarize, the ac gain stability is due only to R_{E1} and most of the dc stability is due to R_{E2}.

DESIGN EXAMPLE 6.8

Objective: Design a bipolar amplifier to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 6.38 and is to amplify a 12 mV sinusoidal signal from a microphone to a 0.4 V sinusoidal output signal. We will assume that the output resistance of the microphone is 0.5 kΩ as shown.

Choices: The transistor used in the design has nominal values of $\beta = 100$ and $V_{BE}(\text{on}) = 0.7$ V, but the current gain for this type of transistor is assumed to be in the range $75 \leq \beta \leq 125$ because of tolerance effects. We will assume that $V_A = \infty$. Standard resistor values are to be used in the final design, but we will assume, in this example, that the actual resistor values are available (no tolerance effects).

Solution (Initial Design Approach): The magnitude of the voltage gain of the amplifier needs to be

$$|A_v| = \frac{0.4\,\text{V}}{12\,\text{mV}} = 33.3$$

From Equation (6.59), the approximate voltage gain of the amplifier is

$$|A_v| \cong \frac{R_C}{R_{E1}}$$

Noting from the last example that this value of gain produces an optimistically high value, we can set $R_C/R_{E1} = 40$ or $R_C = 40\,R_{E1}$.

The dc base-emitter loop equation is

$$5 = I_B R_B + V_{BE}(\text{on}) + I_E(R_{E1} + R_{E2})$$

Assuming $\beta = 100$ and $V_{BE}(\text{on}) = 0.7$ V, we can design the circuit to produce a quiescent emitter current of, for example, 0.20 mA. We then have

$$5 = \frac{(0.20)}{(101)}(100) + 0.70 + (0.20)(R_{E1} + R_{E2})$$

which yields

$$R_{E1} + R_{E2} = 20.5\,\text{k}\Omega$$

Assuming $I_E \cong I_C$ and designing the circuit such that $V_{CEQ} = 4$ V, the collector–emitter loop equation produces

$$5 + 5 = I_C R_C + V_{CEQ} + I_E(R_{E1} + R_{E2}) = (0.2)R_C + 4 + (0.2)(20.5)$$

or

$$R_C = 9.5\,\text{k}\Omega$$

Then

$$R_{E1} = \frac{R_C}{40} = \frac{9.5}{40} = 0.238\,\text{k}\Omega$$

and $R_{E2} = 20.3\,\text{k}\Omega$.

Trade-offs: From Appendix D, we will pick standard resistor values of $R_{E1} = 240\ \Omega$, $R_{E2} = 20\,\text{k}\Omega$, and $R_C = 10\,\text{k}\Omega$. We will assume that these resistor values are available and will investigate the effects of the variation in transistor current gain β.

The various parameters of the circuit for three values of β are shown in the following table. The output voltage V_o is the result of a 12 mV input signal.

β	I_{CQ} (mA)	r_π (kΩ)	$\lvert A_v \rvert$	V_o (V)
75	0.197	9.90	26.1	0.313
100	0.201	12.9	26.4	0.317
125	0.203	16.0	26.6	0.319

One important point to note is that, the output voltage is less than the design objective of 0.4 V for a 12 mV input signal. This effect will be discussed further in the next section involving the computer simulation.

A second point to note is that the quiescent collector current, small-signal voltage gain, and output voltage are relatively insensitive to the current gain β. This stability is a direct result of including the emitter resistor R_{E1}.

Computer Simulation: Since we used approximation techniques in our design, we can use PSpice to give us a more accurate valuation of the circuit for the standard resistor values that were chosen. Figure 6.39 shows the PSpice circuit schematic diagram.

Using the standard resistor values and the 2N3904 transistor, the output signal voltage produced by a 12 mV input signal is 323 mV. A frequency of 2 kHz and capacitor values of 100 μF were used in the simulation. The magnitude of the output signal is slightly less than the desired value of 400 mV. The principal reason for the difference is that the r_π parameter of the transistor was neglected in the design. For a collector current of approximately $I_C = 0.2$ mA, r_π can be significant.

In order to increase the small-signal voltage gain, a smaller value of R_{E1} is necessary. For $R_{E1} = 160\ \Omega$, the output signal voltage is 410 mV, which is very close to the desired value.

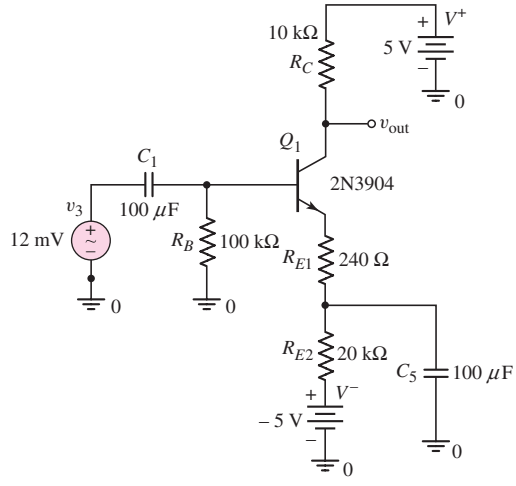


Figure 6.39 PSpice circuit schematic diagram for Example 6.8

Design Pointer: Approximation techniques are extremely useful in an initial electronic circuit design. A computer simulation, such as PSpice, can then be used to verify the design. Slight changes in the design can then be made to meet the required specifications.

EXERCISE PROBLEM

Ex 6.8: For the circuit in Figure 6.40, let $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 100$ V. (a) Determine the small-signal voltage gain. (b) Determine the input resistance seen by the signal source and the output resistance looking back into the output terminal. (Ans. (a) $A_v = -148$ (b) $R_{\text{in}} = 6.09\,\text{k}\Omega$, $R_o = 9.58\,\text{k}\Omega$)

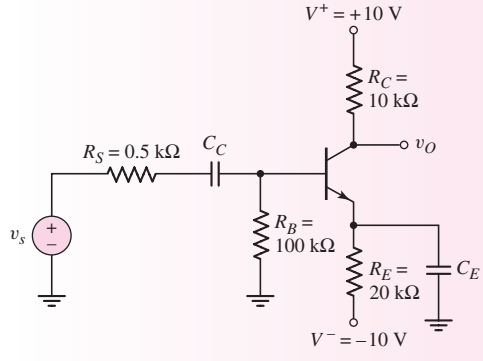


Figure 6.40 Figure for Exercise Ex6.8

Test Your Understanding

TYU 6.7 For the circuit in Figure 6.41, let $\beta = 125$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 200$ V. (a) Determine the small-signal voltage gain A_v. (b) Determine the output resistance R_o. (Ans. (a) $A_v = -50.5$ (b) $R_o = 2.28\,\text{k}\Omega$)

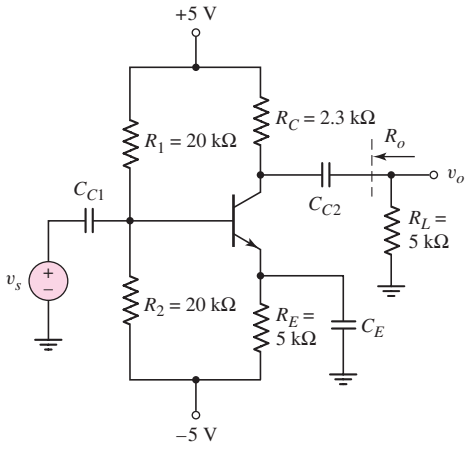


Figure 6.41 Figure for Exercise TYU6.7

COMPUTER ANALYSIS EXERCISE

PS 6.3: (a) Using a PSpice simulation, determine the voltage gain of the circuit shown in Figure 6.41. (b) Repeat Part (a) if $R_L = 50$ kΩ. What can be said about loading effects?

6.4.4 Advanced Common-Emitter Amplifier Concepts

Our previous analysis of common-emitter circuits assumed constant load or collector resistances. The common-emitter circuit shown in Figure 6.42(a) is biased with a constant-current source and contains a nonlinear, rather than a constant, collector resistor. Assume the current–voltage characteristics of the nonlinear resistor are described by the curve in Figure 6.42(b). The curve in Figure 6.42(b) can be generated using the pnp transistor as shown in Figure 6.42(c). The transistor is biased at a constant V_{EB} voltage. This transistor is now the load device and, since transistors are active devices, this load is referred to as an **active load.** We will encounter active loads in much more detail in Part 2 of the text.

Neglecting the base current in Figure 6.42(a), we can assume the quiescent current and voltage values of the load device are $I_Q = I_{CQ}$ and V_{RQ} as shown in Figure 6.42(b). At the Q-point of the load device, assume the incremental resistance $\Delta v_R / \Delta i_C$ is r_c.

The small-signal equivalent circuit of the common-emitter amplifier circuit in Figure 6.42(a) is shown in Figure 6.43. The collector resistor R_C is replaced by the small-signal equivalent resistance r_c that exists at the Q-point. The small-signal voltage gain is then, assuming an ideal voltage signal source,

$$A_v = \frac{V_o}{V_s} = -g_m(r_o \| r_c) \tag{6.60}$$

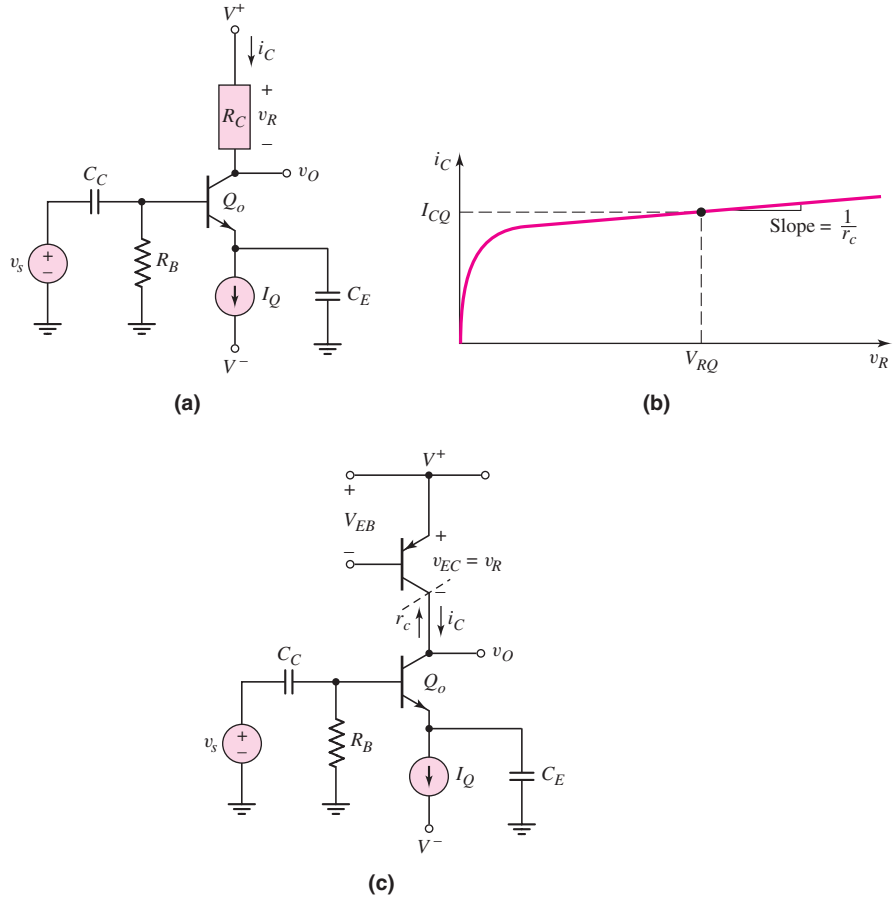


Figure 6.42 (a) A common-emitter circuit with current source biasing and a nonlinear load resistor, (b) current–voltage characteristics of the nonlinear load resistor, and (c) pnp transistor that can be used to generate the nonlinear load characteristics

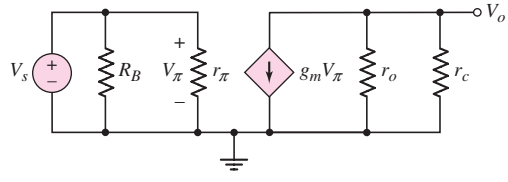


Figure 6.43 Small-signal equivalent circuit of the circuit in Figure 6.42(a)

EXAMPLE 6.9

Objective: Determine the small-signal voltage gain of a common-emitter circuit with a nonlinear load resistance.

Assume the circuit shown in Figure 6.42(a) is biased at $I_Q = 0.5$ mA, and the transistor parameters are $\beta = 120$ and $V_A = 80$ V. Also assume that nonlinear small-signal collector resistance is $r_c = 120\,\text{k}\Omega$.

Solution: For a transistor current gain of $\beta = 120$, $I_{CQ} \cong I_{EQ} = I_Q$, and the small-signal hybrid-π parameters are

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.5}{0.026} = 19.2 \text{ mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{80}{0.5} = 160\,\text{k}\Omega$$

The small-signal voltage gain is therefore

$$A_v = -g_m(r_o \| r_c) = -(19.2)(160 \| 120) = -1317$$

Comment: As we will see further in Part 2 of this text, the nonlinear resistor r_c is produced by the *I–V* characteristics of another bipolar transistor. Because the resulting effective load resistance is large, a very large small-signal voltage gain is produced. A large effective load resistance r_c means that the output resistance r_o of the amplifying transistor cannot be neglected; therefore, the loading effects must be taken into account.

EXERCISE PROBLEM

Ex 6.9: (a) Assume the circuit shown in Figure 6.42(a) is biased at $I_Q = 0.25$ mA and assume transistor parameters $\beta = 100$ and $V_A = 100$ V. Assume the small-signal nonlinear collector resistance is $r_c = 100\,\text{k}\Omega$. Determine the small-signal voltage gain. (b) Repeat part (a) assuming that a small-signal load resistance of $r_L = 100\,\text{k}\Omega$ is connected between the output terminal and ground. (Ans. (a) $A_v = -769$; (b) $A_v = -427$)

6.5 AC LOAD LINE ANALYSIS

Objective: • Understand the concept of the ac load line and calculate the maximum symmetrical swing of the output signal.

A dc load line gives us a way of visualizing the relationship between the *Q*-point and the transistor characteristics. When capacitors are included in a transistor circuit, a new effective load line, called an **ac load line,** may exist. The ac load line helps in visualizing the relationship between the small-signal response and the transistor characteristics. The ac operating region is on the ac load line.

6.5.1 AC Load Line

The circuit in Figure 6.38 has emitter resistors and an emitter bypass capacitor. The dc load line is found by writing a Kirchhoff voltage law (KVL) equation around the collector–emitter loop, as follows:

$$V^+ = I_C R_C + V_{CE} + I_E(R_{E1} + R_{E2}) + V^- \qquad \textbf{(6.61)}$$

Noting that $I_E = [(1+\beta)/\beta]I_C$, Equation (6.61) can be written as

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)(R_{E1} + R_{E2})\right] \tag{6.62}$$

which is the equation of the dc load line. For the parameters and standard resistor values found in Example 6.8, the dc load line and the Q-point are plotted in Figure 6.44. If $\beta \gg 1$, then we can approximate $(1+\beta)/\beta \cong 1$.

From the small-signal analysis in Example 6.8, the KVL equation around the collector–emitter loop is

$$i_c R_C + v_{ce} + i_e R_{E1} = 0 \tag{6.63(a)}$$

or, assuming $i_c \cong i_e$, then

$$v_{ce} = -i_c(R_C + R_{E1}) \tag{6.63(b)}$$

This equation is the ac load line. The slope is given by

$$\text{Slope} = \frac{-1}{R_C + R_{E1}}$$

The ac load line is shown in Figure 6.44. When $v_{ce} = i_c = 0$, we are at the Q-point. When ac signals are present, we deviate about the Q-point on the ac load line.

The slope of the ac load line differs from that of the dc load line because the emitter resistor is not included in the small-signal equivalent circuit. The small-signal C–E voltage and collector current response are functions of the resistor R_C and R_{E1} only.

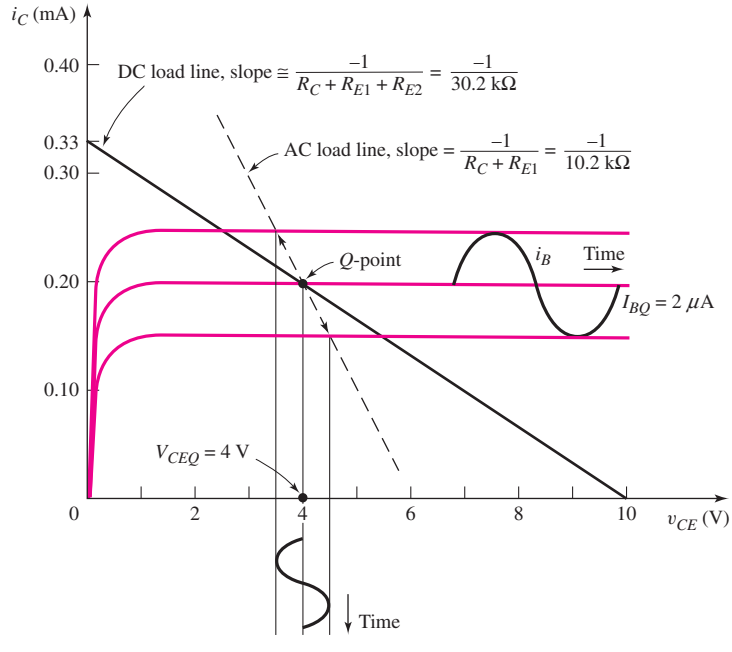


Figure 6.44 The dc and ac load lines for the circuit in Figure 6.38, and the signal responses to input signal

EXAMPLE 6.10

Objective: Determine the dc and ac load lines for the circuit shown in Figure 6.45. Assume the transistor parameters are: $V_{EB}(\text{on}) = 0.7\text{ V}$, $\beta = 150$, and $V_A = \infty$.

DC Solution: The dc load line is found by writing a KVL equation around the C–E loop, as follows:

$$V^+ = I_E R_E + V_{EC} + I_C R_C + V^-$$

The dc load line equation is then

$$V_{EC} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right]$$

Assuming that $(1+\beta)/\beta \cong 1$, the dc load line is plotted in Figure 6.46.

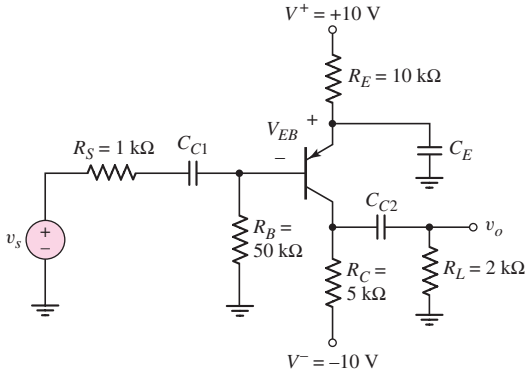


Figure 6.45 Circuit for Example 6.10

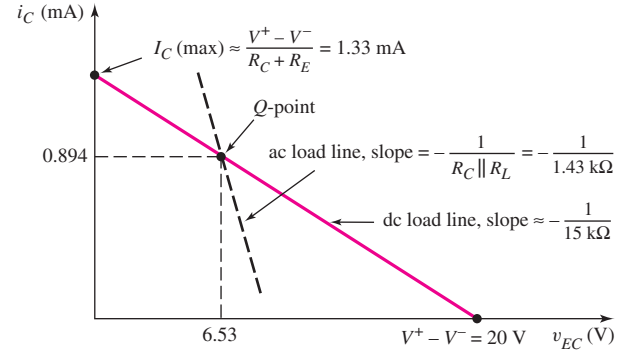


Figure 6.46 Plots of dc and ac load lines for Example 6.10

To determine the Q-point parameters, write a KVL equation around the B–E loop, as follows:

$$V^+ = (1+\beta)I_{BQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_B$$

or

$$I_{BQ} = \frac{V^+ - V_{EB}(\text{on})}{R_B + (1+\beta)R_E} = \frac{10 - 0.7}{50 + (151)(10)} \Rightarrow 5.96\,\mu\text{A}$$

Then,

$$I_{CQ} = \beta I_{BQ} = (150)(5.96\,\mu\text{A}) \Rightarrow 0.894\,\text{mA}$$
$$I_{EQ} = (1+\beta)I_{BQ} = (151)(5.96\,\mu\text{A}) \Rightarrow 0.90\,\text{mA}$$

and

$$V_{ECQ} = (V^+ - V^-) - I_{CQ}R_C - I_{EQ}R_E$$
$$= [10 - (-10)] - (0.894)(5) - (0.90)(10) = 6.53\,\text{V}$$

The Q-point is also plotted in Figure 6.46.

AC Solution: Assuming that all capacitors act as short circuits, the small-signal equivalent circuit is shown in Figure 6.47. Note that the current directions and

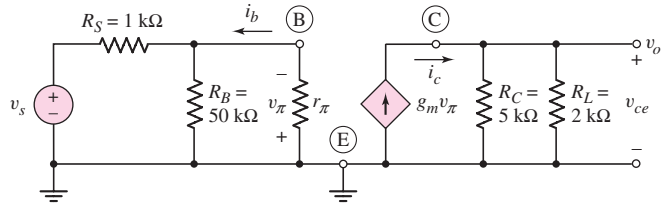


Figure 6.47 The small-signal equivalent circuit for Example 6.10

voltage polarities in the hybrid-π equivalent circuit of the pnp transistor are reversed compared to those of the npn device. The small-signal hybrid-π parameters are

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(150)}{0.894} = 4.36\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.894}{0.026} = 34.4\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{\infty}{I_{CQ}} = \infty$$

The small-signal output voltage, or C–E voltage, is

$$v_o = v_{ce} = +(g_m v_\pi)(R_C \| R_L)$$

where

$$g_m v_\pi = i_c$$

The ac load line, written in terms of the E–C voltage, is defined by

$$v_{ec} = -i_c(R_C \| R_L)$$

The ac load line is also plotted in Figure 6.46.

Comment: In the small-signal equivalent circuit, the large 10 kΩ emitter resistor is effectively shorted by the bypass capacitor C_E, the load resistor R_L is in parallel with R_C as a result of the coupling capacitor C_{C2}, so that the slope of the ac load line is substantially different than that of the dc load line.

EXERCISE PROBLEM

Ex 6.10: For the circuit in Figure 6.41, let $\beta = 125$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 200$ V. Plot the dc and ac load lines on the same graph. (Ans. $I_{CQ} = 0.840$ mA, dc load line, $V_{CE} = 10 - I_C(7.3)$; ac load line, $V_{ce} = -I_c(1.58)$)

6.5.2 Maximum Symmetrical Swing

When symmetrical sinusoidal signals are applied to the input of an amplifier, symmetrical sinusoidal signals are generated at the output, as long as the amplifier operation remains linear. We can use the ac load line to determine the **maximum output symmetrical swing.** If the output exceeds this limit, a portion of the output signal will be clipped and signal distortion will occur.

EXAMPLE 6.11

Objective: Determine the maximum symmetrical swing in the output voltage of the circuit given in Figure 6.45.

Solution: The ac load line is given in Figure 6.46. The maximum negative swing in the collector current is from 0.894 mA to zero; therefore, the maximum possible symmetrical peak-to-peak ac collector current is

$$\Delta i_c = 2(0.894) = 1.79\,\text{mA}$$

The maximum symmetrical peak-to-peak output voltage is given by

$$|\Delta v_{ec}| = |\Delta i_c|(R_C \| R_L) = (1.79)(5\|2) = 2.56\,\text{V}$$

Therefore, the maximum instantaneous collector current is

$$i_C = I_{CQ} + \tfrac{1}{2}|\Delta i_c| = 0.894 + 0.894 = 1.79\,\text{mA}$$

Comment: Considering the Q-point and the maximum swing in the C–E voltage, the transistor remains biased in the forward-active region. Note that the maximum instantaneous collector current, 1.79 mA, is larger than the maximum dc collector current, 1.33 mA, as determined from the dc load line. This apparent anomaly is due to the different resistance in the C–E circuit for the ac signal and the dc signal.

EXERCISE PROBLEM

Ex 6.11: Reconsider the circuit in Figure 6.36. Let $r_o = \infty$, $\beta = 120$, and $V_{EB}(\text{on}) = 0.7$ V. (a) Plot the dc and ac load lines on the same graph. (b) Determine the maximum symmetrical swing in the output voltage, for $i_c > 0$ and $0.5 \le v_{EC} \le 12$ V. (Ans. (b) 6.58 V peak-to-peak)

Note: In considering Figure 6.44, it appears that the ac output signal is smaller for the ac load line compared to the dc load line. This is true for a given sinusoidal input base current. However, the required input signal voltage v_s is substantially smaller for the ac load line to generate the given ac base current. This means the voltage gain for the ac load line is larger than that for the dc load line.

Problem-Solving Technique: Maximum Symmetrical Swing

Again, since we are dealing with linear amplifier circuits, superposition applies so that we can add the dc and ac analysis results. To design a BJT amplifier for maximum symmetrical swing, we perform the following steps.

1. Write the dc load line equation that relates the quiescent values I_{CQ} and V_{CEQ}.
2. Write the ac load line equation that relates the ac values i_c and v_{ce} : $v_{ce} = -i_c R_{eq}$ where R_{eq} is the effective ac resistance in the collector–emitter circuit.
3. In general, we can write $i_c = I_{CQ} - I_C(\text{min})$, where $I_C(\text{min})$ is zero or some other specified minimum collector current.
4. In general, we can write $v_{ce} = V_{CEQ} - V_{CE}(\text{min})$, where $V_{CE}(\text{min})$ is some specified minimum collector-emitter voltage.
5. The above four equations can be combined to yield the optimum I_{CQ} and V_{CEQ} values to obtain the maximum symmetrical swing in the output signal.

DESIGN EXAMPLE 6.12

Objective: Design a circuit to achieve a maximum symmetrical swing in the output voltage.

Specifications: The circuit configuration to be designed is shown in Figure 6.48a. The circuit is to be designed to be bias stable. The minimum collector current is to be $I_C(\text{min}) = 0.1$ mA and the minimum collector-emitter voltage is to be $V_{CE}(\text{min}) = 1$ V.

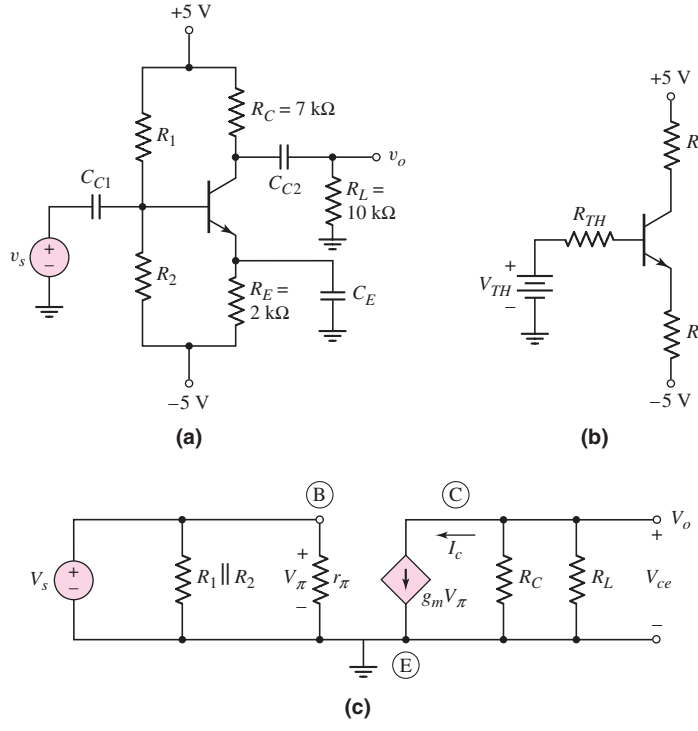


Figure 6.48 (a) Circuit for Example 6.12, (b) Thevenin equivalent circuit, and (c) small-signal equivalent circuit

Choices: Assume nominal resistance values of $R_E = 2\,\text{k}\Omega$ and $R_C = 7\,\text{k}\Omega$. Let $R_{TH} = R_1 \| R_2 = (0.1)(1+\beta)R_E = 24.2\,\text{k}\Omega$. Assume transistor parameters of $\beta = 120$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$.

Solution (Q-Point): The dc equivalent circuit is shown in Figure 6.48(b) and the midband small-signal equivalent circuit is shown in Figure 6.48(c).

The dc load line, from Figure 6.48(b), is (assuming $I_C \cong I_E$)

$$V_{CE} = 10 - I_C(R_C + R_E) = 10 - I_C(9)$$

The ac load line, from Figure 6.48(c), is

$$V_{ce} = -I_c(R_C \| R_L) = -I_c(4.12)$$

These two load lines are plotted in Figure 6.49. At this point, the Q-point is unknown. Also shown in the figure are the $I_C(\text{min})$ and $V_{CE}(\text{min})$ values. The peak value of the ac collector current is ΔI_C and the peak value of the ac collector–emitter voltage is ΔV_{CE}.

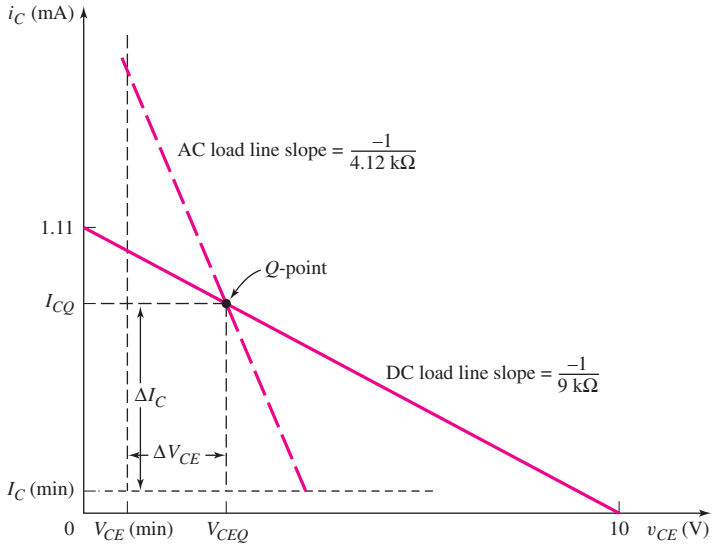


Figure 6.49 The ac and dc load lines to find the maximum symmetrical swing for the circuit shown in Figure 6.48(a) used in Example 6.12

We can write

$$\Delta I_C = I_{CQ} - I_C(\text{min}) = I_{CQ} - 0.1$$

and

$$\Delta V_{CE} = V_{CEQ} - V_{CE}(\text{min}) = V_{CEQ} - 1$$

where $I_C(\text{min})$ and $V_{CE}(\text{min})$ were given in the specifications.

Now

$$\Delta V_{CE} = \Delta I_C(R_C \| R_L)$$

or

$$V_{CEQ} - 1 = (I_{CQ} - 0.1)(4.12)$$

Substituting the expression for the dc load line, we obtain

$$10 - I_{CQ}(9) - 1 = (I_{CQ} - 0.1)(4.12)$$

which yields

$$I_{CQ} = 0.717\,\text{mA}$$

and then

$$V_{CEQ} = 3.54\,\text{V}$$

Solution (Bias Resistors): We can now determine R_1 and R_2 to produce the desired Q-point.

From the dc equivalent circuit, we have

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)[5 - (-5)] - 5$$

$$= \frac{1}{R_1}(R_{TH})(10) - 5 = \frac{1}{R_1}(24.2)(10) - 5$$

Then, from a KVL equation around the B–E loop, we obtain

$$V_{TH} = \left(\frac{I_{CQ}}{\beta}\right) R_{TH} + V_{BE}(\text{on}) + \left(\frac{1+\beta}{\beta}\right) I_{CQ} R_E - 5$$

or

$$\frac{1}{R_1}(24.2)(10) - 5 = \left(\frac{0.717}{120}\right)(24.2) + 0.7 + \left(\frac{121}{120}\right)(0.717)(2) - 5$$

which yields

$$R_1 = 106\,\text{k}\Omega$$

We then find

$$R_2 = 31.4\,\text{k}\Omega$$

Symmetrical Swing Results: We then find that the peak ac collector current is $\Delta I_C = 0.617$ mA, or the peak-to-peak ac collector current is 1.234 mA. The peak ac collect-emitter voltage is 2.54 V, or the peak-to-peak ac collector-emitter voltage is 5.08 V.

Trade-offs: We will investigate the effects of variations in the resistor values of R_E and R_C. In this example, we will assume that the bias resistor values of R_1 and R_2 are fixed, and will assume that the transistor parameters are fixed.

The Thevenin equivalent resistance is $R_{TH} = R_1 \| R_2 = 24.2\,\text{k}\Omega$ and the Thevenin equivalent voltage is $V_{TH} = -2.715$ V. The KVL equation around the B–E loop yields

$$I_{BQ} = \frac{-2.715 - 0.7 - (-5)}{24.2 + (121)R_E} = \frac{1.585}{24.2 + (121)R_E}$$

We have

$$I_{CQ} = (120) I_{BQ}$$

and

$$V_{CEQ} = 10 - I_{CQ}(R_C + R_E)$$

A standard resistor value of 7 kΩ is not available for R_C, so we will pick a value of 6.8 kΩ. For ±10% resistor tolerances, the range of values for R_E is between 1.8 and 2.2 kΩ and the range of values for R_C is between 6.12 and 7.48 kΩ. The Q-point values for the limiting resistor values are shown in the following table and are plotted on the various load lines in Figure 6.50.

	R_E	
R_C	1.8 kΩ	2.2 kΩ
6.12 kΩ	$I_{CQ} = 0.786$ mA	$I_{CQ} = 0.655$ mA
	$V_{CEQ} = 3.77$ V	$V_{CEQ} = 4.55$ V
7.48 kΩ	$I_{CQ} = 0.786$ mA	$I_{CQ} = 0.655$ mA
	$V_{CEQ} = 2.71$ V	$V_{CEQ} = 3.66$ V

Noting that the ac load line is given by $V_{ce} = -I_c(R_C \| R_L)$, we can find the maximum peak-to-peak values of a symmetrical output signal for the various limiting

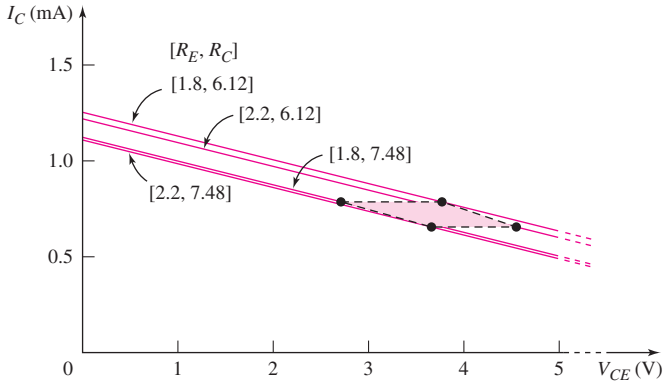


Figure 6.50 Load lines and Q-points for the limiting values of R_E and R_C for Design Example 6.12

resistor values. The limiting values are determined from $I_{CQ} - I_C(\text{min})$ or from $V_{CEQ} - V_{CE}(\text{min})$. The maximum peak-to-peak values are given in the following table.

	R_E	
R_C	**1.8 kΩ**	**2.2 kΩ**
6.12 kΩ	$\Delta I_C = 1.37\,\text{mA}$	$\Delta I_C = 1.11\,\text{mA}$
	$\Delta V_{CE} = 5.22\,\text{V}$	$\Delta V_{CE} = 4.22\,\text{V}$
7.48 kΩ	$\Delta I_C = 0.80\,\text{mA}$	$\Delta I_C = 1.11\,\text{mA}$
	$\Delta V_{CE} = 3.42\,\text{V}$	$\Delta V_{CE} = 4.76\,\text{V}$

The limiting factor for the case of $R_E = 1.8\,\text{k}\Omega$ and $R_C = 7.48\,\text{k}\Omega$ is determined by the maximum swing in the output voltage, $V_{CEQ} - V_{CE}(\text{min})$, whereas the limiting factor for the other cases is determined by the maximum swing in the output collector current, $I_{CQ} - I_C(\text{min})$.

Design Pointer: For this design, then, in the worst case, the maximum peak-to-peak output voltage would be limited to $\Delta V_{CE} = 3.42$ V rather than the ideal designed value of $\Delta V_{CE} = 5.08$ V. Choosing a smaller resistor value for R_C so that the minimum possible value of V_{CEQ} is approximately 3.5 V will allow for a larger output voltage swing.

Comment: To begin to understand trade-offs in a particular design, the tolerances in the R_E and R_C resistors were considered in this design example. Other resistors in the circuit have tolerances in their values and the current gain of the transistor has a range of values. These effects must also be considered in the final design.

EXERCISE PROBLEM

Ex 6.12: For the circuit shown in Figure 6.51, let $\beta = 120$, $V_{EB}(\text{on}) = 0.7$ V, and $r_o = \infty$. (a) Design a bias-stable circuit such that $I_{CQ} = 1.6$ mA. Determine V_{ECQ}. (b) Determine the value of R_L that will produce the maximum symmetrical swing in the output voltage and collector current for $i_C \geq 0.1$ mA and $0.5 \leq v_{EC} \leq 11.5$ V. (Ans. (a) $R_1 = 15.24\,\text{k}\Omega$, $R_2 = 58.7\,\text{k}\Omega$, $V_{ECQ} = 3.99$ V (b) $R_L = 5.56\,\text{k}\Omega$)

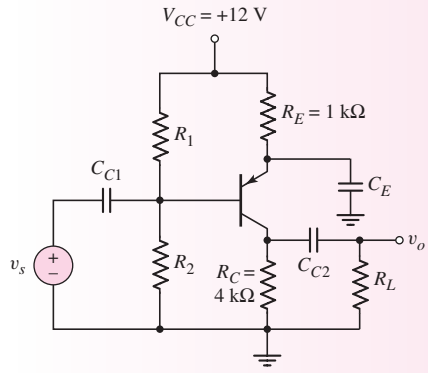


Figure 6.51 Figure for Exercise Ex6.12

Test Your Understanding

TYU 6.8 For the circuit in Figure 6.33, use the parameters given in Exercise Ex6.6. If the total instantaneous current must always be greater than 0.1 mA and the total instantaneous C–E voltage must be in the range $0.5 \leq v_{CE} \leq 5$ V, determine the maximum symmetrical swing in the output voltage. (Ans. 3.82 V peak-to-peak)

TYU 6.9 For the circuit in Figure 6.40, assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. Determine a new value of R_E that will achieve a maximum symmetrical swing in the output voltage, for $i_C > 0$ and $0.7 \leq v_{CE} \leq 19.5$ V. What is the maximum symmetrical swing that can be achieved? (Ans. $R_E = 16.4$ kΩ, 10.6 V peak-to-peak)

6.6 COMMON-COLLECTOR (EMITTER-FOLLOWER) AMPLIFIER

Objective: • Analyze the emitter-follower amplifier and become familiar with the general characteristics of this circuit.

The second type of transistor amplifier to be considered is the **common-collector circuit.** An example of this circuit configuration is shown in Figure 6.52. As seen in the figure, the output signal is taken off of the emitter with respect to ground and the collector is connected directly to V_{CC}. Since V_{CC} is at signal ground in the ac equivalent circuit, we have the name common-collector. The more common name for this circuit is **emitter follower.** The reason for this name will become apparent as we proceed through the analysis.

6.6.1 Small-Signal Voltage Gain

The dc analysis of the circuit is exactly the same as we have already seen, so we will concentrate on the small-signal analysis. The hybrid-π model of the bipolar transistor can also be used in the small-signal analysis of this circuit. Assuming the coupling

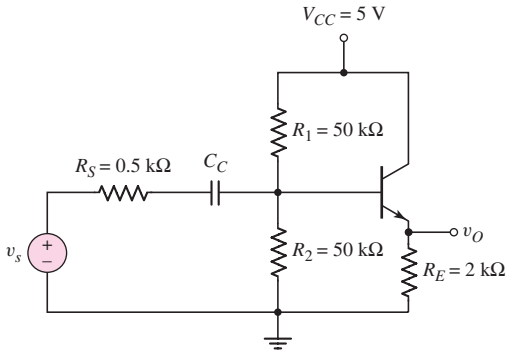


Figure 6.52 Emitter-follower circuit. Output signal is at the emitter terminal with respect to ground.

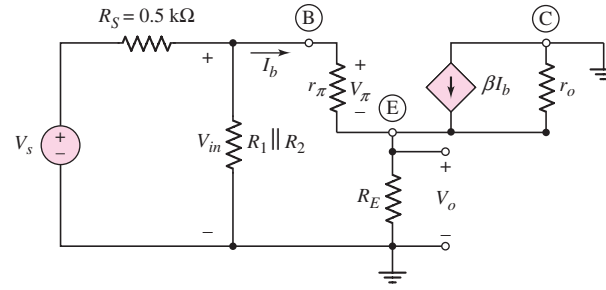


Figure 6.53 Small-signal equivalent circuit of the emitter-follower

capacitor C_C acts as a short circuit, Figure 6.53 shows the small-signal equivalent circuit of the circuit shown in Figure 6.52. The collector terminal is at signal ground and the transistor output resistance r_o is in parallel with the dependent current source.

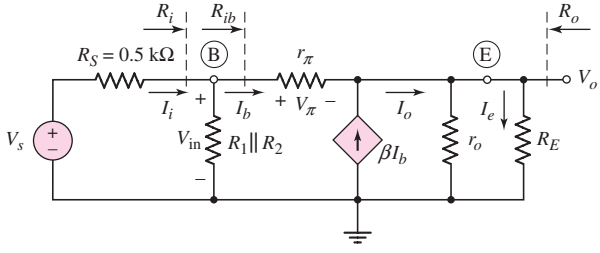


Figure 6.54 Small-signal equivalent circuit of the emitter-follower with all signal grounds connected together

Figure 6.54 shows the equivalent circuit rearranged so that all signal grounds are at the same point.

We see that

$$I_o = (1 + \beta) I_b \tag{6.64}$$

so the output voltage can be written as

$$V_o = I_b (1 + \beta)(r_o \| R_E) \tag{6.65}$$

Writing a KVL equation around the base-emitter loop, we obtain

$$V_{\text{in}} = I_b [r_\pi + (1 + \beta)(r_o \| R_E)] \tag{6.66(a)}$$

or

$$R_{ib} = \frac{V_{\text{in}}}{I_b} = r_\pi + (1 + \beta)(r_o \| R_E) \tag{6.66(b)}$$

We can also write

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_S} \right) \cdot V_s \tag{6.67}$$

where $R_i = R_1 \| R_2 \| R_{ib}$.

Combining Equations (6.65), (6.66(b)), and (6.67), the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = \frac{(1+\beta)(r_o \| R_E)}{r_\pi + (1+\beta)(r_o \| R_E)} \cdot \left(\frac{R_i}{R_i + R_S}\right) \tag{6.68}$$

EXAMPLE 6.13

Objective: Calculate the small-signal voltage gain of an emitter-follower circuit.

For the circuit shown in Figure 6.52, assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 80$ V.

Solution: The dc analysis shows that $I_{CQ} = 0.793$ mA and $V_{CEQ} = 3.4$ V. The small-signal hybrid-π parameters are determined to be

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{0.793} = 3.28\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.793}{0.026} = 30.5\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{80}{0.793} \cong 100\,\text{k}\Omega$$

We may note that

$$R_{ib} = 3.28 + (101)(100 \| 2) = 201\,\text{k}\Omega$$

and

$$R_i = 50 \| 50 \| 201 = 22.2\,\text{k}\Omega$$

The small-signal voltage gain is then

$$A_v = \frac{(101)(100 \| 2)}{3.28 + (101)(100 \| 2)} \cdot \left(\frac{22.2}{22.2 + 0.5}\right)$$

or

$$A_v = +0.962$$

Comment: The magnitude of the voltage gain is slightly less than 1. An examination of Equation (6.68) shows that this is always true. Also, the voltage gain is positive, which means that the output signal voltage at the emitter is in phase with the input signal voltage. The reason for the terminology emitter-follower is now clear. The output voltage at the emitter is essentially equal to the input voltage.

At first glance, a transistor amplifier with a voltage gain essentially of 1 may not seem to be of much value. However, the input and output resistance characteristics make this circuit extremely useful in many applications, as we will show in the next section.

EXERCISE PROBLEM

Ex 6.13: For the circuit shown in Figure 6.52, let $V_{CC} = 5$ V, $\beta = 120$, $V_A = 100$ V, $R_E = 1\,\text{k}\Omega$, $V_{BE}(\text{on}) = 0.7$ V, $R_1 = 25\,\text{k}\Omega$, and $R_2 = 50\,\text{k}\Omega$. (a) Determine the small-signal voltage gain $A_v = V_o/V_s$. (b) Find the input resistance looking into the base of the transistor. (Ans. (a) $A_v = 0.956$ (b) $R_{ib} = 120\,\text{k}\Omega$)

COMPUTER ANALYSIS EXERCISE

PS6.4: Perform a PSpice simulation on the circuit in Figure 6.52. (a) Determine the small-signal voltage gain and (b) find the effective resistance seen by the signal source v_s.

6.6.2 Input and Output Impedance

Input Resistance

The input impedance, or small-signal input resistance for low-frequency signals, of the emitter-follower is determined in the same manner as for the common-emitter circuit. For the circuit in Figure 6.52, the input resistance looking into the base is denoted R_{ib} and is indicated in the small-signal equivalent circuit shown in Figure 6.54.

The input resistance R_{ib} was given by Equation (6.66(b)) as

$$R_{ib} = r_\pi + (1+\beta)(r_o \| R_E)$$

Since the emitter current is $(1+\beta)$ times the base current, the effective impedance in the emitter is multiplied by $(1+\beta)$. We saw this same effect when an emitter resistor was included in a common-emitter circuit. This multiplication by $(1+\beta)$ is again called the **resistance reflection rule.** The input resistance at the base is r_π plus the effective resistance in the emitter multiplied by the $(1+\beta)$ factor. This resistance reflection rule will be used extensively throughout the remainder of the text.

Output Resistance

Initially, to find the output resistance of the emitter-follower circuit shown in Figure 6.52, we will assume that the input signal source is ideal and that $R_S = 0$. The circuit shown in Figure 6.55 can be used to determine the output resistance looking back into the output terminals. The circuit is derived from the small-signal equivalent circuit shown in Figure 6.54 by setting the independent voltage source V_s equal to zero, which means that V_s acts as a short circuit. A test voltage V_x is applied to the output terminal and the resulting test current is I_x. The output resistance, R_o, is given by

$$R_o = \frac{V_x}{I_x} \tag{6.69}$$

In this case, the control voltage V_π is not zero, but is a function of the applied test voltage. From Figure 6.55, we see that $V_\pi = -V_x$. Summing currents at the output node, we have

$$I_x + g_m V_\pi = \frac{V_x}{R_E} + \frac{V_x}{r_o} + \frac{V_x}{r_\pi} \tag{6.70}$$

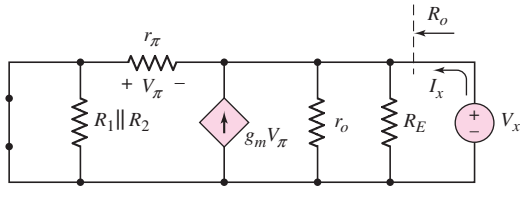


Figure 6.55 Small-signal equivalent circuit of the emitter-follower used to determine the output resistance. The source resistance R_S is assumed to be zero (an ideal signal source).

Since $V_\pi = -V_x$, Equation (6.70) can be written as

$$\frac{I_x}{V_x} = \frac{1}{R_o} = g_m + \frac{1}{R_E} + \frac{1}{r_o} + \frac{1}{r_\pi} \tag{6.71}$$

or the output resistance is given by

$$R_o = \frac{1}{g_m} \| R_E \| r_o \| r_\pi \tag{6.72}$$

The output resistance may also be written in a slightly different form. Equation (6.71) can be written in the form

$$\frac{1}{R_o} = \left(g_m + \frac{1}{r_\pi}\right) + \frac{1}{R_E} + \frac{1}{r_o} = \left(\frac{1+\beta}{r_\pi}\right) + \frac{1}{R_E} + \frac{1}{r_o} \tag{6.73}$$

or the output resistance can be written in the form

$$R_o = \frac{r_\pi}{1+\beta} \| R_E \| r_o \tag{6.74}$$

Equation (6.74) says that the output resistance looking back into the output terminals is the effective resistance in the emitter, $R_E \| r_o$, in parallel with the resistance looking back into the emitter. In turn, the resistance looking into the emitter is the total resistance in the base circuit divided by $(1 + \beta)$. This is an important result and is called the **inverse resistance reflection rule** and is the inverse of the reflection rule looking to the base.

EXAMPLE 6.14

Objective: Calculate the input and output resistance of the emitter-follower circuit shown in Figure 6.52. Assume $R_S = 0$.

The small-signal parameters, as determined in Example 6.13, are $r_\pi = 3.28\,\text{k}\Omega$, $\beta = 100$, and $r_o = 100\,\text{k}\Omega$.

Solution (Input Resistance): The input resistance looking into the base was determined in Example 6.13 as

$$R_{ib} = r_\pi + (1+\beta)(r_o \| R_E) = 3.28 + (101)(100 \| 2) = 201\ \text{k}\Omega$$

and the input resistance seen by the signal source R_i is

$$R_i = R_1 \| R_2 \| R_{ib} = 50 \| 50 \| 201 = 22.2\ \text{k}\Omega$$

Comment: The input resistance of the emitter-follower looking into the base is substantially larger than that of the simple common-emitter circuit because of the $(1 + \beta)$ factor. This is one advantage of the emitter-follower circuit. However, in this case, the input resistance seen by the signal source is dominated by the bias resistors R_1 and R_2. To take advantage of the large input resistance of the emitter-follower circuit, the bias resistors must be designed to be much larger.

Solution (Output Resistance): The output resistance is found from Equation (6.74) as

$$R_o = \left(\frac{r_\pi}{1+\beta}\right) \| R_E \| r_o = \left(\frac{3.28}{101}\right) \| 2 \| 100$$

or

$$R_o = 0.0325 \| 2 \| 100 = 0.0320\ \text{k}\Omega \Rightarrow 32.0\ \Omega$$

The output resistance is dominated by the first term that has $(1+\beta)$ in the denominator.

Comment: The emitter-follower circuit is sometimes referred to as an **impedance transformer,** since the input impedance is large and the output impedance is small. The very low output resistance makes the *emitter-follower act almost like an ideal voltage source,* so the output is not loaded down when used to drive another load. Because of this, the emitter-follower is often used as the output stage of a multistage amplifier.

EXERCISE PROBLEM

EX 6.14: Consider the circuit and transistor parameters described in Exercise Ex6.13 for the circuit shown in Figure 6.52. For the case of $R_S = 0$, determine the output resistance looking into the output terminals. (Ans. 11.1 Ω)

We can determine the output resistance of the emitter-follower circuit taking into account a nonzero source resistance. The circuit in Figure 6.56 is derived from the small-signal equivalent circuit shown in Figure 6.54 and can be used to find R_o. The independent source V_s is set equal to zero and a test voltage V_x is applied to the output terminals. Again, the control voltage V_π is not zero, but is a function of the test voltage. Summing currents at the output node, we have

$$I_x + g_m V_\pi = \frac{V_x}{R_E} + \frac{V_x}{r_o} + \frac{V_x}{r_\pi + R_1 \| R_2 \| R_S} \tag{6.75}$$

The control voltage can be written in terms of the test voltage by a voltage divider equation as

$$V_\pi = -\left(\frac{r_\pi}{r_\pi + R_1 \| R_2 \| R_S}\right) \cdot V_x \tag{6.76}$$

Equation (6.75) can then be written as

$$I_x = \left(\frac{g_m r_\pi}{r_\pi + R_1 \| R_2 \| R_S}\right) \cdot V_x + \frac{V_x}{R_E} + \frac{V_x}{r_o} + \frac{V_x}{r_\pi + R_1 \| R_2 \| R_S} \tag{6.77}$$

Noting that $g_m r_\pi = \beta$, we find

$$\frac{I_x}{V_x} = \frac{1}{R_o} = \frac{1+\beta}{r_\pi + R_1 \| R_2 \| R_S} + \frac{1}{R_E} + \frac{1}{r_o} \tag{6.78}$$

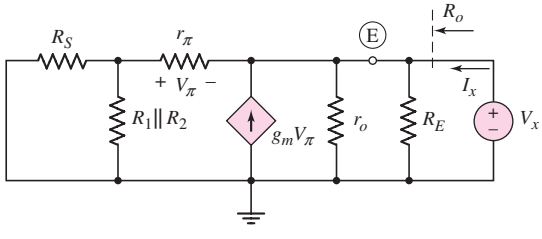


Figure 6.56 Small-signal equivalent circuit of the emitter-follower used to determine the output resistance including the effect of the source resistance R_S

or

$$R_o = \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{1+\beta}\right) \| R_E \| r_o \tag{6.79}$$

In this case, the source resistance and bias resistances contribute to the output resistance.

6.6.3 Small-Signal Current Gain

We can determine the small-signal current gain of an emitter-follower by using the input resistance and the concept of current dividers. For the small-signal emitter-follower equivalent circuit shown in Figure 6.54, the small signal current gain is defined as

$$A_i = \frac{I_e}{I_i} \tag{6.80}$$

where I_e and I_i are the output and input current phasors.

Using a current divider equation, we can write the base current in terms of the input current, as follows:

$$I_b = \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right) I_i \tag{6.81}$$

Since $g_m V_\pi = \beta I_b$, then,

$$I_o = (1+\beta) I_b = (1+\beta)\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right) I_i \tag{6.82}$$

Writing the load current in terms of I_o produces

$$I_e = \left(\frac{r_o}{r_o + R_E}\right) I_o \tag{6.83}$$

Combining Equations (6.82) and (6.83), we obtain the small-signal current gain, as follows:

$$A_i = \frac{I_e}{I_i} = (1+\beta)\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right)\left(\frac{r_o}{r_o + R_E}\right) \tag{6.84}$$

If we assume that $R_1 \| R_2 \gg R_{ib}$ and $r_o \gg R_E$, then

$$A_i \cong (1+\beta) \tag{6.85}$$

which is the current gain of the transistor.

Although the small-signal voltage gain of the emitter follower is slightly less than 1, the small-signal current gain is normally greater than 1. Therefore, the emitter-follower circuit produces a small-signal power gain.

Although we did not explicitly calculate a current gain in the common-emitter circuit previously, the analysis is the same as that for the emitter-follower and in general the current gain is also greater than unity.

DESIGN EXAMPLE 6.15

Objective: To design an emitter-follower amplifier to meet an output resistance specification.

Specifications: Consider the output signal of the amplifier designed in Example 6.8. We now want to design an emitter-follower circuit with the configuration shown in Figure 6.57 such that the output signal from this circuit does not vary by more than 5 percent when a load in the range $R_L = 4\,\text{k}\Omega$ to $R_L = 20\,\text{k}\Omega$ is connected to the output.

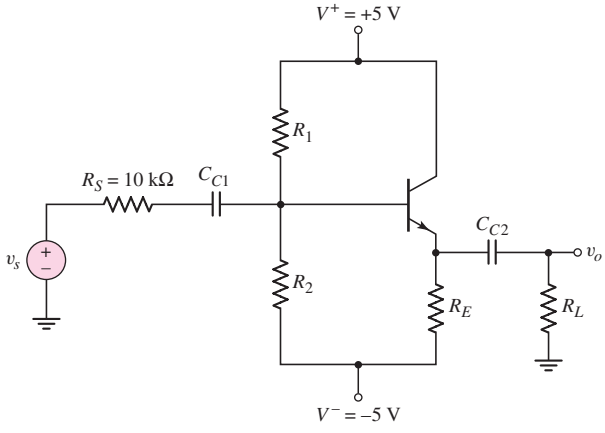


Figure 6.57 Figure for Example 6.15

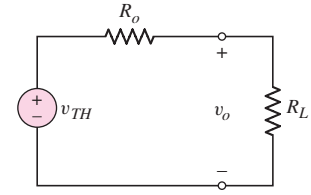


Figure 6.58 Thevenin equivalent of the output of an amplifier

Choices: We will assume that a transistor with nominal parameter values of $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 80$ V is available.

Discussion: The output resistance of the common-emitter circuit designed in Example 6.8 is $R_o = R_C = 10\,\text{k}\Omega$. Connecting a load resistance between $4\,\text{k}\Omega$ and $20\,\text{k}\Omega$ will load down this circuit, so that the output voltage will change substantially. For this reason, an emitter-follower circuit with a low output resistance must be designed to minimize the loading effect. The Thevenin equivalent circuit is shown in Figure 6.58. The output voltage can be written as

$$v_o = \left(\frac{R_L}{R_L + R_o}\right) \cdot v_{TH}$$

where v_{TH} is the ideal voltage generated by the amplifier. In order to have v_o change by less than 5 percent as a load resistance R_L is added, we must have R_o less than or equal to approximately 5 percent of the minimum value of R_L. In this case, then, we need R_o to be approximately 200 Ω.

Initial Design Approach: Consider the emitter-follower circuit shown in Figure 6.57. Note that the source resistance is $R_S = 10\,\text{k}\Omega$, corresponding to the output resistance of the circuit designed in Example 6.8. Assume that $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 80$ V.

The output resistance, given by Equation (6.79), is

$$R_o = \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{1 + \beta}\right) \| R_E \| r_o$$

The first term, with $(1 + \beta)$ in the denominator, dominates, and if $R_1 \| R_2 \| R_S \cong R_S$, then we have

$$R_o \cong \frac{r_\pi + R_S}{1 + \beta}$$

For $R_o = 200\ \Omega$, we find

$$0.2 = \frac{r_\pi + 10}{101}$$

or $r_\pi = 10.2\ \text{k}\Omega$. Since $r_\pi = (\beta V_T)/I_{CQ}$, the quiescent collector current must be

$$I_{CQ} = \frac{\beta V_T}{r_\pi} = \frac{(100)(0.026)}{10.2} = 0.255\ \text{mA}$$

Assuming $I_{CQ} \cong I_{EQ}$ and letting $V_{CEQ} = 5$ V, we find

$$R_E = \frac{V^+ - V_{CEQ} - V^-}{I_{EQ}} = \frac{5 - 5 - (-5)}{0.255} = 19.6\ \text{k}\Omega$$

The term $(1 + \beta)R_E$ is

$$(1 + \beta)R_E = (101)(19.6) \Rightarrow 1.98\ \text{M}\Omega$$

With this large resistance, we can design a bias-stable circuit as defined in Chapter 3 and still have large values for bias resistances. Let

$$R_{TH} = (0.1)(1 + \beta)R_E = (0.1)(101)(19.6) = 198\ \text{k}\Omega$$

The base current is

$$I_B = \frac{V_{TH} - V_{BE}(\text{on}) - V^-}{R_{TH} + (1 + \beta)R_E}$$

where

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5 = \frac{1}{R_1}(R_{TH})(10) - 5$$

We can then write

$$\frac{0.255}{100} = \frac{\dfrac{1}{R_1}(198)(10) - 5 - 0.7 - (-5)}{198 + (101)(19.6)}$$

We find $R_1 = 317\,\text{k}\Omega$ and $R_2 = 527\,\text{k}\Omega$.

Comment: The quiescent collector current $I_{CQ} = 0.255$ mA establishes the required r_π value which in turn establishes the required output resistance R_o.

Trade-offs: We will investigate the effects of a variation in transistor current gain. In this example, we will assume that the designed resistor values are available.

The Thevenin equivalent resistance is $R_{TH} = R_1 \| R_2 = 198\,\text{k}\Omega$ and the Thevenin equivalent voltage is $V_{TH} = 1.244$ V. The base current is found by the KVL equation around the B–E loop. We find

$$I_{BQ} = \frac{1.244 - 0.7 - (-5)}{198 + (1 + \beta)(19.6)}$$

The collector current is $I_{CQ} = \beta I_{BQ}$ and we find $r_\pi = (\beta V_T)/I_{CQ}$. Finally, the output resistance is approximately

$$R_o \cong \frac{r_\pi + R_{TH} \| R_S}{1 + \beta} = \frac{r_\pi + 198 \| 10}{1 + \beta}$$

The values of these parameters for several values of β are shown in the following table.

β	I_{CQ} (mA)	r_π (kΩ)	R_o (Ω)
50	0.232	5.62	297
75	0.246	7.91	229
100	0.255	10.2	195
125	0.260	12.5	175

From these results, we see that the specified maximum output resistance of $R_o \cong 200\ \Omega$ is met only if the current gain of the transistor is at least $\beta = 100$. In this design, then, we must specify that the minimum current gain of a transistor is 100.

Computer Simulation: We again used approximation techniques in our design. For this reason, it is useful to verify our design with a PSpice analysis, since the computer simulation will take into account more details than our hand design.

Figure 6.59 shows the PSpice circuit schematic diagram. A 1 mV sinusoidal signal source is capacitively coupled to the output of the emitter follower. The input

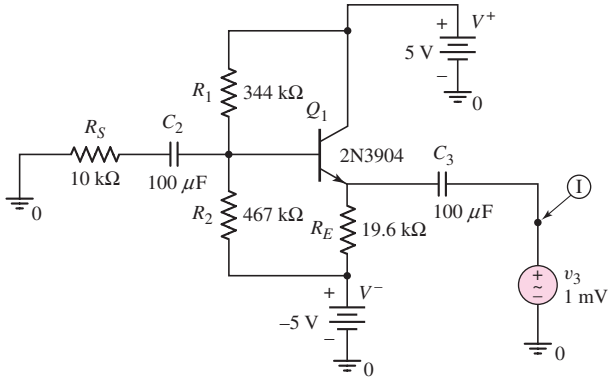


Figure 6.59 PSpice circuit schematic for Example 6.15

signal source has been set equal to zero. The current from the output signal source was found to be 5.667 μA. The output resistance of the emitter follower is then $R_o = 176\ \Omega$, which means that we have met our desired specification that the output resistance should be less than 200 Ω.

```
BJT MODEL PARAMETERS     **** BIPOLAR JUNCTION TRANSISTORS
     Q2N3904             NAME       Q_Q1
     NPN                 MODEL      Q2N3904
 IS   6.734000E-15       IB         2.08E-06
 BF 416.4                IC         2.39E-04
 NF   1                  VBE        6.27E-01
VAF  74.03               VBC       -4.65E+00
IKF    .06678            VCE        5.28E+00
ISE   6.734000E-15       BETADC     1.15E+02
 NE   1.259              GM         9.19E-03
 BR    .7371             RPI        1.47E+04
 NR   1                  RX         1.00E+01
 RB  10                  RO         3.30E+05
```

```
RBM   10                CBE       9.08E-12
 RC    1                CBC       1.98E-12
CJE    4.493000E-12     CJS       0.00E+00
MJE     .2593           BETAAC    1.35E+02
CJC    3.638000E-12     CBX       0.00E+00
MJC     .3085           FT        1.32E+08
 TF  301.200000E-12
XTF    2
VTF    4
ITF     .4
 TR  239.500000E-09
XTB    1.5
```

Discussion: The transistor Q-point values from the PSpice analysis are listed. From the computer simulation, the quiescent collector current is $I_{CQ} = 0.239$ mA compared to the designed value of $I_{CQ} = 0.255$ mA. The principal reason for the difference in value is the difference in base-emitter voltage and current gain between the hand analysis and computer simulation.

The output resistance specification is met in the computer simulation. In the PSpice analysis, the ac beta is 135 and the output resistance is $R_o = 176\,\Omega$. This value correlates very well with the hand analysis in which $R_o = 184\,\Omega$ for $\beta = 125$.

EXERCISE PROBLEM

Ex 6.15: For the circuit in Figure 6.57, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 125$ V. Assume $R_S = 0$ and $R_L = 1$ kΩ. (a) Design a bias-stable circuit such that $I_{CQ} = 125$ mA and $V_{CEQ} = 4$ V. (b) What is the small-signal current gain $A_i = i_o/i_i$? (c) What is the output resistance looking back into the output terminals? (Ans. (a) $R_E = 4.76$ kΩ, $R_1 = 65.8$ kΩ, $R_2 = 178.8$ kΩ; (b) $A_i = 29.9$, (c) $R_o = 20.5\,\Omega$)

Test Your Understanding

TYU 6.10 Assume the circuit in Figure 6.60 uses a 2N2222 transistor. Assume a nominal dc current gain of $\beta = 130$. Using the average h-parameter values (assume $h_{re} = 0$) given in the data sheets, determine $A_v = v_o/v_s$, $A_i = i_o/i_s$, R_{ib}, and R_o for $R_S = R_L = 10$ kΩ. (Ans. $A_v = 0.891$, $A_i = 8.59$, $R_{ib} = 641$ kΩ, $R_o = 96\,\Omega$)

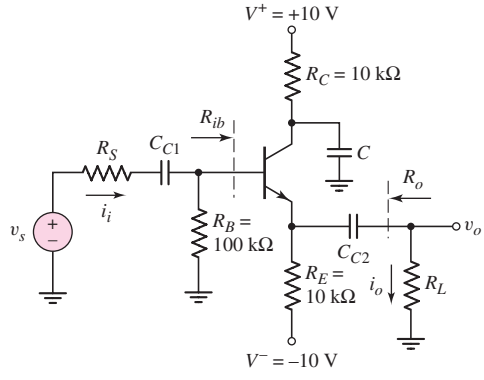


Figure 6.60 Figure for Exercise TYU6.10

TYU 6.11 For the circuit in Figure 6.61, $R_E = 2\,\text{k}\Omega$, $R_1 = R_2 = 50\,\text{k}\Omega$ and the transistor parameters are $\beta = 100$, $V_{EB}(\text{on}) = 0.7$ V, and $V_A = 125$ V. (a) Determine the small-signal voltage gain $A_v = v_o/v_s$. (b) Find the resistances R_{ib} and R_o. (Ans. (a) $A_v = 0.925$, (b) $R_{ib} = 4.37\,\text{k}\Omega$, $R_o = 32.0\ \Omega$)

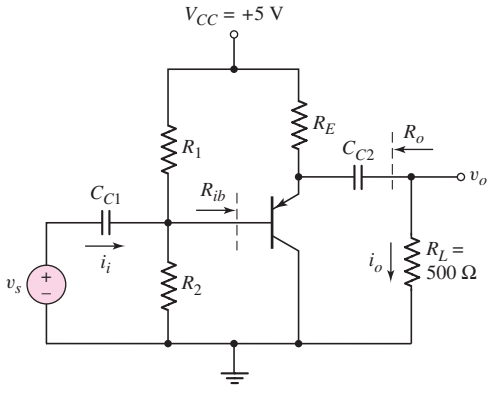


Figure 6.61 Figure for Exercises TYU6.11 and TYU6.12

TYU 6.12 For the circuit in Figure 6.61, the transistor parameters are $\beta = 75$, $V_{EB}(\text{on}) = 0.7$ V, and $V_A = 75$ V. The small-signal current gain is to be $A_i = i_o/i_i = 10$. Assume $V_{ECQ} = 2.5$ V. Determine the values of the elements required if $R_E = R_L$. (Ans. $R_1 = 26.0\,\text{k}\Omega$, $R_2 = 9.53\,\text{k}\Omega$)

COMPUTER ANALYSIS EXERCISE

PS 6.5: For the circuit in Figure 6.61, $R_E = 2\,\text{k}\Omega$ and $R_1 = R_2 = 50\,\text{k}\Omega$. Using a PSpice simulation, determine the small-signal voltage gain for (a) $R_L = 50\ \Omega$, (b) $R_L = 200\ \Omega$, (c) $R_L = 500\ \Omega$, and (d) $R_L = 2\,\text{k}\Omega$. What can be said about loading effects?

6.7 COMMON-BASE AMPLIFIER

Objective: • Analyze the common-base amplifier and become familiar with the general characteristics of this circuit.

A third amplifier circuit configuration is the **common-base circuit.** To determine the small-signal voltage and current gains, and the input and output impedances, we will use the same hybrid-π equivalent circuit for the transistor that was used previously. The dc analysis of the common-base circuit is essentially the same as for the common-emitter circuit.

6.7.1 Small-Signal Voltage and Current Gains

Figure 6.62 shows the basic common-base circuit, in which the base is at signal ground and the input signal is applied to the emitter. Assume a load is connected to the output through a coupling capacitor C_{C2}.

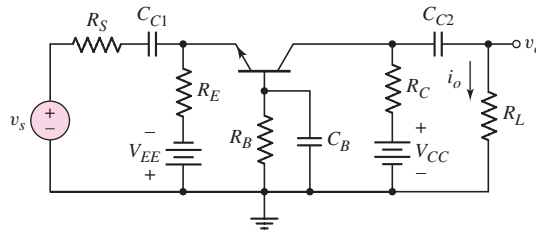


Figure 6.62 Basic common-base circuit. The input signal is applied to the emitter terminal and the output signal is measured at the collector terminal.

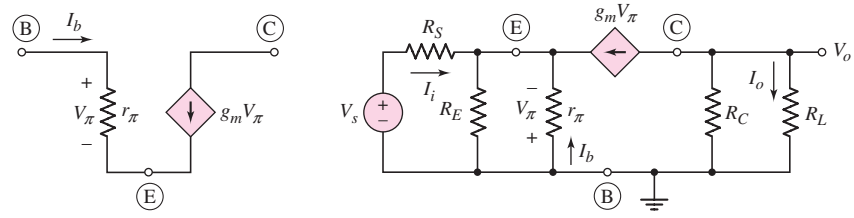


Figure 6.63 (a) Simplified hybrid-π model of the npn transistor and (b) small-signal equivalent circuit of the common-base circuit

Figure 6.63(a) again shows the hybrid-π model of the npn transistor, with the output resistance r_o assumed to be infinite. Figure 6.63(b) shows the small-signal equivalent circuit of the common-base circuit, including the hybrid-π model of the transistor. As a result of the common-base configuration, the hybrid-π model in the small-signal equivalent circuit may look a little strange.

The small signal output voltage is given by

$$V_o = -(g_m V_\pi)(R_C \| R_L) \tag{6.86}$$

Writing a KCL equation at the emitter node, we obtain

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_s - (-V_\pi)}{R_S} = 0 \tag{6.87}$$

Since $\beta = g_m r_\pi$, Equation (6.87) can be written

$$V_\pi \left(\frac{1+\beta}{r_\pi} + \frac{1}{R_E} + \frac{1}{R_S} \right) = -\frac{V_s}{R_S} \tag{6.88}$$

Then,

$$V_\pi = -\frac{V_s}{R_S} \left[\left(\frac{r_\pi}{1+\beta} \right) \| R_E \| R_S \right] \tag{6.89}$$

Substituting Equation (6.89) into (6.86), we find the small-signal voltage gain, as follows:

$$A_v = \frac{V_o}{V_s} = +g_m \left(R_C \| R_L \right) \left[\left(\frac{r_\pi}{1+\beta} \right) \| R_E \| R_S \right] \tag{6.90}$$

We can show that as R_S approaches zero, the small-signal voltage gain becomes

$$A_v = g_m (R_C \| R_L) \tag{6.91}$$

Figure 6.63(b) can also be used to determine the small-signal current gain. The current gain is defined as $A_i = I_o/I_i$. Writing a KCL equation at the emitter node, we have

$$I_i + \frac{V_\pi}{r_\pi} + g_m V_\pi + \frac{V_\pi}{R_E} = 0 \tag{6.92}$$

Solving for V_π, we obtain

$$V_\pi = -I_i \left[\left(\frac{r_\pi}{1+\beta} \right) \Big\| R_E \right] \tag{6.93}$$

The load current is given by

$$I_o = -(g_m V_\pi) \left(\frac{R_C}{R_C + R_L} \right) \tag{6.94}$$

Combining Equations (6.93) and (6.94), we obtain an expression for the small-signal current gain, as follows:

$$A_i = \frac{I_o}{I_i} = g_m \left(\frac{R_C}{R_C + R_L} \right) \left[\left(\frac{r_\pi}{1+\beta} \right) \Big\| R_E \right] \tag{6.95}$$

If we take the limit as R_E approaches infinity and R_L approaches zero, then the current gain becomes the short-circuit current gain given by

$$A_{io} = \frac{g_m r_\pi}{1+\beta} = \frac{\beta}{1+\beta} = \alpha \tag{6.96}$$

where α is the common-base current gain of the transistor.

Equations (6.90) and (6.96) indicate that, for the common-base circuit, the small-signal voltage gain is usually greater than 1 and the small-signal current gain is slightly less than 1. However, we still have a small-signal power gain. The applications of a common-base circuit take advantage of the input and output resistance characteristics.

6.7.2 Input and Output Impedance

Figure 6.64 shows the small-signal equivalent circuit of the common-base configuration looking into the emitter. In this circuit, for convenience only, we have reversed the polarity of the control voltage, which reverses the direction of the dependent current source.

The input resistance looking into the emitter is defined as

$$R_{ie} = \frac{V_\pi}{I_i} \tag{6.97}$$

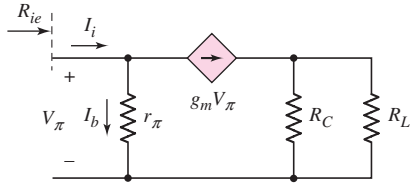


Figure 6.64 Common-base equivalent circuit for input resistance calculations

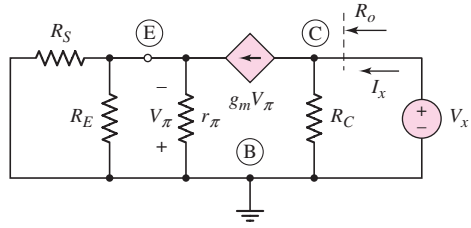


Figure 6.65 Common-base equivalent circuit for output resistance calculations

If we write a KCL equation at the input, we obtain

$$I_i = I_b + g_m V_\pi = \frac{V_\pi}{r_\pi} + g_m V_\pi = V_\pi \left(\frac{1+\beta}{r_\pi} \right) \tag{6.98}$$

Therefore,

$$R_{ie} = \frac{V_\pi}{I_i} = \frac{r_\pi}{1+\beta} \equiv r_e \tag{6.99}$$

The resistance looking into the emitter, with the base grounded, is usually defined as r_e and is quite small, as already shown in the analysis of the emitter-follower circuit. When the input signal is a current source, a small input resistance is desirable.

Figure 6.65 shows the circuit used to calculate the output resistance. The independent source v_s has been set equal to zero. Writing a KCL equation at the emitter, we find

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_\pi}{R_S} = 0 \tag{6.100}$$

This implies that $V_\pi = 0$, which means that the independent source $g_m V_\pi$ is also zero. Consequently, the output resistance looking back into the output terminals is then

$$R_o = R_C \tag{6.101}$$

Because we have assumed r_o is infinite, the output resistance looking back into the collector terminal is essentially infinite, which means that the common-base circuit looks almost like an ideal current source. The circuit is also referred to as a **current buffer.**

Discussion

The common-base circuit is very useful when the input signal is a current. We will see this type of application when we discuss the cascode circuit in Section 6.9.

Test Your Understanding

TYU 6.13 For the circuit shown in Figure 6.66, the transistor parameters are: $\beta = 100$, $V_{EB}(\text{on}) = 0.7$ V, and $r_o = \infty$. (a) Calculate the quiescent values of I_{CQ} and V_{ECQ}. (b) Determine the small-signal current gain $A_i = i_o / i_i$. (c) Determine the small-signal voltage gain $A_v = v_o / v_s$. (Ans. (a) $I_{CQ} = 0.921$ mA, $V_{ECQ} = 6.1$ V (b) $A_i = 0.987$ (c) $A_v = 177$)

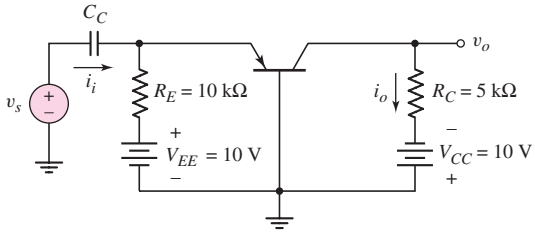


Figure 6.66 Figure for Exercise TYU 6.13

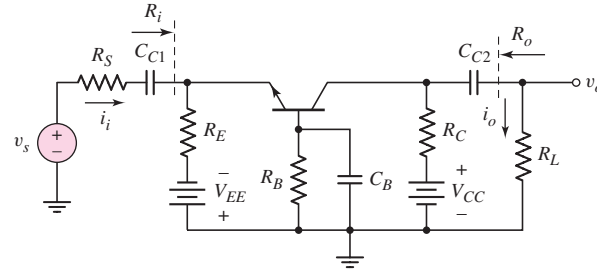


Figure 6.67 Figure for Exercises TYU 6.14 and TYU 6.15

TYU 6.14 For the circuit shown in Figure 6.67, the parameters are: $R_B = 100\ \text{k}\Omega$, $R_E = 10\ \text{k}\Omega$, $R_C = 10\ \text{k}\Omega$, $V_{CC} = V_{EE} = 10\ \text{V}$, $R_L = 1\ \text{k}\Omega$, $R_S = 1\ \text{k}\Omega$, $V_{BE}(\text{on}) = 0.7\ \text{V}$, $\beta = 100$, and $V_A = \infty$. (a) Determine the small-signal transistor parameters g_m, r_π, and r_o. (b) Find the small-signal current gain $A_i = i_o/i_i$ and the small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the input resistance R_i and the output resistance R_o. (Ans. (a) $r_\pi = 3.1\ \text{k}\Omega$, $g_m = 32.23\ \text{mA/V}$, $r_o = \infty$ (b) $A_v = 0.870$, $A_i = 0.90$ (c) $R_i = 30.6\ \Omega$, $R_o = 10\ \text{k}\Omega$)

TYU 6.15 For the circuit shown in Figure 6.67, let $R_S = 0$, $C_B = 0$, $R_C = R_L = 2\ \text{k}\Omega$, $V_{CC} = V_{EE} = 5\ \text{V}$, $\beta = 100$, $V_{BE}(\text{on}) = 0.7\ \text{V}$, and $V_A = \infty$. Design R_E and R_B for a dc quiescent collector current of 1 mA and a small-signal voltage gain of 20. (Ans. $R_B = 2.4\ \text{k}\Omega$, $R_E = 4.23\ \text{k}\Omega$)

COMPUTER ANALYSIS EXERCISE

PS 6.6: Using a PSpice simulation, verify the common-base circuit design in the Test Your Understanding exercise TYU6.15. Use a standard transistor.

6.8 THE THREE BASIC AMPLIFIERS: SUMMARY AND COMPARISON

Objective: • Compare the general characteristics of the three basic amplifier configurations.

The basic small-signal characteristics of the three single-stage amplifier configurations are summarized in Table 6.4.

For the common-emitter circuit, the voltage and current gains are generally greater than 1. For the emitter-follower, the voltage gain is slightly less than 1, while the current gain is greater than 1. For the common-base circuit, the voltage gain is greater than 1, while the current gain is less than 1.

The input resistance looking into the base terminal of a common-emitter circuit may be in the low kilohm range; in an emitter follower, it is generally in the 50 to 100 kΩ range. The input resistance looking into the emitter of a common-base circuit is generally on the order of tens of ohms.

The overall input resistance of both the common-emitter and emitter-follower circuits can be greatly affected by the bias circuitry.

Table 6.4 Characteristics of the three BJT amplifier configurations

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common emitter	$A_v > 1$	$A_i > 1$	Moderate	Moderate to high
Emitter follower	$A_v \cong 1$	$A_i > 1$	High	Low
Common base	$A_v > 1$	$A_i \cong 1$	Low	Moderate to high

The output resistance of the emitter follower is generally in the range of a few ohms to tens of ohms. In contrast, the output resistance looking into the collector terminal of the common-emitter and common-base circuits is very high. In addition, the output resistance looking back into the output terminal of the common-emitter and common-base circuits is a strong function of the collector resistance. For these circuits, the output resistance can easily drop to a few kilohms.

The characteristics of these single-stage amplifiers will be used in the design of multistage amplifiers.

6.9 MULTISTAGE AMPLIFIERS

Objective: • Analyze multitransistor or multistage amplifiers and understand the advantages of these circuits over single-transistor amplifiers.

In most applications, a single transistor amplifier will not be able to meet the combined specifications of a given amplification factor, input resistance, and output resistance. For example, the required voltage gain may exceed that which can be obtained in a single transistor circuit. We also saw an illustration of this effect in Example 6.15, in which a low output resistance was required in a particular design.

Transistor amplifier circuits can be connected in series, or **cascaded,** as shown in Figure 6.68. This may be done either to increase the overall small-signal voltage gain or to provide an overall voltage gain greater than 1, with a very low output resistance. The overall voltage or current gain, in general, is not simply the product of the individual amplification factors. For example, the gain of stage 1 is a function of the input resistance of stage 2. In other words, loading effects may have to be taken into account.

There are many possible multistage configurations; we will examine a few here, in order to understand the type of analysis required.

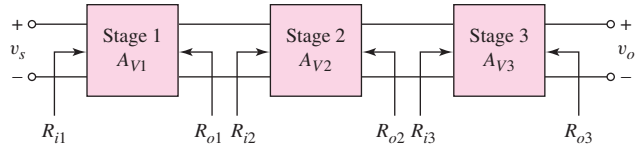


Figure 6.68 A generalized three-stage amplifier

6.9.1 Multistage Analysis: Cascade Configuration

In Figure 6.69, the circuit is a cascade configuration of two common-emitter circuits. The dc analysis of this circuit, done in Example 5.21 of Chapter 5, showed that both transistors are biased in the forward-active mode. Figure 6.70 shows the small-signal equivalent circuit, assuming all capacitors act as short circuits and each transistor output resistance r_o is infinite.

We may start the analysis at the output and work back to the input, or start at the input and work toward the output.

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = g_{m1}g_{m2}(R_{C1} \| r_{\pi 2})(R_{C2} \| R_L)\left(\frac{R_i}{R_i + R_S}\right) \tag{6.102}$$

The input resistance of the amplifier is

$$R_i = R_1 \| R_2 \| r_{\pi 1}$$

which is identical to that of a single-stage common-emitter amplifier. Similarly, the output resistance looking back into the output terminals is $R_o = R_{C2}$. To determine the output resistance, the independent source V_s is set equal to zero, which means that $V_{\pi 1} = 0$. Then $g_{m1}V_{\pi 1} = 0$, which gives $V_{\pi 2} = 0$ and $g_{m2}V_{\pi 2} = 0$. The output resistance is therefore R_{C2}. Again, this is the same as the output resistance of a single-stage common-emitter amplifier.

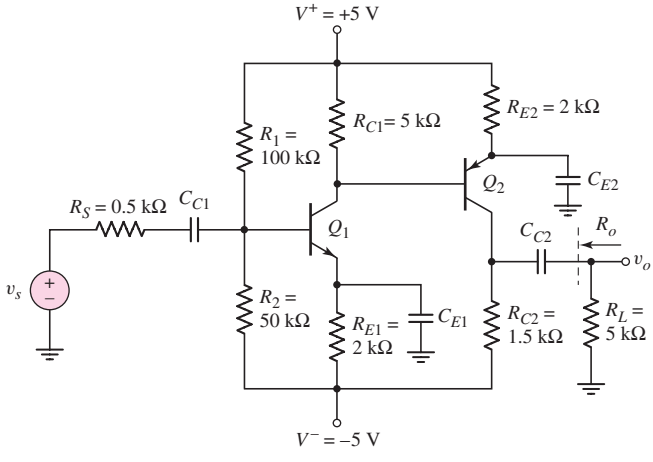


Figure 6.69 A two-stage common-emitter amplifier in a cascade configuration with npn and pnp transistors

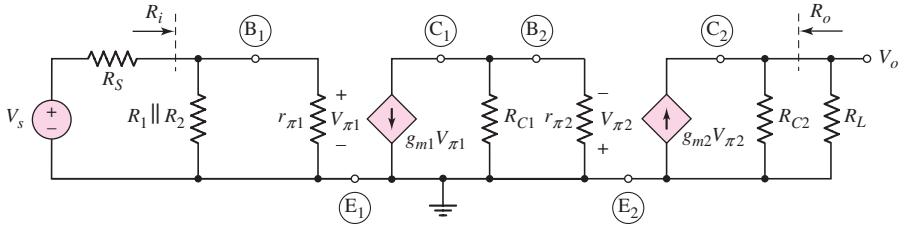


Figure 6.70 Small-signal equivalent circuit of the cascade circuit shown in Figure 6.69

COMPUTER EXAMPLE 6.16

Objective: Determine the small-signal voltage gain of the multitransistor circuit shown in Figure 6.69 using a PSpice analysis.

The dc and ac analyses of a multitransistor circuit become more complex compared to those for a single-transistor circuit. In this situation, a computer simulation of the circuit, without a hand analysis, is extremely useful.

The PSpice circuit schematic diagram is shown in Figure 6.71. Also given are the Q-point values of the transistors. The ac voltage at the collector of the npn transistor is 51 μV and that at the collector of the pnp transistor is 4.79 mV. Since the

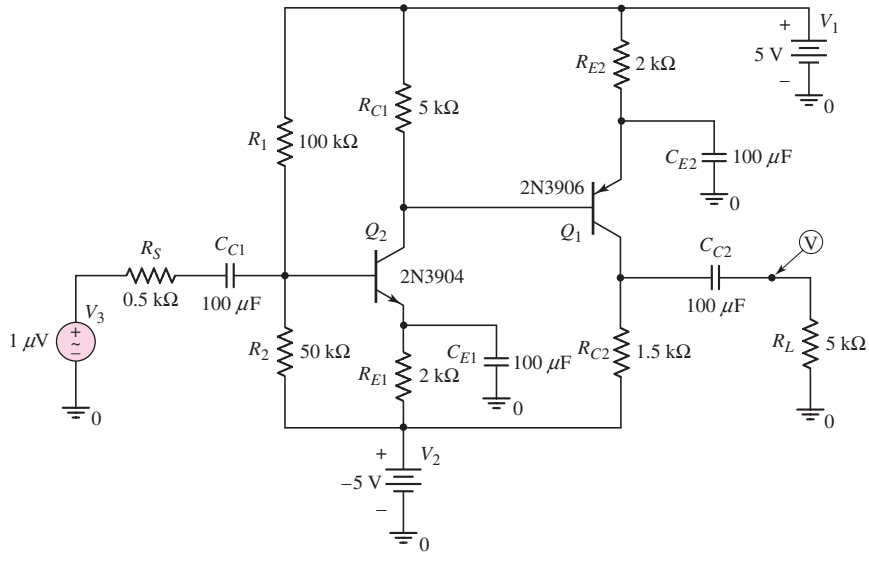


Figure 6.71 PSpice circuit schematic for Example 6.16

input voltage was assumed to be 1 μV, this result shows that a significant voltage gain can be achieved in a two-stage amplifier.

```
**** BIPOLAR JUNCTION TRANSISTORS
NAME        Q_Q1          Q_Q2
MODEL       Q2N3906       Q2N3904
IB        -1.42E-05      8.59E-06
IC        -2.54E-03      1.18E-03
VBE       -7.30E-01      6.70E-01
VBC        3.68E-01     -1.12E+00
VCE       -1.10E+00      1.79E+00
BETADC     1.79E+02      1.37E+02
GM         9.50E-02      4.48E-02
RPI        1.82E+03      3.49E+03
RX         1.00E+01      1.00E+01
RO         7.52E+03      6.37E+04
CBE        3.11E-11      2.00E-11
CBC        7.75E-12      2.74E-12
CJS        0.00E+00      0.00E+00
BETAAC     1.73E+02      1.57E+02
CBX        0.00E+00      0.00E+00
FT         3.89E+08      3.14E+08
```

Comment: We can see from the Q-point values that the collector–emitter voltage of each transistor is quite small. This implies that the maximum symmetrical swing in the output voltage is limited to a fairly small value. These Q-point values can be increased by a slight redesign of the circuit.

Discussion: The transistors used in this PSpice analysis of the circuit were standard bipolar transistors from the PSpice library. We must keep in mind that, for the computer simulation to be valid, the models of the devices used in the simulation must match those of the actual devices used in the circuit. If the actual transistor characteristics were substantially different from those used in the computer simulation, then the results of the computer analysis would not be accurate.

EXERCISE PROBLEM

Ex 6.16: For each transistor in the circuit in Figure 6.72, the parameters are: $\beta = 125$, $V_{BE}(\text{on}) = 0.7$ V, and $r_o = \infty$. (a) Determine the Q-points of each transistor. (b) Find the overall small-signal voltage gain $A_v = V_o/V_s$. (c) Determine the input resistance R_i and the output resistance R_o. (Ans. (a) $I_{CQ1} = 0.364$ mA, $V_{CEQ1} = 7.92$ V, $I_{CQ2} = 4.82$ mA, $V_{CEQ2} = 2.71$ V (b) $A_v = -17.7$ (c) $R_i = 4.76$ kΩ, $R_o = 43.7$ Ω)

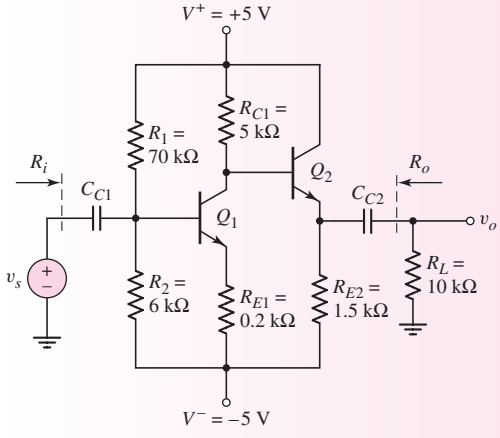


Figure 6.72 Figure for Exercise Ex6.16

6.9.2 Multistage Circuit: Darlington Pair Configuration

In some applications, it would be desirable to have a bipolar transistor with a much larger current gain than can normally be obtained. Figure 6.73(a) shows a multitransistor configuration, called a **Darlington pair** or a **Darlington configuration,** that provides increased current gain.

The small-signal equivalent in which the input signal is assumed to be a current source, is shown in Figure 6.73(b). We will use the input current source to determine the current gain of the circuit. To determine the small-signal current gain $A_i = I_o/I_i$, we see that

$$V_{\pi 1} = I_i r_{\pi 1} \qquad \textbf{(6.103)}$$

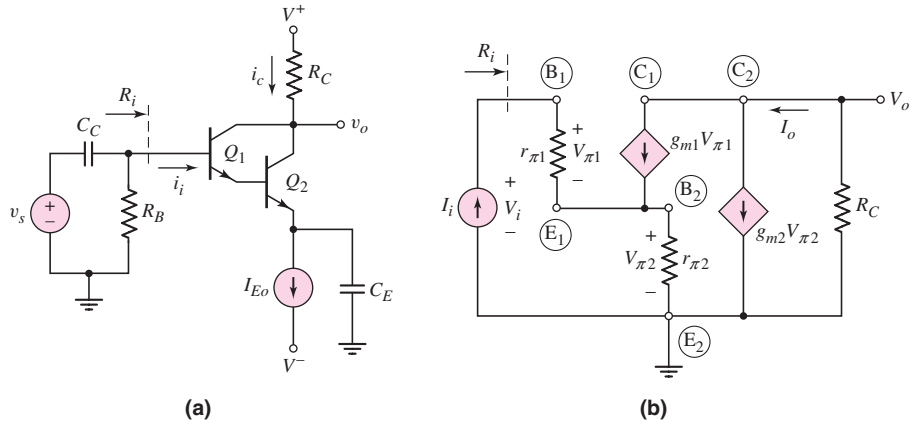


Figure 6.73 (a) A Darlington pair configuration; (b) small-signal equivalent circuit

Therefore,

$$g_{m1}V_{\pi 1} = g_{m1}r_{\pi 1}I_i = \beta_1 I_i \tag{6.104}$$

Then,

$$V_{\pi 2} = (I_i + \beta_1 I_i)r_{\pi 2} \tag{6.105}$$

The output current is

$$I_o = g_{m1}V_{\pi 1} + g_{m2}V_{\pi 2} = \beta_1 I_i + \beta_2(1 + \beta_1)I_i \tag{6.106}$$

where $g_{m2}r_{\pi 2} = \beta_2$. The overall current gain is then

$$A_i = \frac{I_o}{I_i} = \beta_1 + \beta_2(1 + \beta_1) \cong \beta_1\beta_2 \tag{6.107}$$

From Equation (6.107), we see that the overall small-signal current gain of the Darlington pair is essentially the product of the individual current gains.

The input resistance is $R_i = V_i/I_i$. We can write that

$$V_i = V_{\pi 1} + V_{\pi 2} = I_i r_{\pi 1} + I_i(1 + \beta_1)r_{\pi 2} \tag{6.108}$$

so that

$$R_i = r_{\pi 1} + (1 + \beta_1)r_{\pi 2} \tag{6.109}$$

The base of transistor Q_2 is connected to the emitter of Q_1, which means that the input resistance to Q_2 is multiplied by the factor $(1 + \beta_1)$, as we saw in circuits with emitter resistors. We can write

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} \tag{6.110}$$

and

$$I_{CQ1} \cong \frac{1_{CQ2}}{\beta_2} \tag{6.111}$$

Therefore,

$$r_{\pi 1} = \beta_1\left(\frac{\beta_2 V_T}{I_{CQ2}}\right) = \beta_1 r_{\pi 2} \tag{6.112}$$

From Equation (6.109), the input resistance is then approximately

$$R_i \cong 2\beta_1 r_{\pi 2} \tag{6.113}$$

We see from these equations that the overall gain of the Darlington pair is large. At the same time, the input resistance tends to be large, because of the β multiplication.

6.9.3 Multistage Circuit: Cascode Configuration

A slightly different multistage configuration, called a **cascode configuration,** is shown in Figure 6.74(a). The input is into a common-emitter amplifier (Q_1), which drives a common-base amplifier (Q_2). The ac equivalent circuit is shown in Figure 6.74(b). We see that the output signal current of Q_1 is the input signal of Q_2. We mentioned previously that, normally, the input signal of a common-base configuration is to be a current. One advantage of this circuit is that the output resistance looking into the collector of Q_2 is much larger than the output resistance of a simple common-emitter circuit. Another important advantage of this circuit is in the frequency response, as we will see in Chapter 7.

The small-signal equivalent circuit is shown in Figure 6.75 for the case when the capacitors act as short circuits. We see that $V_{\pi 1} = V_s$ since we are assuming an ideal signal voltage source. Writing a KCL equation at E_2, we have

$$g_{m1} V_{\pi 1} = \frac{V_{\pi 2}}{r_{\pi 2}} + g_{m2} V_{\pi 2} \tag{6.114}$$

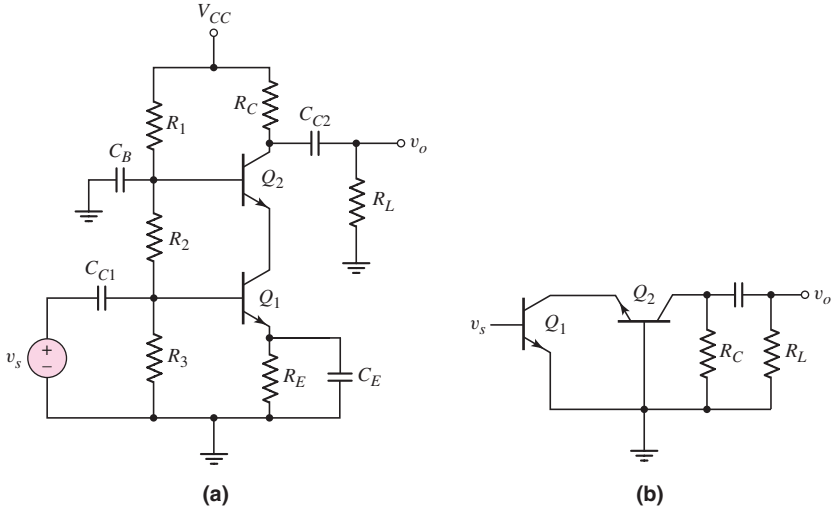


Figure 6.74 (a) Cascode amplifier and (b) the ac equivalent circuit

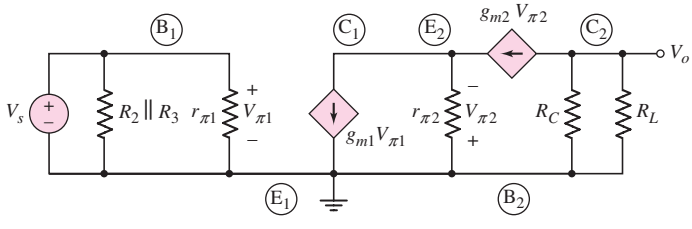


Figure 6.75 Small-signal equivalent circuit of the cascode configuration

Solving for the control voltage $V_{\pi 2}$ (noting that $V_{\pi 1} = V_s$), we find

$$V_{\pi 2} = \left(\frac{r_{\pi 2}}{1+\beta_2}\right)(g_{m1}V_s) \tag{6.115}$$

where $\beta_2 = g_{m2}r_{\pi 2}$. The output voltage is

$$V_o = -(g_{m2}V_{\pi 2})(R_C \| R_L) \tag{6.116(a)}$$

or

$$V_o = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C \| R_L)V_s \tag{6.116(b)}$$

Therefore, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C \| R_L) \tag{6.117}$$

An examination of Equation (6.117) shows

$$g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right) = \frac{\beta_2}{1+\beta_2} \cong 1 \tag{6.118}$$

The gain of the cascode amplifier is then approximately

$$A_v \cong -g_{m1}(R_C \| R_L) \tag{6.119}$$

which is the same as for a single-stage common-emitter amplifier. This result is to be expected since the current gain of the common-base circuit is essentially unity.

Test Your Understanding

TYU 6.16 Consider the circuit in Figure 6.73(a). Let $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$ for each transistor. Assume $R_B = 10\,\text{k}\Omega$, $R_C = 4\,\text{k}\Omega$, $I_{Eo} = 1$ mA, $V^+ = 5$ V, and $V^- = -5$ V. (a) Determine the Q-point values for each transistor. (b) Calculate the small-signal hybrid-π parameters for each transistor. (c) Find the overall small-signal voltage gain $A_v = V_o/V_s$. (d) Find the input resistance R_i. (Ans. (a) $I_{CQ1} = 0.0098$ mA, $V_{CEQ1} = 1.7$ V, $I_{CQ2} = 0.990$ mA, $V_{CEQ2} = 2.4$ V (b) $r_{\pi 1} = 265\,\text{k}\Omega$, $g_{m1} = 0.377$ mA/V, $r_{\pi 2} = 2.63\,\text{k}\Omega$, $g_{m2} = 38.1$ mA/V (c) $A_v = -77.0$ (d) $R_i = 531\,\text{k}\Omega$)

TYU 6.17 Consider the cascode circuit in Figure 6.74(a). Let $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$ for each transistor. Assume $V_{CC} = 12$ V, $R_L = 2\,\text{k}\Omega$, and $R_E = 0.5\,\text{k}\Omega$. (a) Find R_C, R_1, R_2, and R_3 such that $I_{CQ2} = 0.5$ mA and $V_{CE1} = V_{CE2} = 4$ V. Let $R_1 + R_2 + R_3 = 100\,\text{k}\Omega$. (Hint: Neglect the dc base currents and assume $I_C = I_E$ in both Q_1 and Q_2.) (b) Determine the small-signal hybrid-π parameters for each transistor. (c) Determine the small-signal voltage gain $A_v = V_o/V_s$. (Ans. (a) $R_C = 7.5\,\text{k}\Omega$, $R_3 = 7.92\,\text{k}\Omega$, $R_1 = 33.3\,\text{k}\Omega$, $R_1 = 58.8\,\text{k}\Omega$ (b) $r_{\pi 1} = r_{\pi 2} = 5.2\,\text{k}\Omega$, $g_{m1} = g_{m2} = 19.23$ mA/V, $r_{o1} = r_{o2} = \infty$ (c) $A_v = -30.1$)

COMPUTER ANALYSIS EXERCISE

PS 6.7: Verify the cascode circuit design in the Test Your Understanding exercise TYU6.17 using a PSpice analysis. Use standard transistors. Find the transistor Q-point values and the small-signal voltage gain.

6.10 POWER CONSIDERATIONS

Objective: • Analyze the ac and dc power dissipation in a transistor amplifier and understand the concept of signal power gain.

As mentioned previously, an amplifier produces a **small-signal power gain.** Since energy must be conserved, the question naturally arises as to the source of this "extra" signal power. We will see that the "extra" signal power delivered to a load is a result of a redistribution of power between the load and the transistor.

Consider the simple common-emitter circuit shown in Figure 6.76 in which an ideal signal voltage source is connected at the input. The dc power supplied by the V_{CC} voltage source P_{CC}, the dc power dissipated or supplied to the collector resistor P_{RC}, and the dc power dissipated in the transistor P_Q are given, respectively, as

$$P_{CC} = I_{CQ}V_{CC} + P_{\text{Bias}} \tag{6.120(a)}$$

$$P_{RC} = I_{CQ}^2 R_c \tag{6.120(b)}$$

and

$$P_Q = I_{CQ}V_{CEQ} + I_{BQ}V_{BEQ} \cong I_{CQ}V_{CEQ} \tag{6.120(c)}$$

The term P_{Bias} is the power dissipated in the bias resistors R_1 and R_2. Normally in a transistor $I_{CQ} \gg I_{BQ}$, so the power dissipated is primarily a function of the collector current and collector–emitter voltage.

If the signal voltage is given by

$$v_s = V_p \cos \omega t \tag{6.121}$$

then the total base current is given by

$$i_B = I_{BQ} + \frac{V_p}{r_\pi} \cos \omega t = I_{BQ} + I_b \cos \omega t \tag{6.122}$$

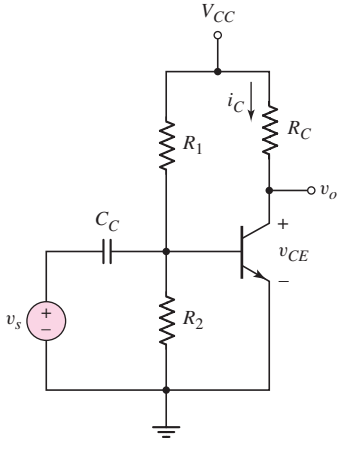


Figure 6.76 Simple common-emitter amplifier for power calculations

and the total collector current is

$$i_C = I_{CQ} + \beta I_b \cos \omega t = I_{CQ} + I_c \cos \omega t \tag{6.123}$$

The total instantaneous collector-emitter voltage is

$$v_{CE} = V_{CC} - i_C R_C = V_{CC} - (I_{CQ} + I_c \cos \omega t) R_C = V_{CEQ} - I_c R_C \cos \omega t \tag{6.124}$$

The average power, including ac signals, supplied by the voltage source V_{CC} is given by

$$\begin{aligned} \bar{p}_{cc} &= \frac{1}{T} \int_0^T V_{CC} \cdot i_C \, dt + P_{\text{Bias}} \\ &= \frac{1}{T} \int_0^T V_{CC} \cdot [I_{CQ} + I_c \cos \omega t] \, dt + P_{\text{Bias}} \\ &= V_{CC} I_{CQ} + \frac{V_{CC} I_c}{T} \int_0^T \cos \omega t \, dt + P_{\text{Bias}} \end{aligned} \tag{6.125}$$

Since the integral of the cosine function over one period is zero, the average power supplied by the voltage source is the same as the dc power supplied. The dc voltage source does not supply additional power.

The average power delivered to the load R_C is found from

$$\begin{aligned} \bar{p}_{RC} &= \frac{1}{T} \int_0^T i_C^2 R_C \, dt = \frac{R_C}{T} \int_0^T [I_{CQ} + I_c \cos \omega t]^2 \, dt \\ &= \frac{I_{CQ}^2 R_C}{T} \int_0^T dt + \frac{2 I_{CQ} I_c}{T} \int_0^T \cos \omega t \, dt + \frac{I_c^2 R_C}{T} \int_0^T \cos^2 \omega t \, dt \end{aligned} \tag{6.126}$$

The middle term of this last expression is again zero, so

$$\bar{p}_{RC} = I_{CQ}^2 R_C + \tfrac{1}{2} I_c^2 R_C \tag{6.127}$$

The average power delivered to the load has increased because of the signal source. This is expected in an amplifier.

Now, the average power dissipated in the transistor is

$$\begin{aligned} \bar{p}_Q &= \frac{1}{T} \int_0^T i_C \cdot v_{CE} \, dt \\ &= \frac{1}{T} \int_0^T [I_{CQ} + I_c \cos \omega t] \cdot [V_{CEQ} - I_c R_C \cos \omega t] \, dt \end{aligned} \tag{6.128}$$

which produces

$$\bar{p}_Q = I_{CQ} V_{CEQ} - \frac{I_c^2 R_C}{T} \int_0^T \cos^2 \omega t \, dt \tag{6.129(a)}$$

or

$$\bar{p}_Q = I_{CQ} V_{CEQ} - \tfrac{1}{2} I_c^2 R_C \tag{6.129(b)}$$

From Equation (6.129(b)), we can deduce that the average power dissipated in the transistor decreases when an ac signal is applied. The V_{CC} source still supplies all of the power, but the input signal changes the relative distribution of power between the transistor and the load.

Test Your Understanding

TYU 6.18 In the circuit in Figure 6.77 the transistor parameters are: $\beta = 80$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. Determine the average power dissipated in R_C, R_L, and Q for: (a) $v_s = 0$, and (b) $v_s = 18 \cos \omega t$ mV. (Ans. (a) $\bar{p}_{RC} = 8$ mW, $\bar{p}_{RL} = 0$, $\bar{p}_Q = 14$ mW (b) $\bar{p}_Q = 13.0$ mW, $\bar{p}_{RL} = 0.479$ mW, $\bar{p}_{RC} = 8.48$ mW)

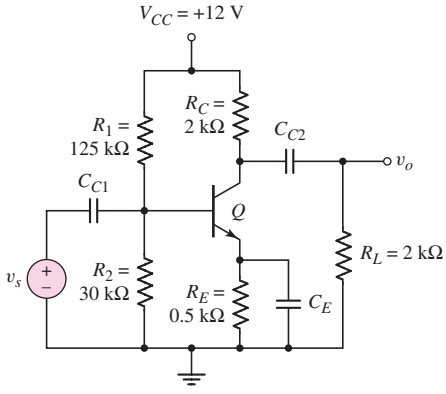


Figure 6.77 Figure for Exercise TYU 6.18

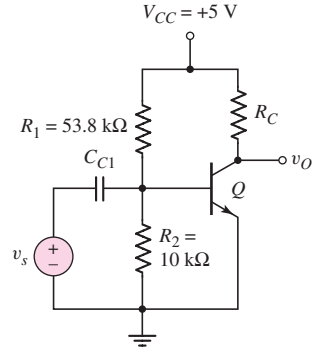


Figure 6.78 Figure for Exercise TYU 6.19

TYU 6.19 For the circuit in Figure 6.78, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. (a) Determine R_C such that the Q-point is in the center of the load line. (b) Determine the average power dissipated in R_C and Q for $v_s = 0$. (c) Considering the maximum symmetrical swing in the output voltage, determine the ratio of maximum signal power delivered to R_C to the total power dissipated in R_C and the transistor. (Ans. (a) $R_C = 2.52\,\text{k}\Omega$ (b) $\bar{p}_{RC} = \bar{p}_Q = 2.48$ mW (c) 0.25)

6.11 DESIGN APPLICATION: AUDIO AMPLIFIER

Objective: • Design a bipolar transistor audio amplifier to meet a set of specifications.

Specifications: An audio amplifier is to deliver an average power of 0.1 W to an 8 Ω speaker from a microphone that produces a 10 mV peak sinusoidal signal and has a source resistance of 10 kΩ.

Design Approach: A direct, perhaps brute force, approach will be taken in this design. The generalized multistage amplifier configuration that will be designed is shown in Figure 6.79. An input buffer stage, which will be an emitter-follower circuit, is to be used to reduce the loading effect of the 10 kΩ source resistance. The output stage will also be an emitter-follower circuit to provide the necessary output current and output signal power. The gain stage will actually be composed of a 2-stage common-emitter amplifier that will provide the necessary voltage gain. We will assume that the entire amplifier system is biased with a 12 volt power supply.

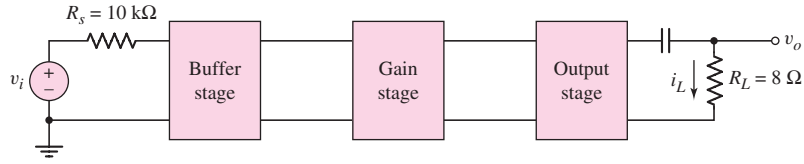


Figure 6.79 Generalized multistage amplifier for design application

Solution (Input Buffer Stage): The input buffer stage, an emitter-follower amplifier, is shown in Figure 6.80. We will assume that the transistor has a current gain of $\beta_1 = 100$. We will design the circuit so that the quiescent collector current is $I_{CQ1} = 1$ mA, the quiescent collector-emitter voltage is $V_{CEQ1} = 6$ V, and $R_1 \| R_2 = 100$ kΩ.

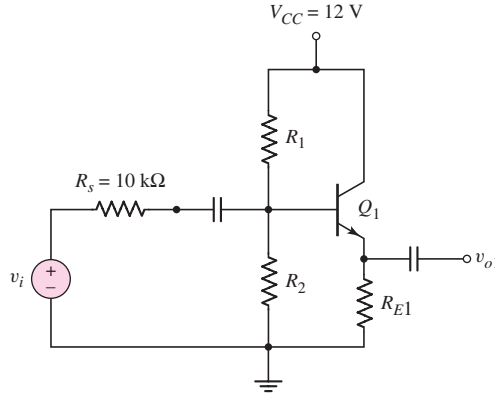


Figure 6.80 Input signal source and input buffer stage (emitter-follower) for design application

We find

$$R_{E1} \cong \frac{V_{CC} - V_{CEQ1}}{I_{CQ1}} = \frac{12 - 6}{1} = 6 \text{ kΩ}$$

We obtain

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} = \frac{(100)(0.026)}{1} = 2.6 \text{ kΩ}$$

We also have, neglecting the loading effect of the next stage,

$$\begin{aligned} R_{i1} &= R_1 \| R_2 \| [r_{\pi 1} + (1 + \beta_1) R_{E1}] \\ &= 100 \| [2.6 + (101)(6)] = 85.9 \text{ kΩ} \end{aligned}$$

The small-signal voltage gain, from Equation (6.68) and assuming that $r_o = \infty$, is (again neglecting the loading effect from the next stage)

$$\begin{aligned} A_{v1} &= \frac{v_{o1}}{v_i} = \frac{(1 + \beta_1) R_{E1}}{r_{\pi 1} + (1 + \beta_1) R_{E1}} \cdot \left(\frac{R_{i1}}{R_{i1} + R_S} \right) \\ &= \frac{(101)(6)}{2.6 + (101)(6)} \cdot \left(\frac{85.9}{85.9 + 10} \right) \end{aligned}$$

or

$$A_{v1} = 0.892$$

For a 10 mV peak input signal voltage, the peak voltage at the output of the buffer stage is now $v_{o1} = 8.92$ mV.

We find the bias resistors to be $R_1 = 155\,\text{k}\Omega$ and $R_2 = 282\,\text{k}\Omega$.

Solution (Output Stage): The output stage, another emitter-follower amplifier circuit, is shown in Figure 6.81. The 8 Ω speaker is capacitively coupled to the output of the amplifier. The coupling capacitor ensures that no dc current flows through the speaker.

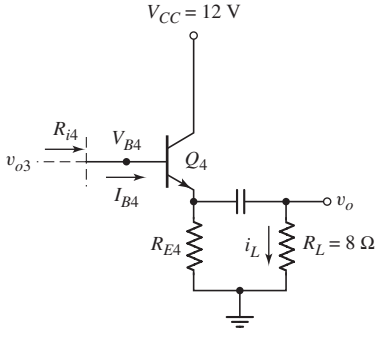


Figure 6.81 Output stage (emitter-follower) for design application

For an average power of 0.1 W to be delivered to the load, the rms value of the load current is found from $P_L = i_L^2(\text{rms}) \cdot R_L$ or $0.1 = i_L^2(\text{rms}) \cdot 8$ which yields $i_L(\text{rms}) = 0.112$ A. For a sinusoidal signal, the peak output current is then

$$i_L(\text{peak}) = 0.158 \text{ A}$$

and the peak output voltage is

$$v_o(\text{peak}) = (0.158)(8) = 1.26 \text{ V}$$

We will assume that the output power transistor has a current gain of $\beta_4 = 50$. We will set the quiescent transistor parameters at

$$I_{EQ4} = 0.3 \text{ A} \qquad \text{and} \qquad V_{CEQ4} = 6 \text{ V}$$

Then

$$R_{E4} = \frac{V_{CC} - V_{CEQ4}}{I_{EQ4}} = \frac{12 - 6}{0.3} = 20\ \Omega$$

We find

$$I_{CQ4} = \left(\frac{\beta_4}{1 + \beta_4}\right) \cdot I_{EQ4} = \left(\frac{50}{51}\right)(0.3) = 0.294 \text{ A}$$

Then

$$r_{\pi 4} = \frac{\beta_4 V_T}{I_{CQ4}} = \frac{(50)(0.026)}{0.294} = 4.42\ \Omega$$

The small-signal voltage gain of the output stage is

$$A_{v4} = \frac{v_o}{v_{o3}} = \frac{(1+\beta_4)(R_{E4} \| R_L)}{r_{\pi 4} + (1+\beta_4)(R_{E4} \| R_L)}$$
$$= \frac{(51)(20\|8)}{4.42 + (51)(20\|8)} = 0.985$$

which is very close to unity, as we would expect. For a required peak output voltage of $v_o = 1.26$ V, we then need a peak voltage at the output of the gain stage to be $v_{o3} = 1.28$ V.

Solution (Gain Stage): The gain stage, which will actually be a two-stage common-emitter amplifier, is shown in Figure 6.82. We will assume that the buffer stage is capacitively coupled to the input of the amplifier, the two stages of the amplifier are capacitively coupled, and the output of this amplifier is directly coupled to the output stage.

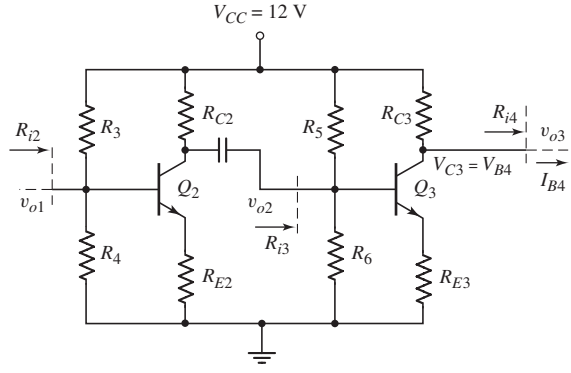


Figure 6.82 Gain stage (two-stage common-emitter amplifier) for design application

We include emitter resistors to help stabilize the voltage gain of the amplifier. Assume that each transistor has a current gain of $\beta = 100$.

The overall gain (magnitude) of this amplifier must be

$$\left|\frac{v_{o3}}{v_{o1}}\right| = \frac{1.28}{0.00892} = 144$$

We will design the amplifier so that the individual gains (magnitudes) are

$$|A_{v3}| = \left|\frac{v_{o3}}{v_{o2}}\right| = 5 \qquad \text{and} \qquad |A_{v2}| = \left|\frac{v_{o2}}{v_{o1}}\right| = 28.8$$

The dc voltage at the collector of Q_3 (with $V_{BE4}(\text{on}) = 0.7$ V) is $V_{C3} = V_{B4} = 6 + 0.7 = 6.7$ V. The quiescent base current to the output transistor is $I_{B4} = 0.294/50$ or $I_{B4} = 5.88$ mA. If we set the quiescent collector current in Q_3 to be $I_{CQ3} = 15$ mA, then $I_{RC3} = 15 + 5.88 = 20.88$ mA. Then

$$R_{C3} = \frac{V_{CC} - V_{C3}}{I_{RC3}} = \frac{12 - 6.7}{20.88} \Rightarrow 254\ \Omega$$

Also

$$r_{\pi 3} = \frac{\beta_3 V_T}{I_{CQ3}} = \frac{(100)(0.026)}{15} \Rightarrow 173\ \Omega$$

We also find

$$\begin{aligned} R_{i4} &= r_{\pi 4} + (1+\beta_4)(R_{E4} \| R_L) \\ &= 4.42 + (51)(20\|8) = 296\ \Omega \end{aligned}$$

The small-signal voltage gain, for a common-emitter amplifier with an emitter resistor, can be written as

$$|A_{v3}| = \left|\frac{v_{o3}}{v_{o2}}\right| = \frac{\beta_3 (R_{C3} \| R_{i4})}{r_{\pi 3} + (1+\beta_3) R_{E3}}$$

Setting $|A_{v3}| = 5$, we have

$$5 = \frac{(100)(254\|296)}{173 + (101) R_{E3}}$$

which yields $R_{E3} = 25.4\ \Omega$.

If we set $R_5 \| R_6 = 50\ \text{k}\Omega$, we find $R_5 = 69.9\ \text{k}\Omega$ and $R_6 = 176\ \text{k}\Omega$.

Finally, if we set $V_{C2} = 6$ V and $I_{CQ2} = 5$ mA, then

$$R_{C2} = \frac{V_{CC} - V_{C2}}{I_{CQ2}} = \frac{12 - 6}{5} = 1.2\ \text{k}\Omega$$

Also

$$r_{\pi 2} = \frac{\beta_2 V_T}{I_{CQ2}} = \frac{(100)(0.026)}{5} = 0.52\ \text{k}\Omega$$

and

$$\begin{aligned} R_{i3} &= R_5 \| R_6 \| [r_{\pi 3} + (1+\beta_3) R_{E3}] \\ &= 50 \| [0.173 + (101)(0.0254)] = 2.60\ \text{k}\Omega \end{aligned}$$

The expression for the voltage gain can be written as

$$|A_{v2}| = \left|\frac{v_{o2}}{v_{o1}}\right| = \frac{\beta_2 (R_{C2} \| R_{i3})}{r_{\pi 2} + (1+\beta_2) R_{E2}}$$

Setting $|A_{v2}| = 28.8$, we find

$$28.8 = \frac{(100)(1.2\|2.6)}{0.52 + (101) R_{E2}}$$

which yields $R_{E2} = 23.1\ \Omega$.

If we set $R_3 \| R_4 = 50\ \text{k}\Omega$, we find $R_3 = 181\ \text{k}\Omega$ and $R_4 = 69.1\ \text{k}\Omega$.

Comment: We may note that, as with any design, there is no unique solution. In addition, to actually build this circuit with discrete components, we would need to use standard values for resistors, which means the quiescent current and voltage values will change, and the overall voltage gain will probably change from the designed value. Also, the current gains of the actual transistors used will probably not be exactly equal to the assumed values. Therefore some slight modifications will likely need to be made in the final design.

Discussion: We implicitly assumed that we were designing an audio amplifier, but we have not discussed the frequency response. For example, the coupling capacitors in the design must be large enough to pass audio signal frequencies. The frequency response of amplifiers will be discussed in detail in Chapter 7.

We will also see in later chapters, in particular Chapter 8, that a more efficient output stage can be designed. The efficiency of the output stage in this design is relatively small; that is, the average signal power delivered to the load is small compared to the average power dissipated in the output stage. However, this design is a first approximation in the design process.

6.12 SUMMARY

- This chapter emphasized the application of bipolar transistors in linear amplifier circuits. The basic process by which a transistor circuit can amplify a small time-varying input signal was discussed.
- The ac equivalent circuit and the hybrid-π equivalent circuit of the bipolar transistor were developed. These equivalent circuits are used in the analysis and design of transistor amplifier circuits.
- Three basic circuit configurations were considered: the common emitter, emitter follower, and common base. These three configurations form the basic building blocks for more complex integrated circuits.
- The common-emitter circuit amplifies both time-varying voltages and currents.
- The emitter-follower circuit amplifies time-varying currents, and has a large input resistance and low output resistance.
- The common-base circuit amplifies time-varying voltages, and has a low input resistance and large output resistance.
- Three multitransistor circuits were considered: a cascade configuration of two common-emitter circuits, a Darlington pair, and a cascode configuration formed by common-emitter and common-base circuits. Each configuration provides specialized characteristics such as an overall larger voltage gain or an overall larger current gain.
- The concept of signal power gain in amplifier circuits was discussed. There is a redistribution of power within the amplifier circuit.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

- ✓ Explain graphically the amplification process in a simple bipolar amplifier circuit.
- ✓ Describe the small-signal hybrid-π equivalent circuit of the bipolar transistor and to determine the values of the small-signal hybrid-π parameters.
- ✓ Apply the small-signal hybrid-π equivalent circuit to various bipolar amplifier circuits to obtain the time-varying circuit characteristics.
- ✓ Characterize the small-signal voltage and current gains and the input and output resistances of a common-emitter amplifier.
- ✓ Characterize the small-signal voltage and current gains and the input and output resistances of an emitter-follower amplifier.
- ✓ Characterize the small-signal voltage and current gains and the input and output resistances of a common-base amplifier.
- ✓ Apply the bipolar small-signal equivalent circuit in the analysis of multistage amplifier circuits.

REVIEW QUESTIONS

1. Discuss, using the concept of a load line superimposed on the transistor characteristics, how a simple common-emitter circuit can amplify a time-varying signal.
2. Why can the analysis of a transistor circuit be split into a dc analysis, with all ac sources set equal to zero, and then an ac analysis, with all dc sources set equal to zero?
3. Sketch the hybrid-π equivalent circuit of an npn and a pnp bipolar transistor.
4. State the relationships of the small-signal hybrid-π parameters g_m, r_π, and r_o to the transistor dc quiescent values.
5. What are the physical meanings of the hybrid-π parameters r_π and r_o?
6. What does the term small-signal imply?
7. Sketch a simple common-emitter amplifier circuit and discuss the general ac circuit characteristics (voltage gain, current gain, input and output resistances).
8. What are the changes in the ac characteristics of a common-emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design?
9. Discuss the concepts of a dc load line and an ac load line.
10. Sketch a simple emitter-follower amplifier circuit and discuss the general ac circuit characteristics (voltage gain, current gain, input and output resistances).
11. Sketch a simple common-base amplifier circuit and discuss the general ac circuit characteristics (voltage gain, current gain, input and output resistances).
12. Compare the ac circuit characteristics of the common-emitter, emitter-follower, and common-base circuits.
13. Discuss the general conditions under which a common-emitter amplifier, an emitter-follower amplifier, and a common-base amplifier would be used in an electronic circuit design.
14. State at least two reasons why a multistage amplifier circuit would be required in a design rather than a single-stage circuit.
15. If a transistor circuit provides signal power gain, discuss the source of this additional signal power.

PROBLEMS

[Note: In the following problems, assume that the B–E turn-on voltage is 0.7 V for both npn and pnp transistors and that $V_A = \infty$ unless otherwise stated. Also assume that all capacitors act as short circuits to the signal.]

Section 6.2 The Bipolar Linear Amplifier

6.1 (a) If the transistor parameters are $\beta = 180$ and $V_A = 150$ V, and it is biased at $I_{CQ} = 2$ mA, determine the values of g_m, r_π, and r_o. (b) Repeat part (a) if $I_{CQ} = 0.5$ mA.

6.2 (a) A transistor with parameters $\beta = 120$ and $V_A = 120$ V is biased at a collector current of $I_{CQ} = 0.80$ mA. Determine the values of g_m, r_π, and r_o. (b) Repeat part (a) for $I_{CQ} = 80\ \mu$A.

6.3 The transistor parameters are $\beta = 125$ and $V_A = 200$ V. A value of $g_m = 200$ mA/V is desired. Determine the collector current required, and then find r_π and r_o.

6.4 A particular amplifier design application requires a value of $g_m = 80$ mA/V and $r_\pi = 1.20$ kΩ. What is the necessary dc collector current and transistor current gain β?

6.5 For the circuit in Figure 6.3, the transistor parameters are $\beta = 120$ and $V_A = \infty$, and the circuit parameters are $V_{CC} = 5$ V, $R_C = 4$ kΩ, $R_B = 250$ kΩ, and $V_{BB} = 2.0$ V. (a) Determine the hybrid-π parameter values of g_m, r_π, and r_o. (b) Find the small-signal voltage gain $A_v = v_o/v_s$. (c) If the time-varying output signal is given by $v_o = 0.8\sin(100t)$ V, what is v_s?

6.6 The nominal quiescent collector current of a transistor is 1.2 mA. If the range of β for this transistor is $80 \le \beta \le 120$ and if the quiescent collector current changes by ±10 percent, determine the range in values for g_m and r_π.

6.7 For the circuit in Figure 6.3, $\beta = 120$, $V_{CC} = 5$ V, $V_A = 100$ V, and $R_B = 25$ kΩ. (a) Determine V_{BB} and R_C such that $r_\pi = 5.4$ kΩ and the Q-point is in the center of the load line. (b) Find the resulting small-signal voltage gain $A_v = v_o/v_s$.

6.8 For the circuit in Figure 6.14, $\beta = 100$, $V_A = \infty$, $V_{CC} = 10$ V, and $R_B = 50$ kΩ. (a) Determine V_{BB} and R_C such that $I_{CQ} = 0.5$ mA and the Q-point is in the center of the load line. (b) Find the small-signal parameters g_m, r_π, and r_o. (c) Determine the small-signal voltage gain $A_v = v_o/v_s$.

6.9 The circuit in Figure 6.3 is biased at $V_{CC} = 10$ V and has a collector resistor of $R_C = 4$ kΩ. The voltage V_{BB} is adjusted such that $V_C = 4$ V. The transistor has $\beta = 100$. The signal voltage between the base and emitter is $v_{be} = 5\sin\omega t$(mV). Determine the total instantaneous values of $i_B(t)$, $i_C(t)$, and $v_C(t)$, and determine the small-signal voltage gain $A_v = v_c(t)/v_{be}(t)$.

6.10 The ac equivalent circuit shown in Figure 6.7 has $R_C = 2$ kΩ. The transistor parameters are $g_m = 50$ mA/V and $\beta = 100$. The time-varying output voltage is given by $v_o = 1.2\sin\omega t$ (V). Determine $v_{be}(t)$ and $i_b(t)$.

Section 6.4 Common-Emitter Amplifier

6.11 The parameters of the transistor in the circuit in Figure P6.11 are $\beta = 150$ and $V_A = \infty$. (a) Determine R_1 and R_2 to obtain a bias-stable circuit with the Q-point in the center of the load line. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$.

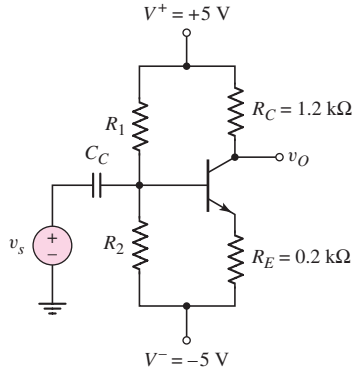


Figure P6.11

6.12 Assume that $\beta = 100$, $V_A = \infty$, $R_1 = 10\ \text{k}\Omega$, and $R_2 = 50\ \text{k}\Omega$ for the circuit in Figure P6.12. (a) Plot the Q-point on the dc load line. (b) Determine the small-signal voltage gain. (c) Determine the range of voltage gain if each resistor value varies by ± 5 percent.

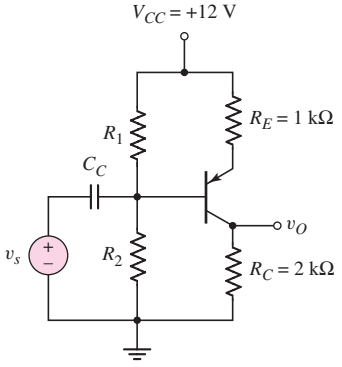


Figure P6.12

D6.13 The transistor parameters for the circuit in Figure P6.12 are $\beta = 100$ and $V_A = \infty$. (a) Design the circuit such that it is bias stable and that the Q-point is in the center of the load line. (b) Determine the small-signal voltage gain of the designed circuit.

D6.14 For the circuit in Figure P6.14, the transistor parameters are $\beta = 100$ and $V_A = \infty$. Design the circuit such that $I_{CQ} = 0.25$ mA and $V_{CEQ} = 3$ V. Find the small-signal voltage gain $A_v = v_o/v_s$. Find the input resistance seen by the signal source v_s.

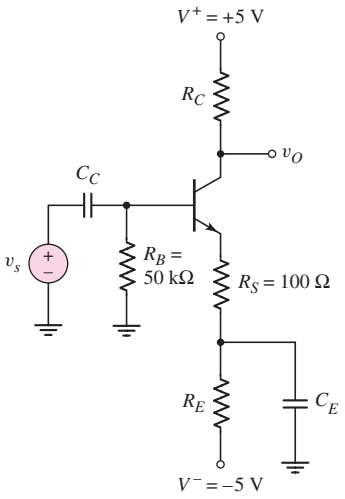


Figure P6.14

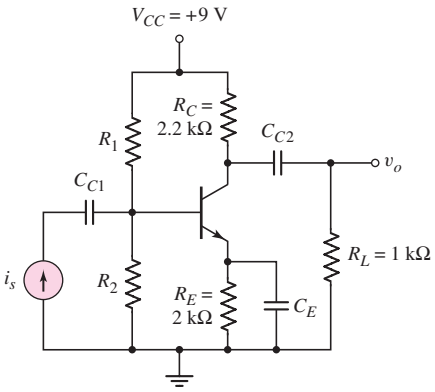


Figure P6.15

D6.15 Assume the transistor in the circuit in Figure P6.15 has parameters $\beta = 120$ and $V_A = 100$ V. (a) Design the circuit such that $V_{CEQ} = 3.75$ V. (b) Determine the small-signal transresistance $R_m = v_o/i_s$.

D6.16 For transistor parameters $\beta = 65$ and $V_A = 75$ V, (a) design the circuit in Figure P6.16 such that the dc voltages at the base and collector terminals are 0.30 V and −3 V, respectively. (b) Determine the small-signal transconductance $G_f = i_o/v_s$.

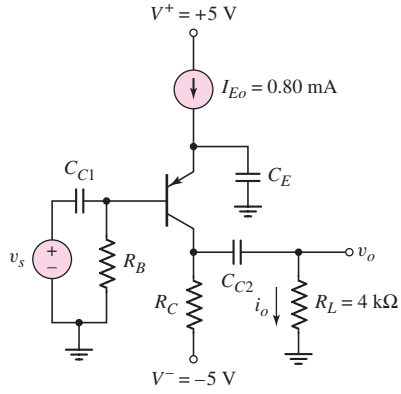


Figure P6.16

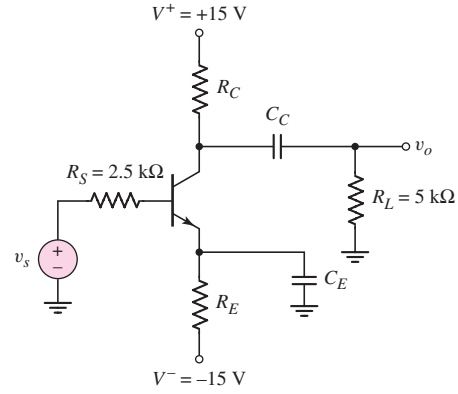


Figure P6.17

6.17 The source in Figure P6.17 is $v_s = 5 \sin \omega t$ (mV). The transistor has a current gain of $\beta = 120$. (a) Design the circuit such that $I_{CQ} = 0.8$ mA and $V_{CEQ} = 7$ V. Find the voltage gain $A_v = v_o/v_s$. (b) Repeat part (a) for $R_S = 0$.

6.18 Consider the circuit shown in Figure P6.18 where $v_s = 4 \sin \omega t$ (mV). Assume $\beta = 80$. (a) Determine $v_o(t)$ and $i_o(t)$. What are the small-signal voltage and current gains? (b) Repeat part (a) for $R_S = 0$.

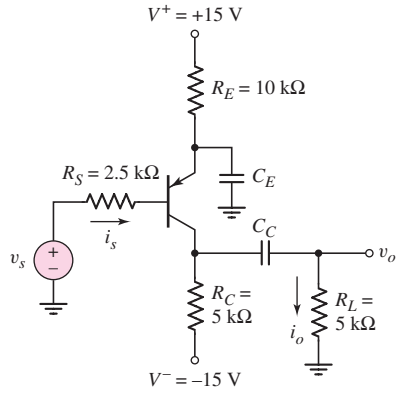


Figure P6.18

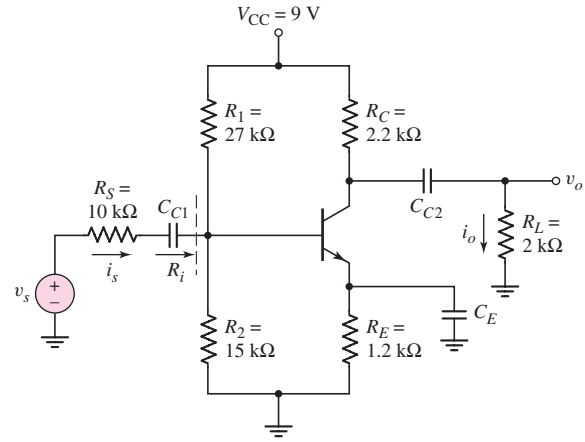


Figure P6.19

6.19 Consider the circuit shown in Figure P6.19. The transistor parameters are $\beta = 100$ and $V_A = 100$ V. Determine R_i, $A_v = v_o/v_s$, and $A_i = i_o/i_s$.

6.20 The parameters of the transistor in the circuit in Figure P6.20 are $\beta = 100$ and $V_A = 100$ V. (a) Find the dc voltages at the base and emitter terminals. (b) Find R_C such that $V_{CEQ} = 3.5$ V. (c) Assuming C_C and C_E act as short circuits, determine the small-signal voltage gain $A_v = v_o/v_s$. (d) Repeat part (c) if a 500 Ω source resistor is in series with the v_s signal source.

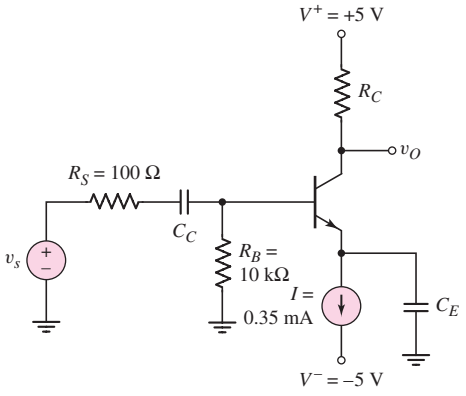


Figure P6.20

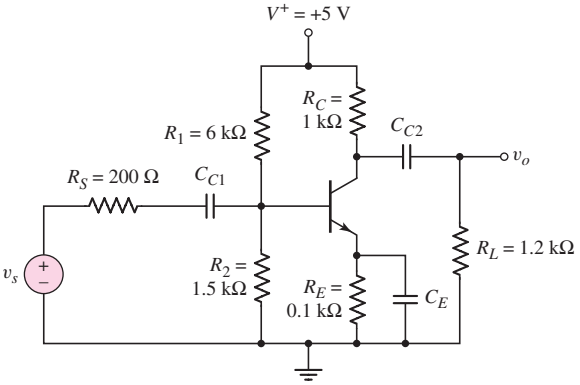


Figure P6.21

6.21 For the circuit in Figure P6.21, the transistor parameters are $\beta = 180$ and $r_o = \infty$. (a) Determine the Q-point values. (b) Find the small-signal hybrid-π parameters. (c) Find the small-signal voltage gain $A_v = v_o/v_s$.

6.22 For the circuit in Figure P6.22, the transistor parameters are $\beta = 80$ and $V_A = 80$ V. (a) Determine R_E such that $I_{EQ} = 0.75$ mA. (b) Determine R_C such that $V_{ECQ} = 7$ V. (c) For $R_L = 10\,\text{k}\Omega$, determine the small-signal voltage gain $A_v = v_o/v_s$. (d) Determine the impedance seen by the signal source v_s.

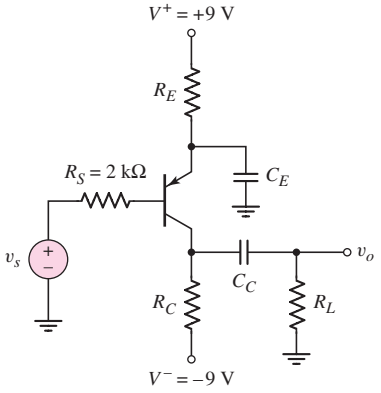


Figure P6.22

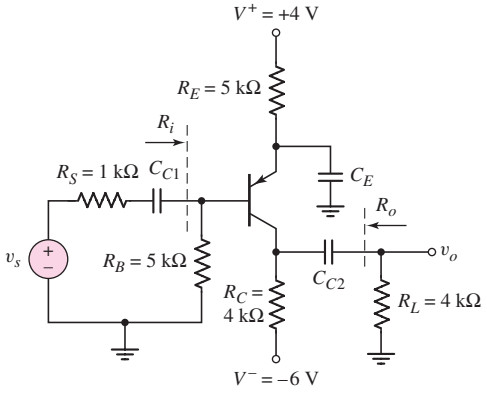


Figure P6.23

6.23 The transistor in the circuit in Figure P6.23 is a 2N2907A with a nominal dc current gain of $\beta = 100$. Assume the range of h_{fe} is $80 \le h_{fe} \le 120$ and the range of h_{oe} is $10 \le h_{oe} \le 20\ \mu$S. For $h_{re} = 0$ determine: (a) the range of small-signal voltage gain $A_v = v_o/v_s$, and (b) the range in the input and output resistances R_i and R_o.

D6.24 Design a one-transistor common-emitter preamplifier that can amplify a 10 mV (rms) microphone signal and produce a 0.5 V (rms) output signal. The source resistance of the microphone is 1 kΩ. Use standard resistor values in the design and specify the value of β required.

6.25 For the transistor in the circuit in Figure P6.25, the parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the Q-point. (b) Find the small-signal parameters g_m, r_π, and r_o. (c) Find the small-signal voltage gain $A_v = v_o/v_s$ and the small-signal current gain $A_i = i_o/i_s$. (d) Find the input resistances R_{ib} and R_{is}. (e) Repeat part (c) if $R_S = 0$.

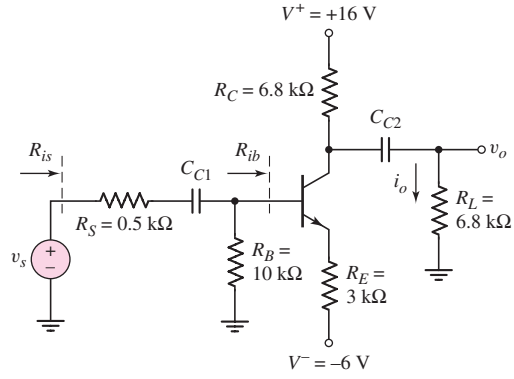


Figure P6.25

6.26 If the collector of a transistor is connected to the base terminal, the transistor continues to operate in the forward-active mode, since the B–C junction is not reverse biased. Determine the small-signal resistance, $r_e = v_{ce}/i_e$, of this two-terminal device in terms of g_m, r_π, and r_o.

D6.27 Design an amplifier with the configuration similar to that shown in Figure 6.31. The source resistance is $R_S = 100\,\Omega$ and the voltage gain should be approximately -10. The total power dissipated in the circuit should be no more than approximately 0.12 mW. Specify the required value of β.

D6.28 An ideal signal voltage source is given by $v_s = 5\sin(5000t)$ (mV). The peak current that can be supplied by this source is 0.2 μA. The desired output voltage across a 10 kΩ load resistor is $v_o = 100\sin(5000t)$ (mV). Design a one-transistor common-emitter amplifier to meet this specification. Use standard resistor values and specify the required value of β.

D6.29 Design a bias-stable common-emitter circuit that has a minimum open-circuit small-signal voltage gain of $|A_v| = 10$. The circuit is to be biased from a single power supply $V_{CC} = 10$ V that can supply a maximum current of 1 mA. The available transistors are pnp's with $\beta = 80$ and $V_A = \infty$. Minimize the number of capacitors required in the circuit.

D6.30 Design a common-emitter circuit whose output is capacitively coupled to a load resistor $R_L = 10\,\text{k}\Omega$. The minimum small-signal voltage gain is to be $|A_v| = 50$. The circuit is to be biased at ± 5 V and each voltage source can supply a maximum of 0.5 mA. The parameters of the available transistors are $\beta = 120$ and $V_A = \infty$.

Section 6.5 AC Load Line Analysis

6.31 For the circuit in Figure P6.12 with circuit and transistor parameters as described in Problem 6.12, determine the maximum undistorted swing in the output voltage if the total instantaneous E–C voltage is to remain in the range $1 \le v_{EC} \le 11$ V.

6.32 For the circuit in Figure P6.14, let $\beta = 100$, $V_A = \infty$, $R_E = 12.9\ \text{k}\Omega$, and $R_C = 6\ \text{k}\Omega$. Determine the maximum undistorted swing in the output voltage if the total instantaneous C–E voltage is to remain in the range $1 \leq v_{CE} \leq 9$ V and if the total instantaneous collector current is to remain greater or equal to 50 μA.

6.33 Consider the circuit in Figure P6.18. (a) Determine the maximum undistorted swing in the output voltage if the total instantaneous C–E voltage is to remain in the range $2 \leq v_{EC} \leq 12$ V. (b) Using the results of part (a), determine the range of collector current.

6.34 Consider the circuit in Figure P6.16. Let $\beta = 100$, $V_A = \infty$, $R_B = 10\ \text{k}\Omega$, and $R_C = 4\ \text{k}\Omega$. Determine the maximum undistorted swing in the output current i_o if the total instantaneous collector current is $i_C \geq 0.08$ mA and the total instantaneous E–C voltage is in the range $1 \leq v_{EC} \leq 9$ V.

6.35 Consider the circuit in Figure P6.25 with transistor parameters described in Problem 6.25. Determine the maximum undistorted swing in the output current i_C if the total instantaneous collector current is $i_C \geq 0.1$ mA and the total instantaneous C–E voltage is in the range $1 \leq v_{CE} \leq 21$ V.

6.36 For the circuit in Figure P6.19, the transistor parameters are $\beta = 100$ and $V_A = 100$ V. The values of R_C, R_E, and R_L are as shown in the figure. Design a bias-stable circuit to achieve the maximum undistorted swing in the output voltage if the total instantaneous C–E voltage is to remain in the range $1 \leq v_{CE} \leq 8$ V and the minimum collector current is to be $i_C(\text{min}) = 0.1$ mA.

6.37 In the circuit in Figure P6.21 with transistor parameters $\beta = 180$ and $V_A = \infty$, redesign the bias resistors R_1 and R_2 to achieve maximum symmetrical swing in the output voltage and to maintain a bias-stable circuit. The total instantaneous C–E voltage is to remain in the range $0.5 \leq v_{CE} \leq 4.5$ V and the total instantaneous collector current is to be $i_C \geq 0.25$ mA.

6.38 For the circuit in Figure P6.23, the transistor parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the maximum undistorted swing in the output voltage if the total instantaneous E–C voltage is to remain in the range $1 \leq v_{EC} \leq 9$ V. (b) Using the results of part (a), determine the range of collector current.

Section 6.6 Common-Collector (Emitter-Follower) Amplifier

6.39 The transistor parameters for the circuit in Figure P6.39 are $\beta = 180$ and $V_A = \infty$. (a) Find I_{CQ} and V_{CEQ}. (b) Plot the dc and ac load lines. (c) Calculate the small-signal voltage gain. (d) Determine the input and output resistances R_{ib} and R_o.

6.40 Consider the circuit in Figure P6.40. The transistor parameters are $\beta = 120$ and $V_A = \infty$. Repeat parts (a)–(d) of Problem 6.39.

6.41 For the circuit shown in Figure P6.41, let $V_{CC} = 5$ V, $R_L = 4\ \text{k}\Omega$, $R_E = 3\ \text{k}\Omega$, $R_1 = 60\ \text{k}\Omega$, and $R_2 = 40\ \text{k}\Omega$. The transistor parameters are $\beta = 50$ and $V_A = 80$ V. (a) Determine I_{CQ} and V_{ECQ}. (b) Plot the dc and ac load lines. (c) Determine $A_v = v_o/v_s$ and $A_i = i_o/i_s$. (d) Determine R_{ib} and R_o. (e) Determine the range in current gain if each resistor value varies by ± 5 percent.

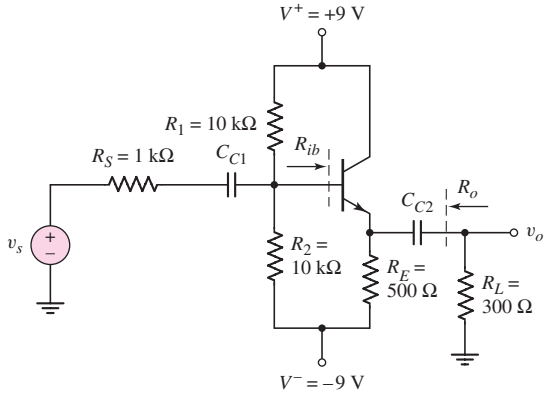


Figure P6.39

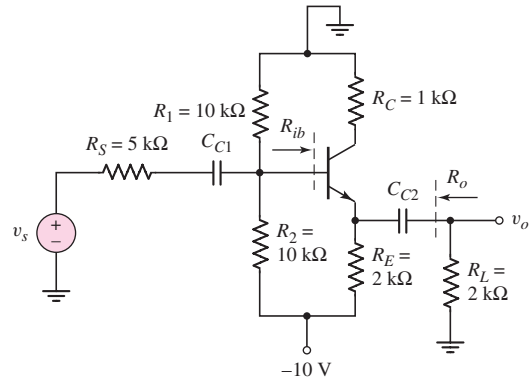


Figure P6.40

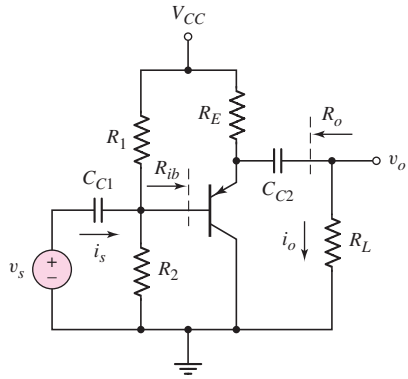


Figure P6.41

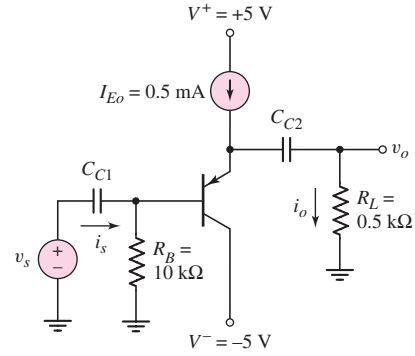


Figure P6.42

6.42 For the transistor in Figure P6.42, $\beta = 80$ and $V_A = 150$ V. (a) Determine the dc voltages at the base and emitter terminals. (b) Calculate the small-signal parameters g_m, r_π, and r_o. (c) Determine the small-signal voltage gain and current gain. (d) Repeat part (c) if a 2 kΩ source resistor is in series with the v_s signal source.

6.43 Consider the emitter-follower amplifier shown in Figure P6.43. The transistor parameters are $\beta = 100$ and $V_A = 100$ V. (a) Find the output resistance R_o. (b) Determine the small-signal voltage gain for (i) $R_L = 500\ \Omega$ and (ii) $R_L = 5$ kΩ.

6.44 The signal source in the circuit shown in Figure P6.44 is given by $v_s = 2 \sin \omega t$ (V). The transistor parameter is $\beta = 125$. (a) Determine R_{ib} and R_o. (b) Determine $i_s(t)$, $i_o(t)$, $v_o(t)$, and $v_{eb}(t)$.

D6.45 For the transistor in Figure P6.45, the parameters are $\beta = 100$ and $V_A = \infty$. (a) Design the circuit such that $I_{EQ} = 1$ mA and the Q-point is in the center of the dc load line. (b) If the peak-to-peak sinusoidal output voltage is 4 V, determine the peak-to-peak sinusoidal signals at the base of the transistor and the peak-to-peak value of v_s. (c) If a load resistor $R_L = 1\,\text{k}\Omega$ is connected to the output through a coupling capacitor, determine the peak-to-peak value in the output voltage, assuming v_s is equal to the value determined in part (b).

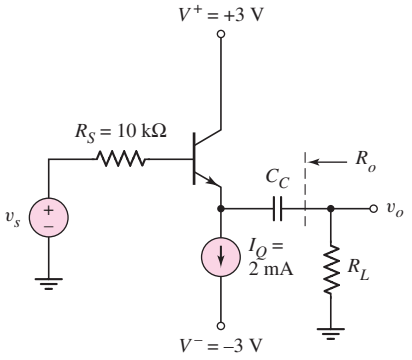


Figure P6.43

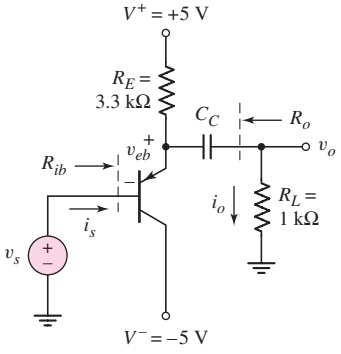


Figure P6.44

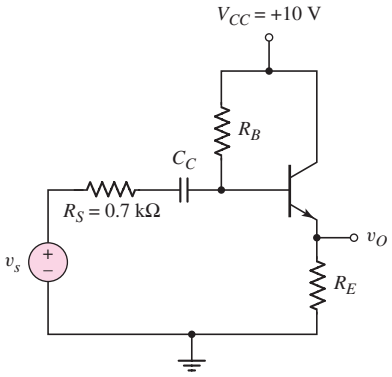


Figure P6.45

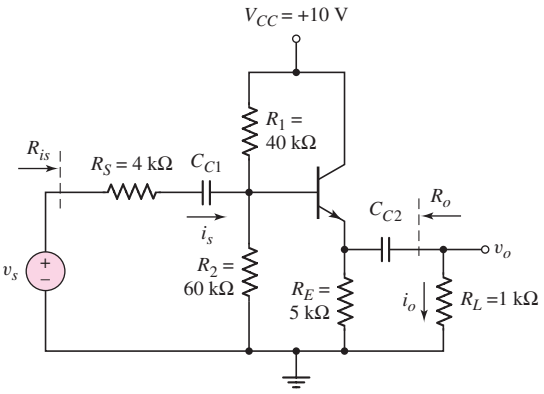


Figure P6.46

6.46 In the circuit shown in Figure P6.46, determine the range in small-signal voltage gain $A_v = v_o/v_s$ and current gain $A_i = i_o/i_s$ if β is in the range $75 \leq \beta \leq 150$.

6.47 The transistor current gain β in the circuit shown in Figure P6.47 is in the range $50 \leq \beta \leq 200$. (a) Determine the range in the dc values of I_E and V_E. (b) Determine the range in the values of input resistance R_i and voltage gain $A_v = v_o/v_s$.

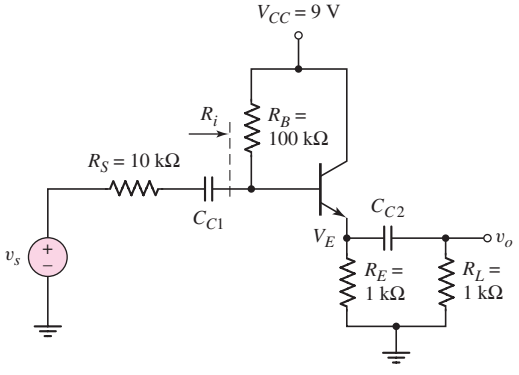


Figure P6.47

6.48 Consider the circuit shown in Figure P6.42. The transistor current gain is in the range $100 \leq \beta \leq 180$ and the Early voltage is $V_A = 150$ V. Determine the range in small-signal voltage gain if the load resistance varies from $R_L = 0.5\,\text{k}\Omega$ to $R_L = 500\,\text{k}\Omega$.

*D6.49 For the circuit in Figure P6.49, the transistor current gain is $\beta = 80$ and $R_L = 500\,\Omega$. Design the circuit to obtain a small-signal current gain of $A_i = i_o/i_s = 8$. Let $V_{CC} = 10$ V. Find R_1, R_2, and the output resistance R_o if $R_E = 500\,\Omega$. What is the current gain if $R_L = 2000\,\Omega$?

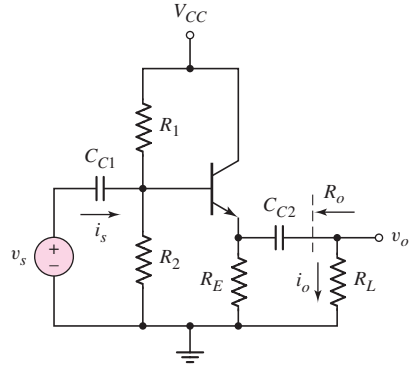


Figure P6.49

D6.50 Design an emitter-follower circuit with the configuration shown in Figure 6.52 such that the input resistance R_i, as defined in Figure 6.54, is 120 kΩ. Assume transistor parameters of $\beta = 120$ and $V_A = \infty$. Let $V_{CC} = 5$ V and $R_E = 2\,\text{k}\Omega$. Find new values of R_1 and R_2. The Q-point should be approximately in the center of the load line.

D6.51 (a) For the emitter-follower circuit in Figure P6.49, assume $V_{CC} = 24$ V, $\beta = 75$, and $A_i = i_o/i_s = 8$. Design the circuit to drive an 8 Ω load. (b) Determine the maximum undistorted swing in the output voltage. (c) Determine the output resistance R_o.

*D6.52 The output of an amplifier can be represented by $v_s = 4\sin\omega t$ (V) and $R_S = 4\,\text{k}\Omega$. An emitter-follower circuit, with the configuration shown in Figure 6.57, is to be designed such that the output signal does not vary by more than 5 percent when a load in the range $R_L = 4$ to $10\,\text{k}\Omega$ is connected to the output. The transistor current gain is in the range $90 \leq \beta \leq 130$ and the Early voltage is $V_A = \infty$. For your design, find the minimum and maximum possible value of the output voltage.

*D6.53 An emitter-follower amplifier, with the configuration shown in Figure 6.57, is to be designed such that an audio signal given by $v_s = 5\sin(3000t)$ V but with a source resistance of $R_S = 10\,\text{k}\Omega$ can drive a small speaker. Assume the supply voltages are $V^+ = +12$ V and $V^- = -12$ V. The load, representing the speaker, is $R_L = 12\,\Omega$. The amplifier should be capable of delivering approximately 1 W of average power to the load. What is the signal power gain of your amplifier?

Section 6.7 Common-Base Amplifier

6.54 For the circuit shown in Figure P6.54, $\beta = 125$, $V_A = \infty$, $V_{CC} = 18$ V, $R_L = 4\,\text{k}\Omega$, $R_E = 3\,\text{k}\Omega$, $R_C = 4\,\text{k}\Omega$, $R_1 = 25.6\,\text{k}\Omega$, and $R_2 = 10.4\,\text{k}\Omega$.

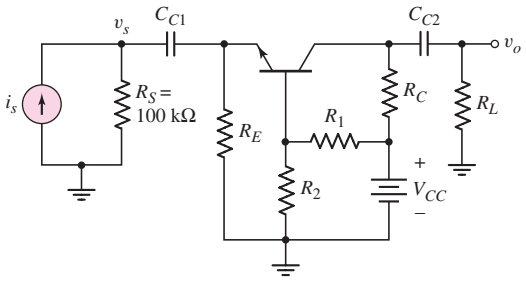


Figure P6.54

The input signal is a current. (a) Determine the Q-point values. (b) Determine the transresistance $R_m = v_o/i_s$. (c) Find the small-signal voltage gain $A_v = v_o/v_s$.

*D6.55 For the common-base circuit shown in Figure P6.54, let $\beta = 100$, $V_A = \infty$, $V_{CC} = 12$ V, $R_L = 12\,\text{k}\Omega$, and $R_E = 500\,\Omega$. (a) Redesign the circuit such that the small-signal voltage gain is $A_v = v_o/v_s = 10$. (b) What are the Q-point values? (c) What is the small-signal voltage gain if R_2 is bypassed by a large capacitor?

6.56 For the circuit shown in Figure P6.56, the transistor parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the dc voltages at the collector, base, and emitter terminals. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$. (c) Find the input resistance R_i.

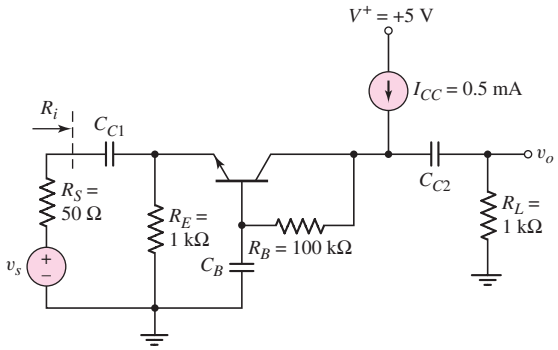


Figure P6.56

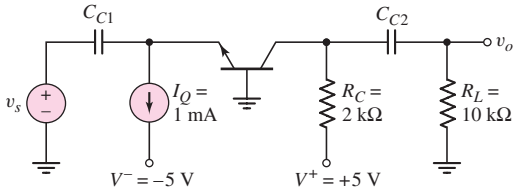


Figure P6.57

6.57 Consider the common-base circuit in Figure P6.57. The transistor has parameters $\beta = 120$ and $V_A = \infty$. (a) Determine the quiescent V_{CEQ}. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$.

6.58 The transistor in the circuit shown in Figure P6.58 has $\beta = 100$ and $V_A = \infty$. (a) Determine the quiescent values I_{CQ} and V_{ECQ}. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$.

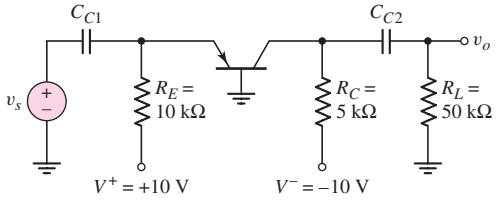


Figure P6.58

6.59 Repeat Problem 6.58 with a 100 Ω resistor in series with the v_s signal source.

6.60 Consider the circuit shown in Figure P6.60. The transistor has parameters $\beta = 60$ and $V_A = \infty$. (a) Determine the quiescent values of I_{CQ} and V_{CEQ}. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$.

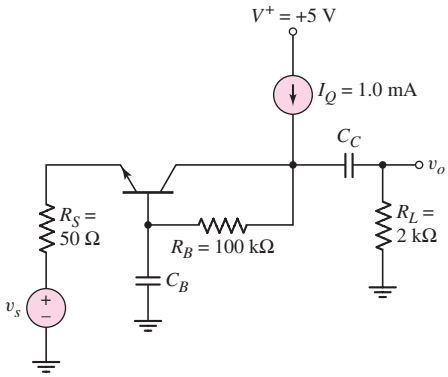


Figure P6.60

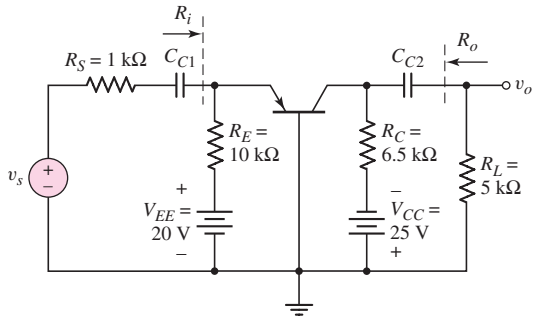


Figure P6.62

*D6.61 A photodiode in an optical transmission system, such as shown in Figure 1.35, can be modeled as a Norton equivalent circuit with i_s in parallel with R_S as shown in Figure P6.54. Assume that the current source is given by $i_s = 2.5 \sin \omega t\, \mu$A and $R_S = 50$ kΩ. Design the common-base circuit of Figure P6.54 such that the output voltage is $v_o = 5 \sin \omega t$ mV. Assume transistor parameters of $\beta = 120$ and $V_A = \infty$. Let $V_{CC} = 5$ V.

6.62 In the common-base circuit shown in Figure P6.62, the transistor is a 2N2907A, with a nominal dc current gain of $\beta = 80$. (a) Determine I_{CQ} and V_{ECQ}. (b) Using the h-parameters (assuming $h_{re} = 0$), determine the range in small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the range in input and output resistances R_i and R_o.

*D6.63 In the circuit of Figure P6.62, let $V_{EE} = V_{CC} = 5$ V, $\beta = 100$, $V_A = \infty$, $R_L = 1$ kΩ, and $R_S = 0$. (a) Design the circuit such that the small-signal voltage gain is $A_v = v_o/v_s = 25$ and $V_{ECQ} = 3$ V. (b) What are the values of the small-signal parameters g_m, r_π, and r_o?

Section 6.9 Multistage Amplifiers

*6.64 The parameters for each transistor in the circuit shown in Figure P6.64 are $\beta = 100$ and $V_A = \infty$. (a) Determine the small-signal parameters g_m, r_π, and r_o for both transistors. (b) Determine the small-signal voltage gain $A_{v1} = v_{o1}/v_s$, assuming v_{o1} is connected to an open circuit, and determine the gain $A_{v2} = v_o/v_{o1}$. (c) Determine the overall small-signal voltage gain $A_v = v_o/v_s$. Compare the overall gain with the product $A_{v1} \cdot A_{v2}$, using the values calculated in part (b).

*6.65 Consider the circuit shown in Figure P6.65 with transistor parameters $\beta = 120$ and $V_A = \infty$. (a) Determine the small-signal parameters g_m, r_π, and r_o for both transistors. (b) Plot the dc and ac load lines for both transistors. (c) Determine the overall small-signal voltage gain $A_v = v_o/v_s$.

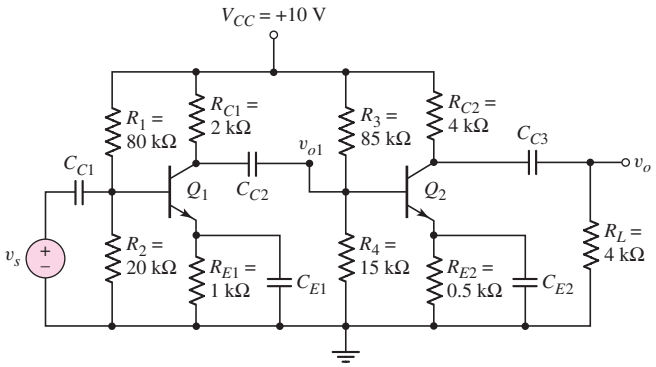


Figure P6.64

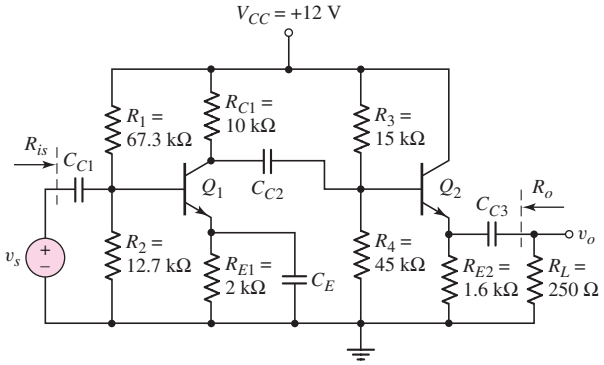


Figure P6.65

(d) Determine the input resistance R_{is} and the output resistance R_o. (e) Determine the maximum undistorted swing in the output voltage.

6.66 For the circuit shown in Figure P6.66, assume transistor parameters of $\beta = 100$ and $V_A = \infty$. (a) Determine the dc collector current in each transistor. (b) Find the small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the input and output resistances R_{ib} and R_o.

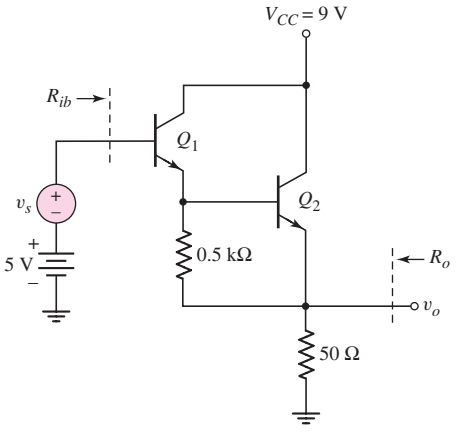


Figure P6.66

*6.67 For each transistor in Figure P6.67, the parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the Q-point values for both Q_1 and Q_2. (b) Determine the overall small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the input and output resistances R_{is} and R_o.

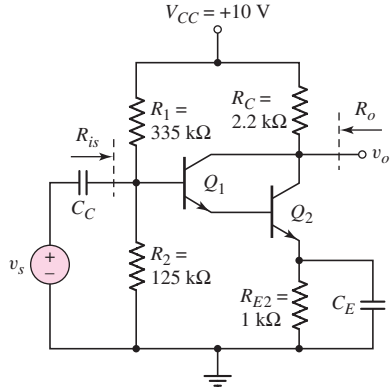


Figure P6.67

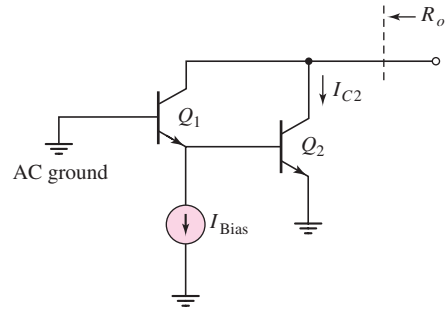


Figure P6.68

6.68 An equivalent ac circuit of a Darlington pair configuration is shown in Figure P6.68. (a) Derive the expression for the output resistance R_o as a function of I_{Bias} and I_{C2}. Take into account the transistor output resistances r_{o1} and r_{o2}. (b) Assuming transistor parameters of $\beta = 100$ and $V_A = 100$ V, determine R_o for (i) $I_{C2} = I_{\text{Bias}} = 1$ mA and (ii) $I_{C2} = 1$ mA, $I_{\text{Bias}} = 0$.

Section 6.10 Power Considerations

6.69 The transistor in the circuit shown in Figure 6.28 has parameters $\beta = 100$ and $V_A = 100$ V. (a) Determine the average power dissipated in the transistor and R_C, for $v_s = 0$. (b) Determine the maximum undistorted signal power that can be delivered to R_C.

6.70 Consider the circuit shown in Figure 6.40. The transistor parameters are $\beta = 120$ and $r_o = \infty$. (a) Calculate the average power dissipated in the transistor, R_E, and R_C, for $v_s = 0$. (b) Determine the maximum undistorted signal power that can be delivered to R_C.

6.71 For the circuit shown in Figure 6.45, use the circuit and transistor parameters described in Example 6.10. (a) Calculate the average power dissipated in the transistor, R_E, and R_C, for $v_s = 0$. (b) Determine the maximum signal power that can be delivered to R_L. What are the signal powers dissipated in R_E and R_C, and what is the average power dissipated in the transistor in this case?

6.72 For the circuit shown in Figure 6.60, the transistor parameters are $\beta = 100$ and $V_A = 100$ V, and the source resistor is $R_S = 0$. Determine the maximum undistorted signal power that can be delivered to R_L if: (a) $R_L = 1$ kΩ, and (b) $R_L = 10$ kΩ.

6.73 Consider the circuit shown in Figure 6.67 with parameters given in Exercise TYU6.14. (a) Calculate the average power dissipated in the transistor and R_C, for $v_s = 0$. (b) Determine the maximum undistorted signal power that can be delivered to R_L, and the resulting average power dissipated in the transistor and R_C.

COMPUTER SIMULATION PROBLEMS

6.74 Consider Example 6.2. Using a computer simulation analysis, investigate the effect of the Early voltage on the small-signal characteristics of the circuit.

6.75 The circuit in Figure P6.75 can be used to simulate the circuit shown in Figure 6.42(c). Assume Early voltages of $V_A = 60$ V. (a) Plot the voltage transfer characteristics, v_O versus V_{BB}, over the range $0 \leq V_{BB} \leq 1$ V. (b) Set V_{BB} such that the dc value of the output voltage is $v_O \cong 2.5$ V. Determine the small-signal voltage gain at this Q-point. Compare the results to those found in Example 6.9.

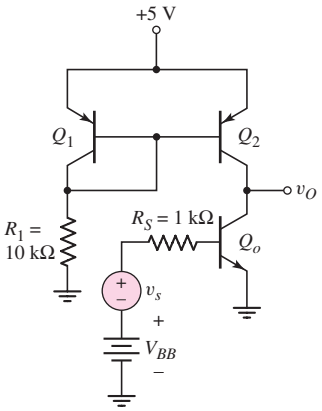


Figure P6.75

6.76 Verify the results of Example 6.10 with a computer simulation analysis.

6.77 Verify the input and output resistances of the emitter-follower circuit described in Example 6.14.

6.78 Perform a computer simulation analysis of the common-base circuit described in Exercise TYU6.14. In addition, assume $V_A = 80$ V and determine the output resistance looking into the collector of the transistor. How does this value compare to $r_o = V_A / I_{CQ}$?

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer simulation.]

*D6.79 Design a common-emitter circuit with a small-signal voltage gain of $|A_v| = 50$ while driving a load $R_L = 5\,\text{k}\Omega$. The source signal is $v_s = 0.02 \cos \omega t$ V and the source resistance is $R_S = 1\,\text{k}\Omega$. Bias the circuit at ± 5 V, and use transistors with a maximum collector current rating of 10 mA and current gains in the range $80 \leq \beta \leq 150$.

*D6.80 For the circuit in Figure P6.41, let $V_{CC} = 10$ V and $R_L = 1\,\text{k}\Omega$. The transistor parameters are $\beta = 120$ and $V_A = \infty$. (a) Design the circuit such that the current gain is $A_i = 18$. (b) Determine R_{ib} and R_o. (c) Find the maximum undistorted swing in the output voltage.

*D6.81 Design a common-base amplifier with the general configuration shown in Figure 6.67. The available power supplies are ± 10 V. The output resistance

of the signal source is 50 Ω, and the input resistance of the amplifier should match this value. The output resistance is $R_L = 2\,\text{k}\Omega$, and the output voltage is to have the largest possible symmetrical swing. In order to maintain linearity, the peak value of the B–E signal voltage should be limited to 15 mV. Assume that transistors with $\beta = 150$ are available. Specify the current and power ratings of the transistors.

*D6.82 A microphone puts out a peak voltage of 1 mV and has an output resistance of 10 kΩ. Design an amplifier system to drive an 8 Ω speaker, producing 2 W of signal power. Use a 24 V power supply to bias the circuit. Assume a current gain of $\beta = 50$ for the available transistors. Specify the current and power ratings of the transistors.

*D6.83 Redesign the two-stage amplifier in Figure 6.69 such that a symmetrical sine wave with a peak value of ±3 V can be obtained at the output. The load resistor is still $R_L = 5\,\text{k}\Omega$. To avoid distortion, the minimum C–E voltage should be at least 1 V and the maximum C–E voltage should be no more than 9 V. Assume the transistor current gains are $\beta = 100$. If the Early voltage for each transistor is $V_A = \infty$, calculate the resulting overall small-signal voltage gain. State the value of each resistor and the quiescent values of each transistor.