CHAPTER

FOUR

OPERATIONAL-AMPLIFIER CIRCUITS

The *operational amplifier* (op amp) is an extremely versatile and inexpensive semiconductor device. It is the workhorse of the communication, control, and instrumentation industry.

For *low-frequency* applications, the op amp behaves like a *four-terminal nonlinear resistor* which can often be represented by an *ideal op-amp model*. This model greatly simplifies the analysis and design of op-amp circuits. In fact, one of the reasons why op amps are so popular is that, at low frequencies, they behave almost like the *ideal* model! Consequently, except in the last section, our methods of analysis in this chapter will be based on the *ideal* model. This choice is justified in Sec. 4 by analyzing a typical op-amp circuit (operating at low frequency) using a more complicated (*finite-gain*) op-amp model and then comparing the results with those predicted by the ideal op-amp model.

Depending on the *dynamic range* of the input signals, an op amp may operate in the *linear* or *nonlinear* region. Section 2 is devoted to those circuits where the op amp is operating only in the linear region. This restriction allows us to simplify the (nonlinear) ideal op-amp model into a *linear* model, called the *virtual short-circuit model*. This model is used exclusively in Sec. 2 for analyzing both simple circuits *by inspection*, as well as complicated circuits via a *systematic method*.

The organization in Sec. 2 is followed in Sec. 3 for op amps operating in the nonlinear region. Here, it is necessary to use the (nonlinear) ideal op-amp model.

1 DEVICE DESCRIPTION, CHARACTERISTICS, AND MODEL

Operational amplifiers (op amps) are multiterminal devices sold in several standard packages, two of which are shown in Figs. 1.1 and 1.2. Because they

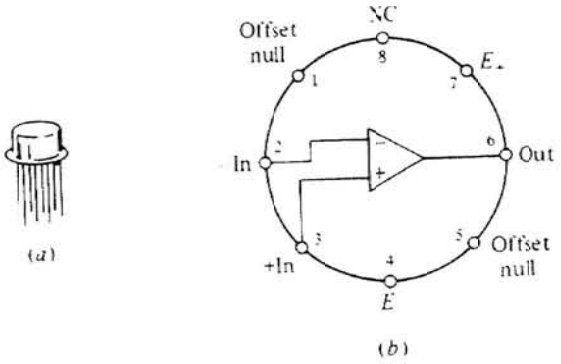


Figure 1.1 Eight-lead metal can. (*a*) Side view. (*b*) Top view.

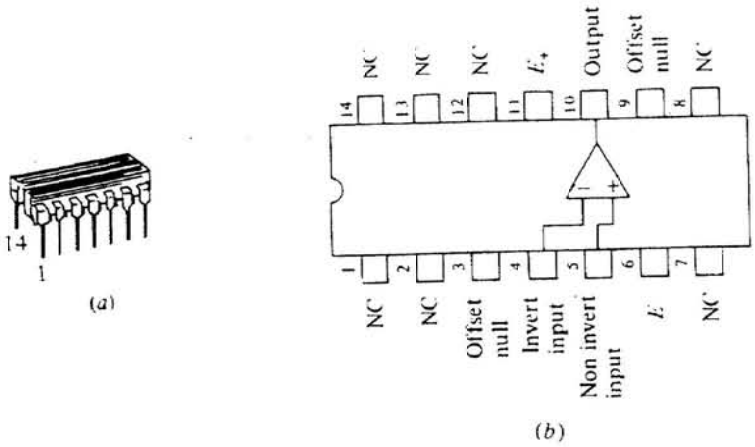


Figure 1.2 A 14-lead DIP (dual in-line package). (*a*) Side view (*b*) Top view.

are inexpensive (some cost less than 25 cents a piece), reliable, and extremely versatile, op amps have become the workhorse of the electronics industry.

Over 2000 types of integrated circuits (*IC*) op amps are currently available, each containing nearly two dozen transistors. Figure 1.3 gives the schematic of the popular μA741, a second-generation op amp introduced by Fairchild Semiconductor in 1968. The seven terminals brought out through the package leads are labeled *inverting input*, *noninverting input*, *output*, E_+, E_-, and *offset null* (two of them). The remaining terminals of the package in Figs. 1.1*b* and 1.2*b* not connected to the *IC* are labeled *NC* (for no connection).

Some op amps have more than seven terminals; others have less. For most applications, however, only the five terminals indicated in the standard op-amp symbol in Fig. 1.4*a* are essential. The additional terminals are usually connected to some external nulling or compensation circuit for improving the performance of the op amp. In order for the op amp to function properly its internal transistors must be biased at appropriate operating points. Terminals E_+ and E_- are provided for this purpose. In general, they are connected to a split power supply as shown in Fig. 1.4*b*, where E_+ and E_- denote the voltage with respect to the *external* ground. Typically, $E_+ = +15$ V and $E_- = -15$ V.

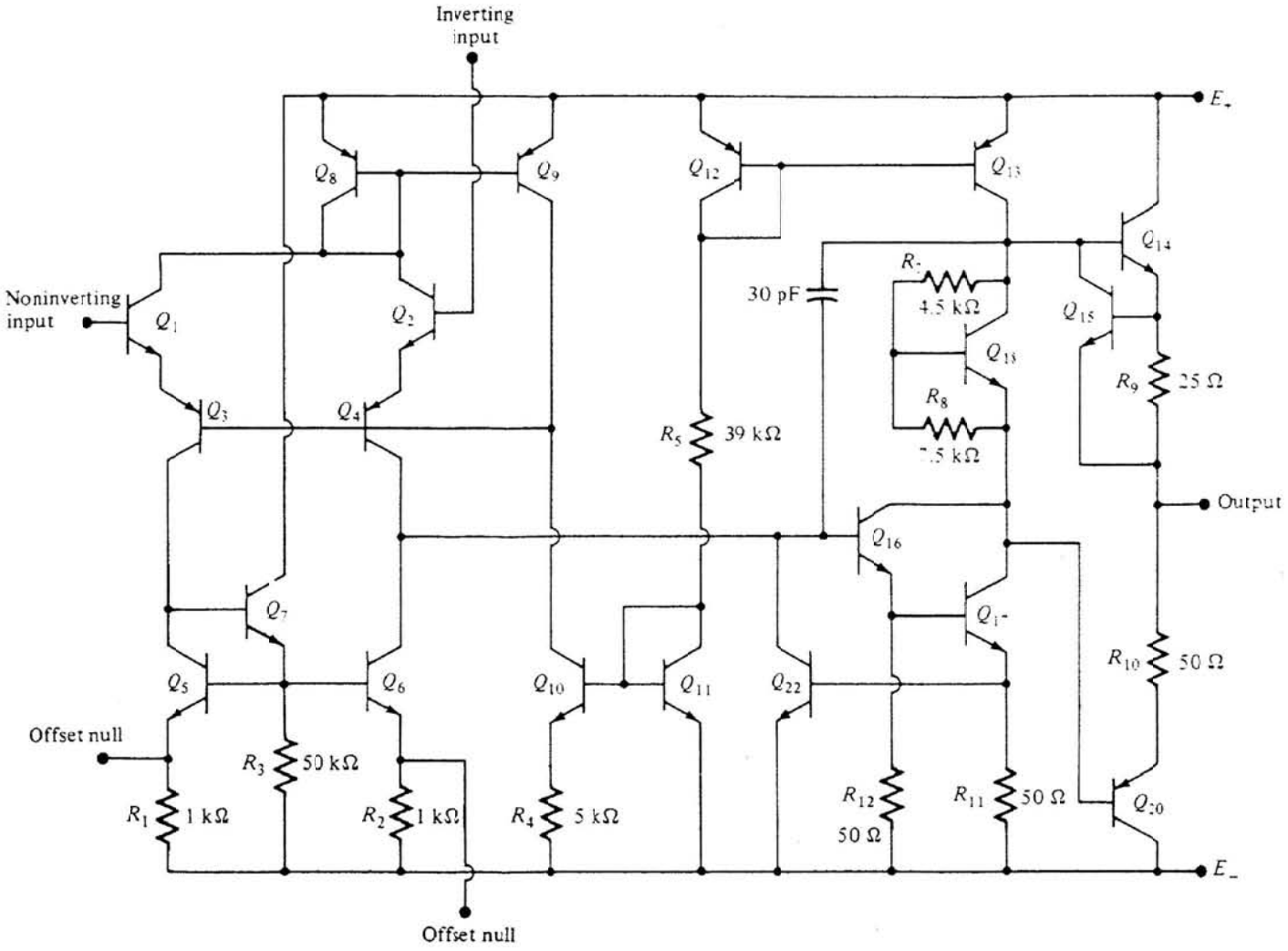


Figure 1.3 Schematic of the μA741 op amp.

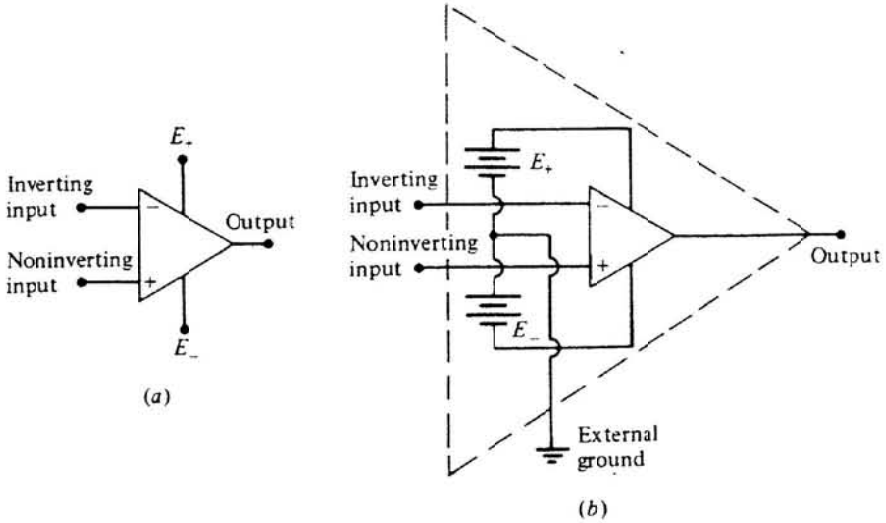


Figure 1.4 Standard op-amp symbol and a typical biasing scheme. (*a*) The − and + signs inside the triangle denote the inverting and noninverting input terminals, respectively. (*b*) A "biased" op amp (enclosed within the triangle) can be considered as a 4-terminal device for circuit analysis and design purposes.

After the power supply has been connected and after an external nulling and/or compensation circuit has been connected to any additional terminals, only four terminals are available for external connections. Hence, from the circuit designer's point of view, an op amp is really a *four-terminal device*, regardless of the original number of terminals in the op-amp package. This four-terminal device lies inside the dotted triangle in Fig. 1.4*b* and will henceforth be denoted by the symbol shown in Fig. 1.5*a*.[1] Here, i_- and i_+ denote the current entering the op-amp "inverting" and "noninverting" terminals, respectively. Similarly, v_-, v_+, and v_o denote respectively the voltage from the inverting terminal ⊖, noninverting terminal ⊕, and output terminal ⓞ to *ground*. The variable $v_d \triangleq v_+ - v_-$ is called the *differential input voltage* and will play an important role in op-amp circuit analysis.

To derive an exact characterization of an op amp would require analyzing the entire integrated circuit, such as the one shown in Fig. 1.3. Fortunately, for many low-frequency applications, the op-amp terminal currents and voltages have been found *experimentally* to obey the following *approximate* relationships:

$$\boxed{\begin{aligned} i_- &= I_{B-} \\ i_+ &= I_{B+} \\ v_o &= f(v_d) \end{aligned}} \tag{1.1}$$

where I_{B-} and I_{B-} are called the *input bias currents* and $f(v_d)$ denotes the v_o-vs.-v_d transfer characteristic. Apart from a scaling factor which depends on the power supply voltage, $f(v_d)$ follows approximately an odd-symmetric

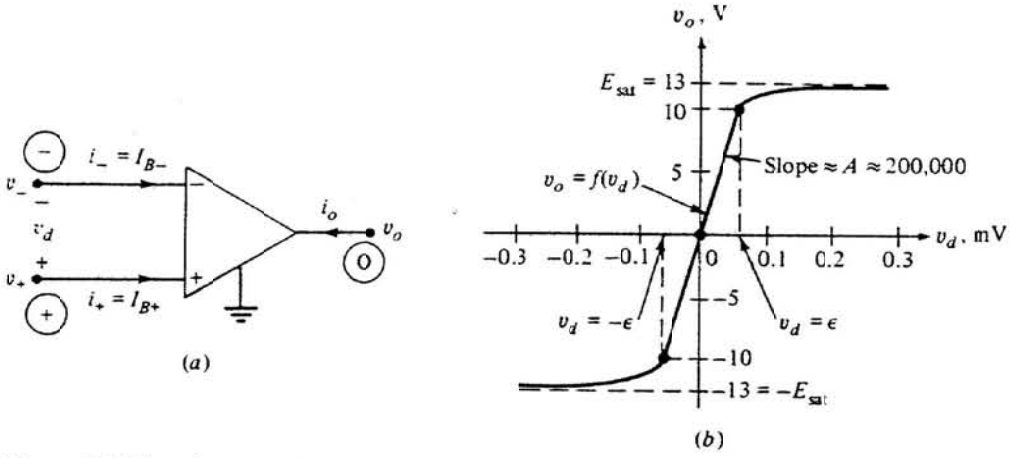


Figure 1.5 Experimental characterization of a typical op amp.

[1] The op-amp symbol given in most electronics literature shows only three terminals with the ground terminal omitted. This is because the ground terminal in Fig. 1.4*b* does not exist physically as a pin in most modern op-amp packages, but is rather created externally through the dual power supply. We added this terminal because without it, KCL would give the erroneous relationship $i_- + i_+ + i_o = 0$.

function as shown in Fig. 1.5*b* (drawn for a ±15-V supply voltage). Moreover, this function has been found to be rather insensitive to changes in the output current i_o.

The transfer characteristic in Fig. 1.5*b* displays three remarkable properties:

1. v_o and v_d have different scales: one in volts, the other in millivolts.
2. In a small interval $-\epsilon < v_d < \epsilon$ of the origin, $f(v_d) \approx Av_d$ is nearly *linear* with a very steep slope A—called the *open-loop voltage gain.*
3. $f(v_d)$ *saturates* at $v_o = \pm E_{sat}$, where E_{sat} is typically 2 V less than the power supply voltage ($E_{sat} = 13$ V in Fig. 1.5*b*).

In most op amps using bipolar input transistors, such as in Fig. 1.3, I_{B-} and I_{B+} represent the dc *base* currents used to bias the transistors (typically, less than 0.2 mA). For op amps using FET input transistors, the input bias currents are much smaller. For example, the *average input bias current* $I_B \triangleq \frac{1}{2}(|I_{B+}| + |I_{B-}|)$ is equal to 0.1 mA for the μA741 but only 0.1 nA for the μA740 (which uses a pair of FET input transistors).

The open-loop voltage gain A is typically equal to at least 100,000 (200,000 for the μA741). On the other hand, the voltage ϵ at the end of the *linear* region in Fig. 1.5*b* is typically less than 0.1 mV.

An ideal op-amp model In view of the typical magnitudes of I_{B-}, I_{B+}, A, and ϵ, little accuracy is lost by assuming $I_{B-} = I_{B+} = \epsilon = 0$ and $A = \infty$. This simplifying assumption leads to the *ideal op-amp model* shown in Fig. 1.6*a* and *b*. Note that the transfer characteristic $f(v_d)$ in this *ideal* model has been approximated by a three-segment piecewise-linear characteristic. For future reference, the three distinct operating regions are labeled *Linear*, + *Saturation*, and − *Saturation*, respectively, in Fig. 1.6.

To emphasize that $A = \infty$ in the linear region, we add ∞ inside the triangle to distinguish the *ideal op-amp symbol* in Fig. 1.6*a* from other models. Unless otherwise stated, this ideal op-amp model will be used throughout this book.

The ideal op-amp model can be described analytically as follows:

Equations describing the ideal op-amp model

$$i_- = 0 \tag{1.2a}$$

$$i_+ = 0 \tag{1.2b}$$

$$v_o = E_{sat}\frac{|v_d|}{v_d}, \qquad v_d \neq 0 \tag{1.2c}$$

$$v_d = 0, \qquad -E_{sat} < v_o < E_{sat} \tag{1.2d}$$

Because these equations are rather cumbersome and difficult to manipulate analytically, it is much more practical to represent each region by a simple *equivalent circuit*, as shown in Fig. 1.6*c*, *d*, and *e*, respectively.

Note that these three equivalent circuits contain exactly the same information as Eq. (1.2). In particular, when the op amp is operating in the *linear*

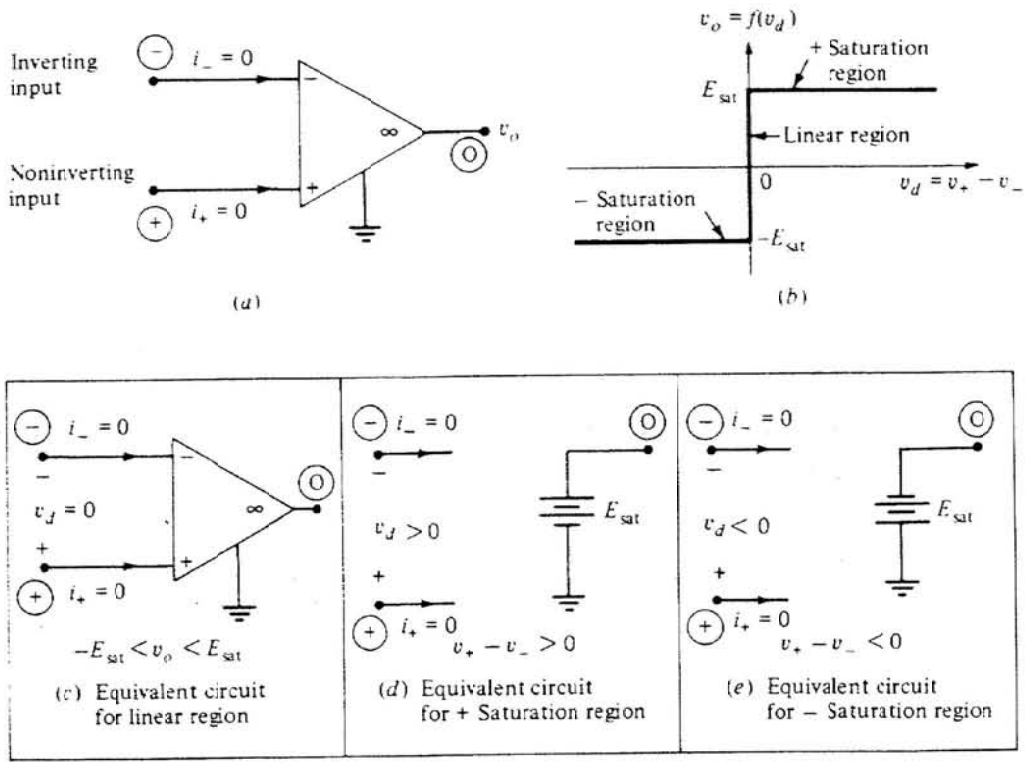


Figure 1.6 Ideal op-amp model.

region, the ideal op-amp model reduces to that shown in Fig. 1.6*c*. Note that here, v_d is constrained to be *zero* at all times while $|v_o|$ is constrained to be *less* than the saturation voltage E_{sat}. Hence, this circuit is described by Eqs. (1.2*a*), (1.2*b*), and (1.2*d*).

The circuit in Fig. 1.6*d* is described by Eqs. (1.2*a*), (1.2*b*), and (1.2*c*) with $v_d > 0$. Likewise, the circuit in Fig. 1.6*e* is described by Eqs. (1.2*a*), (1.2*b*), and (1.2*c*) with $v_d < 0$.

The ideal op-amp model is therefore described by three equivalent circuits, one for each operating region. If an op amp is known, a priori, to be operating in only one of these three regions in a given circuit, then we sometimes abuse our language by referring to the corresponding equivalent circuit in Fig. 1.6 as the ideal op-amp model.

For most low-frequency applications, the ideal op-amp model has been found to be quite realistic. For some specialized low-frequency applications (such as precision instrumentation) or high-frequency applications (such as filters), various op-amp imperfections may become important. In that case, the ideal model can be refined by introducing additional circuit elements.

Most op-amp circuits are designed so that the op amps operate *only in the linear region*. These circuits may contain both linear and nonlinear elements, and are studied in Sec. 2 using the equivalent circuit in Fig. 1.6*c*. Other op-amp circuits are designed to take advantage of the abrupt nonlinearities and are studied in Sec. 3 using all three equivalent circuits in Fig. 1.6.

Exercises

1. The op-amp manufacturers' data sheets usually specify the typical value of the average *input bias current* $I_B \triangleq \frac{1}{2}(|I_{B+}| + |I_{B-}|)$ and the *offset current* $I_{os} \triangleq |I_{B+}| - |I_{B-}|$. Express $|I_{B+}|$ and $|I_{B-}|$ in terms of I_B and I_{os}.
2. Calculate I_{B+} and I_{B-} for the following op amps:

	Op amp				
	μA709	LM101	μA741	LM301A	LM101A
Typical input bias current at 25°C	200 nA	120 nA	80 nA	70 nA	30 nA
Typical offset current at 25°C	50 nA	40 nA	20 nA	3.0 nA	1.5 nA

3. The data sheet for the μA741 shows a typical open-loop voltage gain of 200,000. Calculate the value of ϵ for the following power supply voltages (assume E_{sat} = magnitude of power supply voltage − 2 V): (*a*) ±15 V and (*b*) ±20 V.

2 OP-AMP CIRCUITS OPERATING IN THE LINEAR REGION

The methods to be developed in this section are valid *only* if the op-amp output voltage satisfies

$$-E_{sat} < v_o(t) < E_{sat} \tag{2.1}$$

for all times t (see Fig. 1.6*b*). We will henceforth refer to the expression (2.1) as the *validating inequality* for the *linear* region. If this inequality is violated over any time interval $[t_1, t_2]$, the solution in this interval is incorrect and must be recalculated using the method in Sec. 3.

2.1 Virtual Short Circuit Model

Recall from Chap. 3 that a three-port or four-terminal resistor is characterized by three relationships among the associated voltage and current variables. In the *linear* region, the ideal op-amp model in Fig. 1.6*a* and *b* can be described analytically by three equations:[2]

Virtual short circuit model

$$\boxed{\begin{aligned} i_- &= 0 \\ i_+ &= 0 \\ v_+ - v_- &= 0 \end{aligned}} \tag{2.2}$$

Consequently, we can think of the ideal op-amp model in Fig. 1.6*c* as a three-port or four-terminal resistor. For purposes of analysis, Eq. (2.2) is

[2] These correspond to Eqs. (1.2*a*), (1.2*b*), and (1.2*d*).

equivalent to (*a*) connecting a *short circuit* across the op-amp input terminals, and (*b*) stipulating that *the current through it is zero at all times*. To emphasize the special nature of this short circuit, we will henceforth refer to Eq. (2.2) as the *virtual short circuit* model. Using this equivalent circuit, many op-amp circuits can be analyzed by inspection.

2.2 Inspection Method

This method usually requires no more than three calculations and is often implemented by invoking KCL and Eq. (2.2) mentally with perhaps an occasional scribble on the "back of the envelope." It is best illustrated via some useful op-amp circuits as examples.

A. Voltage follower (buffer) The simplest op-amp circuit operating in the linear region is the voltage follower shown in Fig. 2.1*a*. To illustrate the *inspection method*, we first apply KCL at node ② and obtain

$$i_{\text{in}} = i_- = 0 \tag{2.3}$$

Applying next KVL around the closed node sequence ④–③–②–①–④, we obtain $v_o - v_{\text{in}} + v_d = 0$. Since $v_d = 0$, we have

$$v_o = v_{\text{in}} \tag{2.4}$$

To complete the analysis, we apply the *validating inequality* (2.1) and obtain

$$-E_{\text{sat}} < v_{\text{in}} < E_{\text{sat}} \tag{2.5}$$

This gives the dynamic range of input voltages beyond which the op amp no longer operates in the linear region.

Note that Eqs. (2.3) and (2.4) define a unity-gain VCVS (Fig. 2.1*b*). This circuit has an *infinite* input resistance because $i_{\text{in}} = 0$ and its output "duplicates" the input voltage, regardless of the external load. Consequently, it is

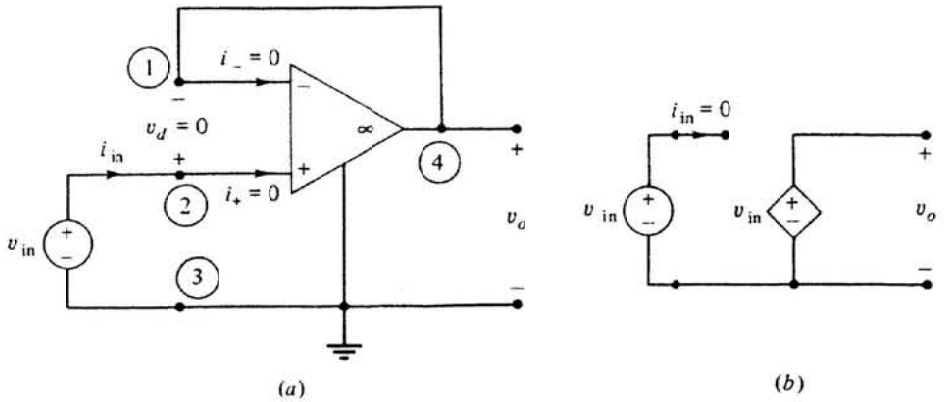


Figure 2.1 The voltage follower circuit in (*a*) is equivalent to the unity-gain VCVS in (*b*).

usually called a *voltage follower*, a *buffer*, or an *isolation amplifier*. It is widely used between 2 two-ports as shown in Fig. 2.2 to prevent N_2 from "loading down" N_1. This isolation technique is one of the most useful tools in the designer's bag of tricks.

Exercises

1. (*a*) Let N_1 and N_2 denote two identical *linear* voltage dividers made of resistances R_1 and R_2. Find the transfer characteristic $v_o = f(v_{in})$. (*b*) Repeat (*a*) without the buffer.
2. (*a*) Let N_1 and N_2 denote the "half-wave rectifier circuit" (Fig. 6.3*a*) analyzed earlier in Chap. 2. Find the v_o vs. v_{in} transfer characteristic. (*b*) Does your answer from (*a*) remain valid if N_1 is connected directly to N_2?

B. Inverting amplifier To illustrate the *inspection method* for op-amp circuits containing linear resistors, consider the circuit shown in Fig. 2.3. Since $v_d = 0$, we have $v_1 = v_{in}$, and hence $i_1 = v_{in}/R_1$. Since $i_- = 0$, we have $i_2 = i_1$, and hence $v_2 = R_f i_1 = R_f(v_{in}/R_1)$. Applying KVL around the closed node sequence ④–②–①–④, we obtain

$$v_o = -\left(\frac{R_f}{R_1}\right) v_{in} \tag{2.6}$$

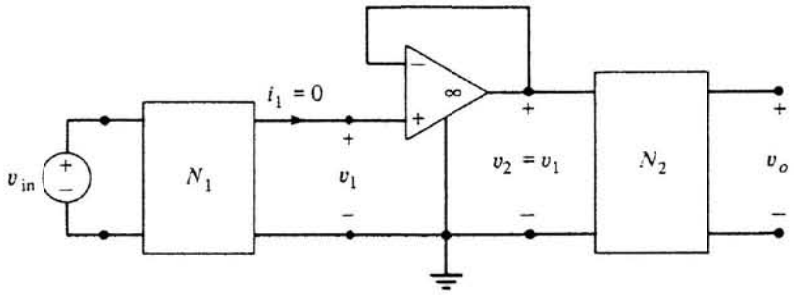


Figure 2.2 The above buffer greatly simplifies analysis and allows N_1 and N_2 to be designed separately.

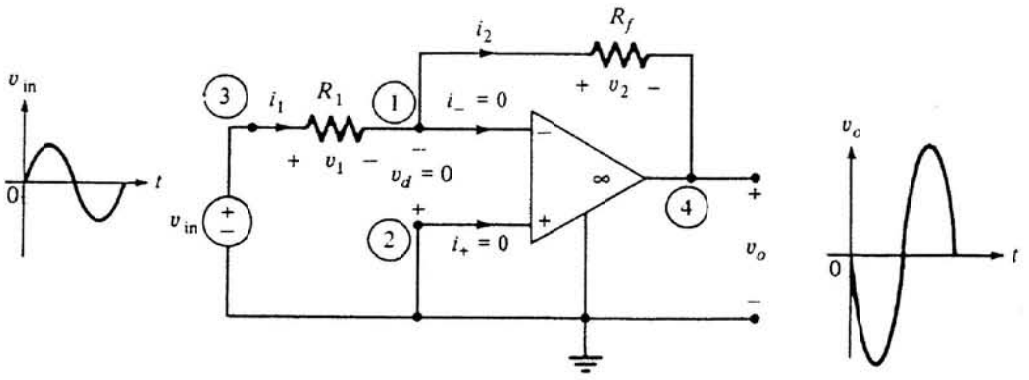


Figure 2.3 An inverting amplifier.

Substituting Eq. (2.6) into the validating inequality (2.1) and solving for v_{in}, we obtain the dynamic range

$$-\left(\frac{R_1}{R_f}\right) E_{sat} < v_{in} < \left(\frac{R_1}{R_f}\right) E_{sat} \tag{2.7}$$

for which Eq. (2.6) is valid.

Hence, so long as the input signal satisfies Eq. (2.7), this circuit functions as a voltage amplifier with a *voltage gain* equal to $-R_f/R_1$ (assuming $R_f > R_1$). Note that the negative sign means that for a sinusoidal input, the output is shifted in phase by 180°. Consequently, this circuit is called an *inverting amplifier*. In the special case where $R_1 = R_f$, it is called a *phase inverter*. (Why?)

Note that whereas $i_- = 0$ and $i_+ = 0$ are imposed by the op-amp v-i characteristics, the "virtual short circuit" $v_d = 0$ is achieved externally by "feeding back" the output voltage v_o to the op-amp inverting terminal through the feedback resistor R_f. The physical mechanism which automatically adjusts v_d to a nearly zero voltage is discussed in Sec. 3.2B.

Exercises

1. Using a buffer and the circuit in Fig. 2.3 (assume $R_1 = 10$ K), design a VCVS ($v_o = \mu v_{in}$) with a controlling coefficient $\mu = -1000$.
2. Repeat Exercise 1 with $\mu = 1000$. Hint: Add a phase inverter.

C. Noninverting amplifier As a further illustration of the inspection method, consider next the circuit shown in Fig. 2.4. Since $v_d = 0$, we have $v_1 = v_{in}$, and hence $i_1 = v_{in}/R_1$. Since $i_- = 0$, we have $i_2 = i_1 = v_{in}/R_1$, and hence $v_2 = (R_f/R_1)v_{in}$. Applying KVL around the closed node sequence ④–③–①–④ and simplifying, we obtain

$$v_o = \left(1 + \frac{R_f}{R_1}\right) v_{in} \tag{2.8}$$

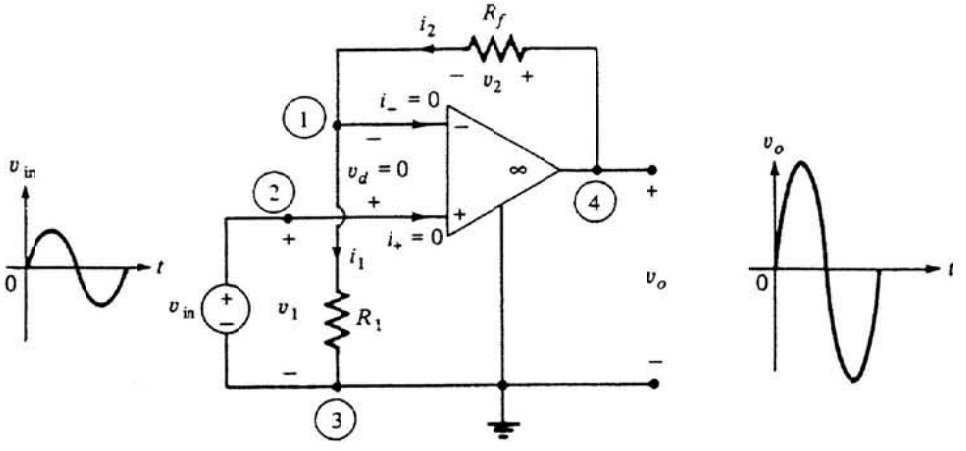


Figure 2.4 A noninverting amplifier.

Substituting Eq. (2.8) in the validating inequality (2.1) and solving for v_{in}, we obtain the dynamic range

$$-\left(\frac{R_1}{R_1+R_f}\right)E_{sat} < v_{in} < \left(\frac{R_1}{R_1+R_f}\right)E_{sat} \tag{2.9}$$

for which Eq. (2.8) is valid.

Hence, so long as the input signal satisfies Eq. (2.9), this circuit functions as a voltage amplifier with a *positive* voltage gain $(R_1+R_f)/R_1$. It is usually called a *noninverting amplifier*. Note that a voltage follower is simply a unity-gain noninverting amplifier obtained by choosing $R_1=\infty$ and $R_f=0$.

Exercises

1. The circuit in Fig. 2.5 is called an *algebraic summer* because $v_o = k_1v_1 + k_2v_2$. Find k_1 and k_2 and identify the region in the v_1-v_2 plane for which this relationship is valid.
2. Using exactly two op amps and $n+3$ resistors, design an n-input summer giving $v_o = v_1 + v_2 + \cdots + v_n$.
3. (*a*) Explain why the resistor R_f in Figs. 2.3 and 2.4 can be replaced by *any* one-port (except an open circuit) without affecting the value of i_2. (*b*) Using a 3-V battery and either circuit in Figs. 2.3 and 2.4, design a *dc current source* having a terminal current of 30 mA. Hint: Use the property from (*a*). (*c*) Repeat (*b*) for a terminal current of −30 mA.
4. Using only one op amp and one resistor, design a VCCS described by $i_2 = kv_{in}$, where $k>0$. Specify the maximum range of permissible "load" voltage across the current source.

D. Resistance measurement without surgery To show that the "virtual short circuit" is not just a powerful tool for simplifying *analysis*, Fig. 2.6 gives a circuit which exploits this remarkable property in a practical *design*. The linear resistive circuit enclosed within the circle represents the portion of a circuit where the value of each resistance is to be measured *without cutting any wires*. This problem usually arises when a circuit breaks down and a faulty resistor is to be identified by comparing its resistance with the nominal value.

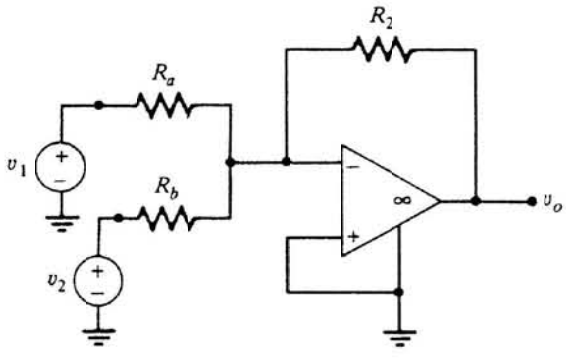


Figure 2.5 An algebraic summer.

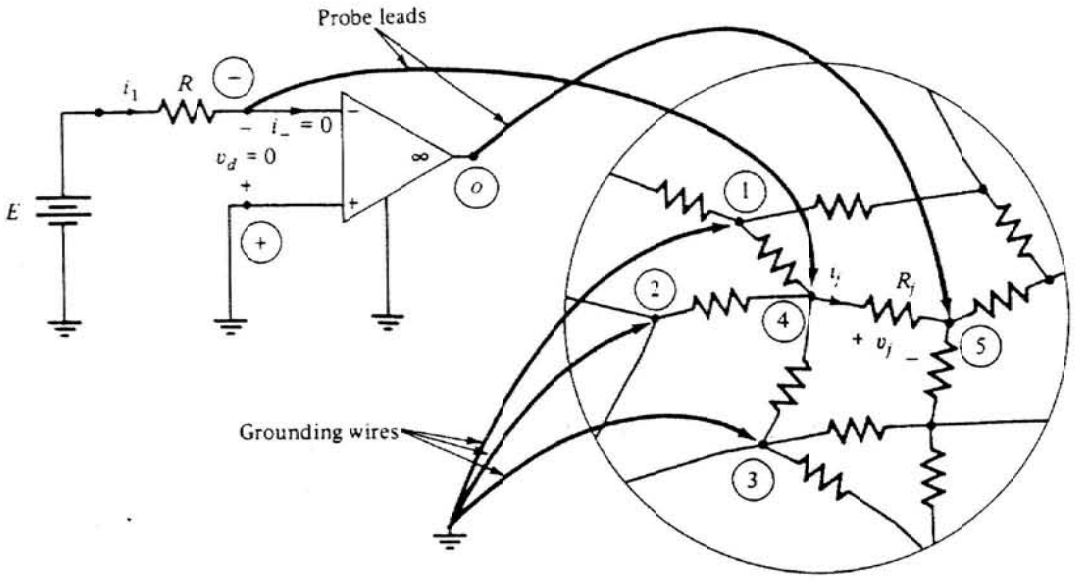


Figure 2.6 An op-amp fault detector.

To show how this circuit works, suppose resistor R_j is to be measured. (*a*) Connect the op-amp inverting terminal ⊖ to one terminal of R_j (node ④ in Fig. 2.6) and ground the second terminal of all other resistors connected to node ④ (nodes ①, ②, and ③ in Fig. 2.6). (*b*) Connect the op-amp output terminal ⓞ to the second terminal of R_j (node ⑤ in Fig. 2.6). It follows from the virtual short-circuit property that except for R_j, the current through all resistors connected to node ④ is zero. Moreover, since $i_1 = E/R$ and $i_- = 0$, we have $i_j = E/R$ and $v_j = (E/R)R_j$. Hence, by measuring the voltage v_j, we can calculate

$$R_j = \frac{R}{E} v_j \tag{2.10}$$

Note that without the virtual short circuit, R_j would have to be cut before its value can be measured.

E. Nonlinear feedback To illustrate that the inspection method holds even if the op-amp circuit contains one or more *nonlinear* resistors, consider the circuit shown in Fig. 2.7. By inspection, we note that $i_2 = i_1 = v_{in}/R_1$ and $v_o = -v_2$.

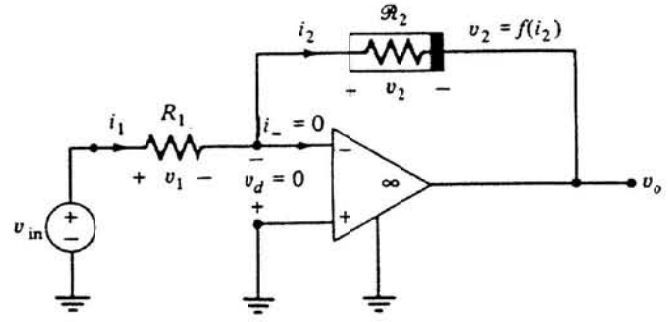


Figure 2.7 An op-amp circuit containing a nonlinear resistor.

Consequently

$$v_o = -f\left(\frac{v_{in}}{R_1}\right) \tag{2.11}$$

To determine the dynamic range of v_{in} for which Eq. (2.11) holds, we apply the validating inequality (2.1) and obtain

$$-E_{sat} < -f\left(\frac{v_{in}}{R_1}\right) < E_{sat} \tag{2.12}$$

Equations (2.11) and (2.12) give the *nonlinear* transfer characteristic with the op amp operating in the *linear* region. Since this configuration is widely used in nonlinear applications, we will consider an example.

Example Let $R_1 = 1\ \text{k}\Omega$ in Fig. 2.7. Let the nonlinear resistor represent the one-port shown in Fig. 2.8*a*. Using the graphic method from Chap. 2, we obtain the driving-point characteristic in Fig. 2.8*b*, where we have chosen v_2 as the vertical axis so that the curve represents $v_2 = f(i_2)$. It follows from Eq. (2.11) that the transfer characteristic is obtained by flipping this curve about the horizontal axis and then relabeling v_3 and i_2 with v_o and v_{in}, respectively. The result is shown in Fig. 2.8*c*.

Assuming a 15-V supply voltage for the op amp so that $E_{sat} = 13$ V, we note that Eq. (2.12) is satisfied for *all* values of v_{in} because $|v_o| = |-f(v_{in}/R_1)| < 10$ V in Fig. 2.8*c*. Hence, we have demonstrated that the op amp can operate in the linear region for all values of input voltages, even though the circuit contains two nonlinear devices (zener diodes in this example).

An examination of Fig. 2.8*c* shows that all input signal amplitudes exceeding 5 V will give a constant output of ±10 V. Consequently, the circuit in this example is called a *limiter* or *clipper*, and is widely used for overvoltage protection and other applications in communication circuits.

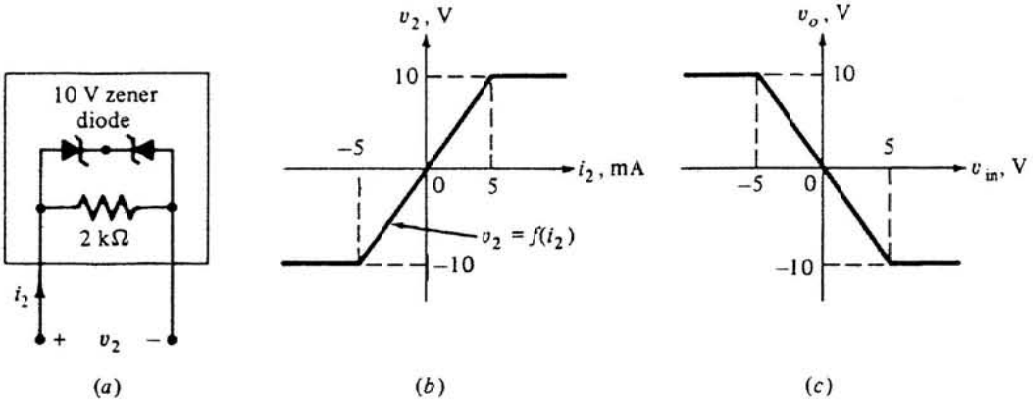


Figure 2.8 (*a*) Circuit for realizing the nonlinear resistor $\mathcal{R}_2$ in Fig. 2.7. (*b*) Driving-point characteristic of the circuit in *a*. (*c*) Transfer characteristic of the circuit in Fig. 2.7 with $\mathcal{R}_2$ replaced by the circuit in *a*, and assuming $R_1 = 1\ \text{k}\Omega$.

2.3 Systematic Method

The *inspection method* often fails whenever it is necessary to solve two or more simultaneous equations. In such cases, it is desirable to develop a *systematic method* for writing a system of linearly independent equations involving *as few variables* as possible. The following example illustrates the basic steps involved.

Example Consider the op-amp circuit shown in Fig. 2.9, where the op amp is modeled by a virtual short circuit (Fig. 1.6*c*). Although this circuit could be solved by inspection, we will solve it by the systematic method, and let the reader verify its answer by the inspection method.

Step 1. Label the nodes consecutively and let e_j denote as usual the voltage from node ⓙ to datum, $j = 1, 2, \ldots, 5$. Express *all* resistor voltages and the differential op-amp voltage v_d in terms of node-to-datum voltages via KVL:

$$v_1 = e_1 - e_3 \tag{2.13a}$$

$$v_2 = e_3 - e_5 \tag{2.13b}$$

$$v_3 = e_2 - e_4 \tag{2.13c}$$

$$v_4 = e_4 \tag{2.13d}$$

$$v_d = e_4 - e_3 \tag{2.13e}$$

Step 2. Express the branch current in each linear resistor in terms of node-to-datum voltages via Ohm's law:

$$i_1 = \frac{e_1 - e_3}{R_1} \tag{2.14a}$$

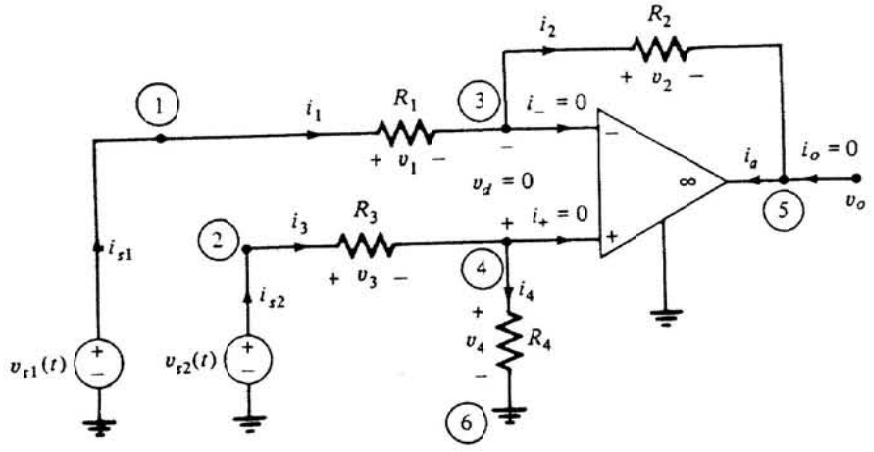


Figure 2.9 An op-amp circuit for illustrating the systematic method.

$$i_2 = \frac{e_3 - e_5}{R_2} \tag{2.14b}$$

$$i_3 = \frac{e_2 - e_4}{R_3} \tag{2.14c}$$

$$i_4 = \frac{e_4}{R_4} \tag{2.14d}$$

Step 3. Identify all other branch *current* variables which *cannot* be expressed in terms of node-to-datum voltages, namely, the currents i_{s1} and i_{s2} of the voltage sources and the current i_a of the op-amp *output* terminal. Note that the op-amp input currents i_- and i_+ are *not* variables (assuming an ideal op-amp model) because they are equal to zero. Our objective is to write a system of linearly independent equations in terms of the node-to-datum voltages $\{e_1, e_2, \ldots, e_5\}$ and the *identified* current variables $\{i_{s1}, i_{s2}, i_a\}$.

Step 4. Write KCL at each node except the datum node in terms of $\{e_1, e_2, e_3, e_4, e_5, i_{s1}, i_{s2}, i_a\}$:

Node ①: $$\frac{e_1 - e_3}{R_1} - i_{s1} = 0 \tag{2.15a}$$

Node ②: $$\frac{e_2 - e_4}{R_3} - i_{s2} = 0 \tag{2.15b}$$

Node ③: $$\frac{e_3 - e_5}{R_2} - \frac{e_1 - e_3}{R_1} = 0 \tag{2.15c}$$

Node ④: $$\frac{e_4}{R_4} - \frac{e_2 - e_4}{R_3} = 0 \tag{2.15d}$$

Node ⑤: $$i_a - \frac{e_3 - e_5}{R_2} = 0 \tag{2.15e}$$

Step 5. Equation (2.15) consists of five equations with eight variables. Hence, we need to write three more independent equations. Since we have already made use of KVL (Step 1), KCL (Step 4), and the resistor characteristics (Step 2), these three equations must come from the characteristics of the voltage sources and the op amp:

Voltage sources:

$$e_1 = v_{s1} = v_{s1}(t) \tag{2.16a}$$

$$e_2 = v_{s2} = v_{s2}(t) \tag{2.16b}$$

Op amp:[3]

$$e_4 - e_3 = 0 \tag{2.16c}$$

[3] Note that $v_d = e_4 - e_3$.

Step 6. Together, Eqs. (2.15) and (2.16) constitute a system of eight linearly independent equations in terms of eight variables. Solving these equations for the desired op-amp output voltage e_5 by elimination and substitution of variables, or by any other method, we obtain

$$v_o = e_5 = \left[\frac{R_4(1 + R_2/R_1)}{R_3 + R_4}\right] v_{s2}(t) - \left(\frac{R_2}{R_1}\right) v_{s1}(t) \tag{2.17}$$

Note that only Eqs. (2.15*c* and *d*) and (2.16) are used to solve for v_0. The remaining equations (2.15*a*, *b*, and *e*) are needed, however, to solve for the remaining variables i_{s1}, i_{s2}, and i_a, respectively.

Step 7. Determine the dynamic range of the input voltages where Eq. (2.17) holds, i.e., where the op amp is operating in the *linear* region:

$$-E_{\text{sat}} < \left[\frac{R_4(1 + R_2/R_1)}{R_3 + R_4}\right] v_{s2}(t) - \left(\frac{R_2}{R_1}\right) v_{s1}(t) < E_{\text{sat}} \tag{2.18}$$

Hence, Eq. (2.17) holds at all times when the expression (2.18) is satisfied.

Exercise Derive Eqs. (2.17) and (2.18) by the inspection method.

Special case (differential amplifier) Suppose $R_1/R_2 = R_3/R_4$ in Fig. 2.9. Then Eqs. (2.17) and (2.18) reduce to the following:

$$v_o = \frac{R_2}{R_1}\left[v_{s2}(t) - v_{s1}(t)\right],$$

$$-\frac{R_1}{R_2} E_{\text{sat}} < v_{s2}(t) - v_{s1}(t) < \frac{R_1}{R_2} E_{\text{sat}} \tag{2.19}$$

Equation (2.19) defines a *differential dc amplifier*, a circuit widely used in instrumentation applications.

The preceding systematic method is applicable to any op-amp circuit containing linear resistors, independent voltage and current sources, and op amps modeled by virtual short circuits. This method will be generalized in Chap. 8 [called the *modified node analysis* (MNA) method] for arbitrary resistive circuits.

Exercises

1. Generalize the steps in the preceding systematic method for a connected n-node circuit containing *linear* resistors, k voltage sources, ℓ current sources, and m op amps.
2. (*a*) Show that in the linear region, the ideal op-amp model is equivalent to a *linear* two-port resistor described by a *transmission matrix* **T** which specifies the port variables v_d and i_- (associated with port 1) in terms of the port variables v_o and i_o (associated with port 2). (*b*) Use the "linearity" property from (*a*) to show any circuit made of linear resistors, independent sources, and ideal op amps operating in the linear region can be analyzed by solving only linear equations.

3 OP-AMP CIRCUITS OPERATING IN THE NONLINEAR REGION

There are many applications where the op amp operates in all three regions of the ideal op-amp model in Fig. 1.6. This occurs whenever the amplitudes of one or more input signals are such that the validating inequality in each region is violated over some time intervals. In this case it is necessary to revert to the nonlinear model in Fig. 1.6 and we say the op amp is operating in the *nonlinear* region. Fortunately, since the characteristic in Fig. 1.6*b* is *piecewise linear*, the circuit in each region can be easily analyzed as a *linear* circuit.

3.1 + Saturation and − Saturation Equivalent Circuits

In the + *Saturation* region, the ideal op-amp model in Fig. 1.6 can be described analytically by three equations:

+ Saturation characteristics

$$\boxed{\begin{aligned} i_- &= 0 \\ i_+ &= 0 \\ v_o &= E_{\text{sat}} \end{aligned}} \tag{3.1}$$

These equations are applicable provided the following *validating inequality* holds:

$$\boxed{v_d = v_+ - v_- > 0} \tag{3.2}$$

Note that the *crucial* difference between the "+ Saturation characteristics" and the previous "linear characteristics" is that here, $v_d \triangleq v_+ - v_- \neq 0$ *and* v_o is now "clamped" at a fixed positive voltage equal to E_{sat}. In this region, we can replace the op amp by the equivalent circuit shown in Fig. 1.6*d*, which is redrawn in Fig. 3.1 for convenience.

In the − *Saturation* region, the ideal op-amp model in Fig. 1.6 can be described analytically as follows:

− Saturation characteristics

$$\boxed{\begin{aligned} i_- &= 0 \\ i_+ &= 0 \\ v_o &= -E_{\text{sat}} \end{aligned}} \tag{3.3}$$

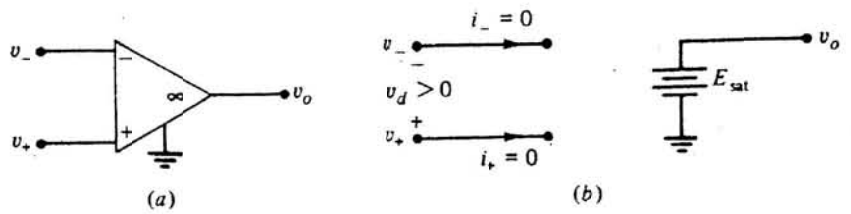


Figure 3.1 The + Saturation model.

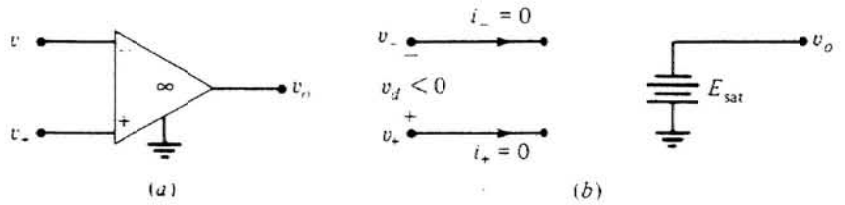


Figure 3.2 The − Saturation model.

These equations are applicable provided the following *validating inequality* holds:

$$\boxed{v_d = v_+ - v_- < 0} \tag{3.4}$$

Again, in sharp contrast to the "linear characteristics," here $v_d \triangleq v_+ - v_- \neq 0$ *and* v_o is "clamped" at a fixed negative voltage equal to $-E_{sat}$. In this region, we can replace the op amp by the equivalent circuit shown in Fig. 1.6*e*, which is redrawn in Fig. 3.2 for convenience.

Analogous to Eq. (2.1), we will henceforth call Eqs. (3.2) and (3.4) the *validating inequality* for the + *Saturation* and − *Saturation* regions, respectively.

Corresponding to the three regions in the ideal op-amp model of Fig. 1.6, we have three simplified equivalent circuits defined by Eqs. (2.1) and (2.2), (3.1) and (3.2), and (3.3) and (3.4), respectively. *The correct equivalent circuit to use in a given situation depends on, and only on, which of the three validating inequalities (2.1), (3.2), or (3.4) holds.*

3.2 Inspection Method

Most op-amp circuits which operate in the *nonlinear* region have a single input and a single output of interest. For this class of circuits, the basic problem is to derive the *driving-point characteristic* or the *transfer characteristic*. Once these characteristics are found, the output waveform due to *any* input waveform can be easily obtained either graphically or by direct substitution. The method for deriving these characteristics is best illustrated via examples.

A. Comparator (threshold detector) The simplest op-amp circuit operating in the nonlinear region is the comparator circuit shown in Fig. 3.3*a*. Replacing the ideal op-amp model by the virtual short circuit, + Saturation, and − Saturation equivalent circuits, respectively, we obtain the corresponding *linear* circuit shown in Fig. 3.4*a*, *b*, and *c*, respectively.

Consider first the circuit in Fig. 3.4*a*. Since $v_d = v_{in} - E_T = 0$, the op amp can operate in the *linear region* if and only if $v_{in} = E_T$. In such a case, we find $i_{in} = 0$ (Fig. 3.3*b*) and $-E_{sat} < v_o < E_{sat}$ (Fig. 3.3*c*).

Consider next the circuit in Fig. 3.4*b*. Since $v_d = v_{in} - E_T > 0$, the op amp operates in the + *Saturation region* if and only if $v_{in} > E_T$. In such a case, we find $i_{in} = 0$ (Fig. 3.3*b*) and $v_o = E_{sat}$ (Fig. 3.3*c*).

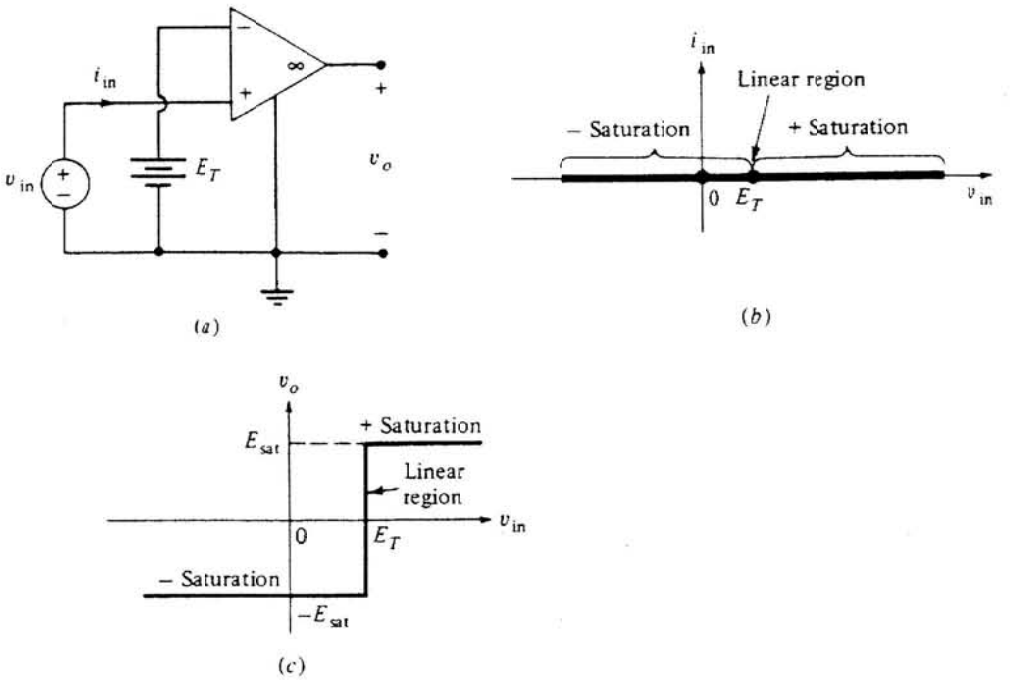


Figure 3.3 (*a*) Comparator. (*b*) Driving-point characteristic. (*c*) Transfer characteristic.

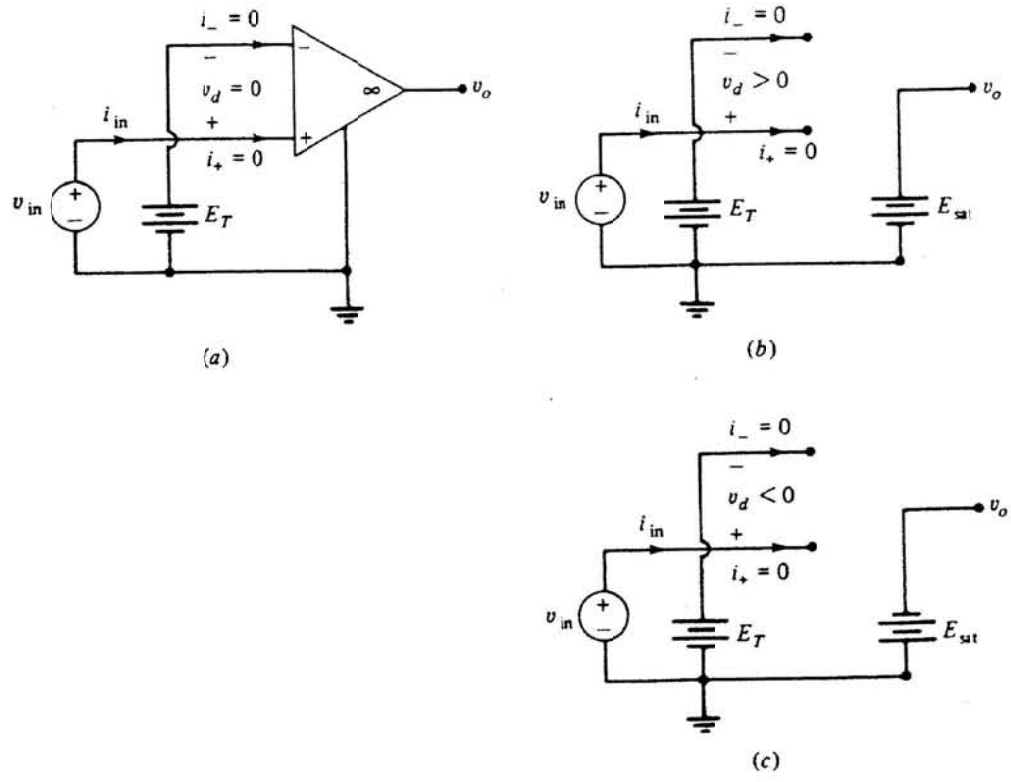


Figure 3.4 Linear circuit for each region.

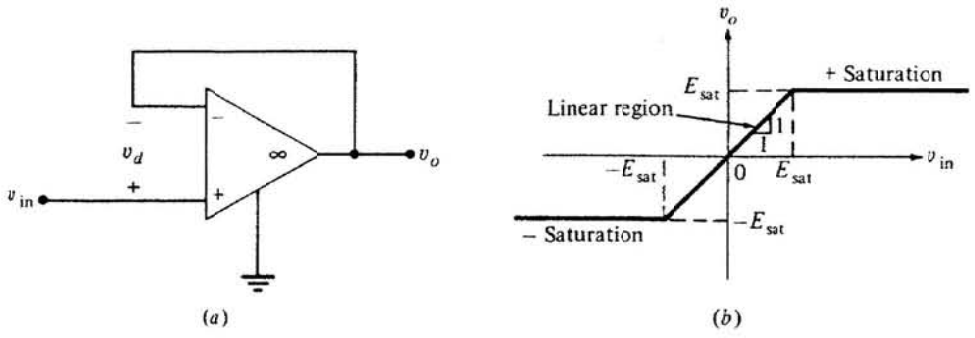
It remains to consider the circuit in Fig. 3.4*c*. Since $v_d = v_{in} - E_T < 0$, the op amp operates in the *– Saturation region* if and only if $v_{in} < E_T$. In which case, we find $i_{in} = 0$ (Fig. 3.3*b*) and $v_o = -E_{sat}$ (Fig. 3.4*c*).

An examination of the transfer characteristic in Fig. 3.3*c* shows that the circuit "compares" the input signal with a prescribed threshold voltage E_T and responds by jumping abruptly from one level to another. Consequently, it is called a *comparator* or a *threshold detector*. In the special case where $E_T = 0$, the circuit becomes a *zero-crossing detector*. Comparators are so widely used in digital circuits that they are mass produced (with "bells and whistles" added for improved performance) and sold under the name "comparator."

B. Negative vs. positive feedback circuit Consider the circuit shown in Fig. 3.5*a*. Note that this is just the voltage follower in Fig. 2.1 studied earlier. There, we found that $v_o = v_{in}$ provided $|v_{in}| < E_{sat}$. By inspection, we found $v_o = E_{sat}$ whenever $v_{in} > E_{sat}$, and $v_o = -E_{sat}$ whenever $v_{in} < -E_{sat}$. The complete transfer characteristic is therefore as shown in Fig. 3.5*b*.

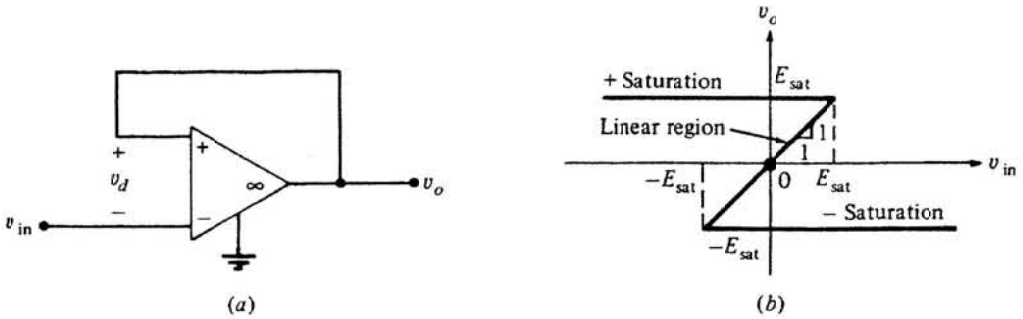
This circuit is said to have a "negative" feedback because the output voltage is fed back to the *inverting* input terminal.

What happens if we interchange the inverting and noninverting terminals as shown in Fig. 3.6*a*? By inspection, we found $v_o = v_{in}$ provided $|v_{in}| < E_{sat}$. Hence, in the linear region, the transfer characteristic for this "positive" feedback circuit is identical to that of the negative feedback circuit in Fig. 3.5*a*.



(*a*) (*b*)

Figure 3.5 (*a*) A negative feedback circuit and (*b*) its transfer characteristic.



(*a*) (*b*)

Figure 3.6 (*a*) A positive feedback circuit and (*b*) its transfer characteristic.

In practice, however, they do not behave in the same way: One functions as a voltage follower, the other does *not*. To uncover the reason, let us derive the transfer characteristics in the remaining regions.

When the op amp is in the + Saturation region, we can replace it by the equivalent circuit shown in Fig. 3.7*a*. The validating inequality (3.2) requires that $v_d = E_{sat} - v_{in} > 0$ or $v_{in} < E_{sat}$. Hence, the transfer characteristic in this region is given by $v_o = E_{sat}$ whenever $v_{in} < E_{sat}$, as shown in Fig. 3.6*b*.

Conversely, when the op amp is in the − Saturation region, the equivalent circuit shown in Fig. 3.7*b* holds and hence we obtain $v_o = -E_{sat}$ whenever $v_{in} > -E_{sat}$, as shown in Fig. 3.6*b*.

Note that the complete transfer characteristics in Figs. 3.5 and 3.6 are quite different. Even if the op amp is operating in the linear region ($|v_{in}| < E_{sat}$), there are three distinct output voltages for each value of v_{in} for the positive feedback circuit. Using a more realistic op-amp circuit model augmented by a capacitor, and the method to be developed in Chap. 6, we will show that all operating points on the middle segment (linear region) in Fig. 3.6*b* are *unstable*. The important concept of *stability* and *instability* will be discussed in detail in Chap. 6. In the present context, having *unstable operating points* in the middle region means that even if the initial voltage $v_{in}(0)$ lies on this segment, it will quickly move into the + Saturation region if $v_{in}(0) > 0$, or into the − Saturation region if $v_{in}(0) < 0$.

We can also give an *intuitive* explanation of this *unstable* behavior by referring back to the *nonideal* op-amp characteristics shown in Fig. 1.5*b*, where

$$v_o = A(v_+ - v_-) \tag{3.5}$$

in the linear region. Equation (3.5) shows that the output voltage v_o *decreases* (respectively, *increases*) whenever the potential v_- at the *inverting* (respectively noninverting) node increases, and vice versa.

Since physical signals can only propagate at a *finite* velocity, changes in the input voltage are not felt instantaneously at the output terminal, but at some moments [say 1 picosecond (ps)] later. Now suppose $v_d = v_{in} - v_o = 1$ nV at $t = 0$, whereupon v_{in} is increased slightly in both circuits in Figs. 3.5 and 3.6.

For the negative feedback circuit, v_o will increase initially in accordance with Eq. (3.5). However, since this signal is fed back to the inverting terminal

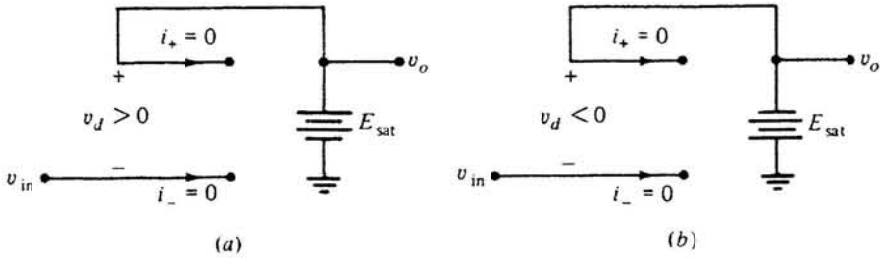


Figure 3.7 (*a*) Equivalent circuit in + Saturation region. (*b*) Equivalent circuit in − Saturation region.

in Fig. 3.5*a*, $v_d = v_+ - v_-$ will decrease a short moment later. Hence, the operating point in the middle segment of Fig. 3.5*b* will tend to return to its original position. The negative feedback circuit is therefore said to be "stable" because it tends to restore the original equilibrium position in the presence of small disturbances.

Exactly the opposite happens in the *positive* feedback circuit in Fig. 3.6*a*. Here, the slightest disturbance is amplified strongly—in view of the high gain A—as the signal goes around the feedback loop in finite time. This increase in v_d causes a further increase in v_d the next time around the loop. This "unstable" phenomenon is repeated in rapid order until the output is driven into saturation; thereafter, the model must be replaced by either Fig. 3.1 or 3.2.

C. Negative-resistance converter The circuit shown in Fig. 3.8*a* incorporates both a *negative* feedback path (via R_f) and a *positive* feedback path (via R_1).

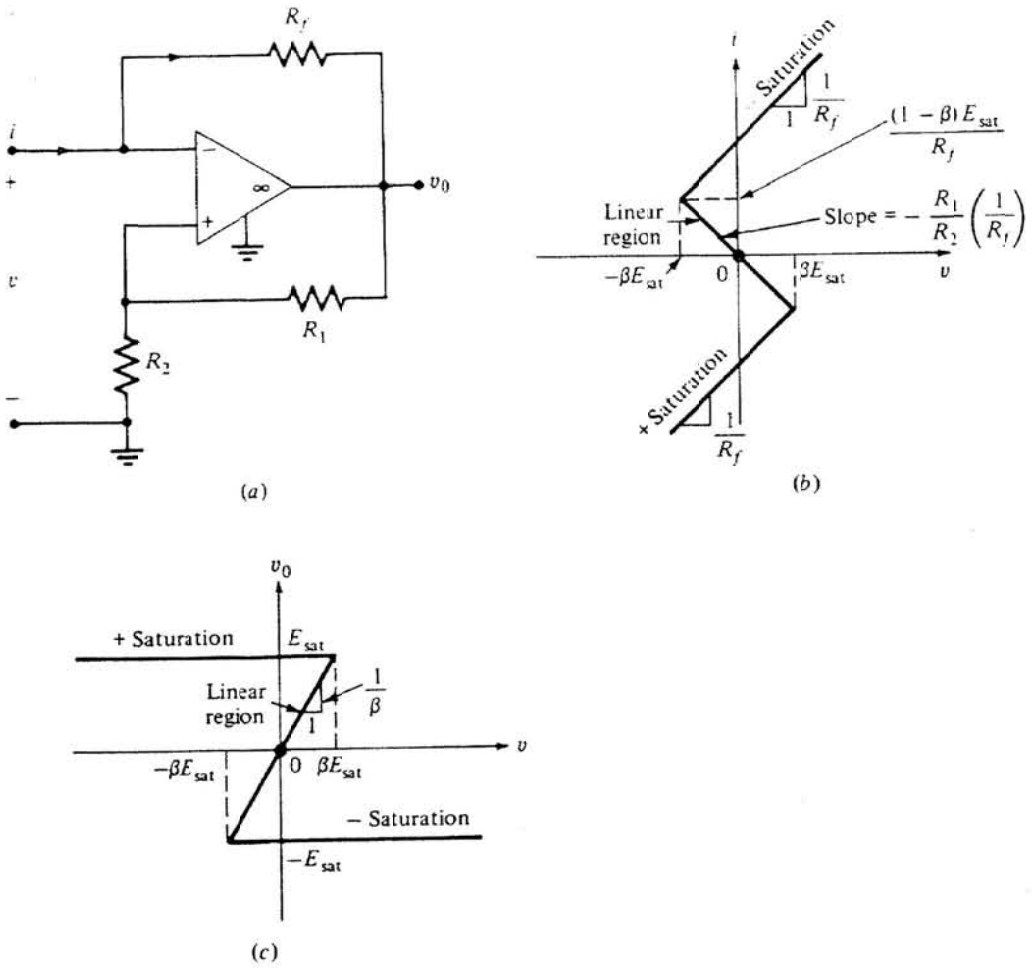


Figure 3.8 A negative-resistance converter and its driving-point and transfer characteristics. Here, $\beta \triangleq R_2/(R_1 + R_2)$.

Our problem is to derive its driving-point and transfer characteristics. As before, we replace the op amp in Fig. 3.8*a* by its three ideal models as shown in Fig. 3.9.

Linear region By inspection of the equivalent circuit in Fig. 3.9*a*, we note that R_1 and R_2 form a voltage divider so that

$$v_2 = \frac{R_2}{R_1 + R_2} v_o = \beta v_o \tag{3.6}$$

where $\beta \triangleq R_2/(R_1 + R_2)$. Substituting $v_2 = v$ into Eq. (3.6), we obtain

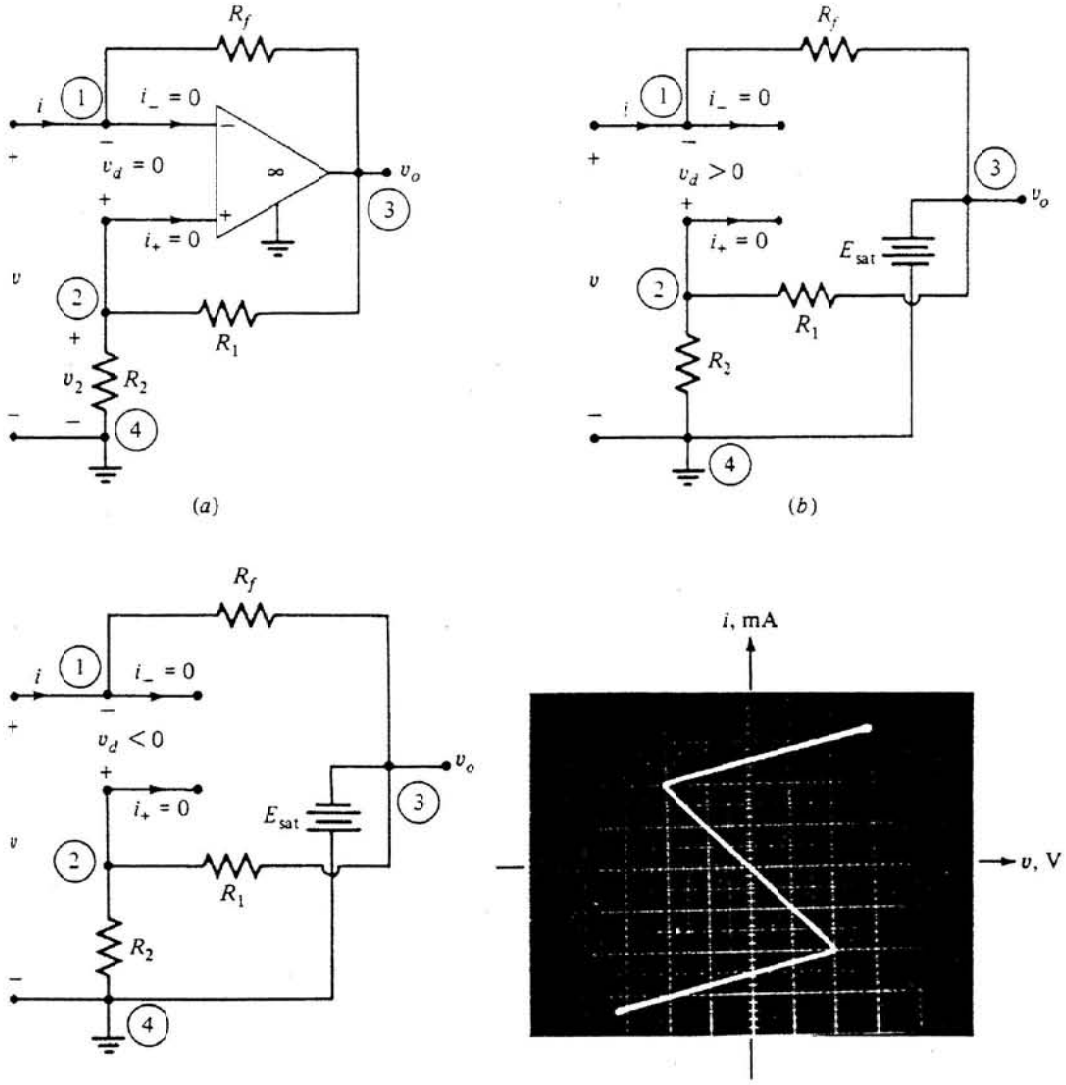


Figure 3.9 Equivalent circuit in (*a*) linear region, (*b*) + Saturation region, (*c*) − Saturation region, and (*d*) typical negative-resistance characteristic measured from an actual op-amp circuit.

$$v_o = \frac{1}{\beta} v \tag{3.7}$$

Applying KVL around the closed node sequence ④–①–③–④, we obtain

$$v = R_f i + v_o \tag{3.8}$$

Substituting Eq. (3.7) into Eq. (3.8) and solving for i, we obtain

$$i = -\left(\frac{R_1}{R_2}\right)\left(\frac{1}{R_f}\right) v \tag{3.9}$$

Equations (3.9) and (3.7) are drawn as the middle segment in Fig. 3.8*b* and *c*, respectively. To determine the boundary of these segments, substitute Eq. (3.7) into the validating inequality (2.1) and obtain

$$-\beta E_{\text{sat}} < v < \beta E_{\text{sat}} \tag{3.10}$$

+ Saturation region By inspection of the equivalent circuit in Fig 3.9*b*, we found

$$v = R_f i + E_{\text{sat}} \tag{3.11}$$

$$v_o = E_{\text{sat}} \tag{3.12}$$

To determine the range of v for which Eqs. (3.11) and (3.12) are valid, we solve for v_d by applying KVL around the closed node sequence ④–①–②–④:

$$v_d = \frac{R_2}{R_1 + R_2} E_{\text{sat}} - v = \beta E_{\text{sat}} - v \tag{3.13}$$

Applying the validating inequality (3.2) and solving for v, we obtain

$$v < \beta E_{\text{sat}} \tag{3.14}$$

Equations (3.11), (3.12), and (3.14) define the lower segment in Fig. 3.8*b* and the upper segment in Fig. 3.8*c*.

− Saturation region By inspection of the equivalent circuit in Fig. 3.9*c* and following the same procedure as above, we obtain

$$v = R_f i - E_{\text{sat}} \tag{3.15}$$

$$v_o = -E_{\text{sat}} \tag{3.16}$$

$$v > -\beta E_{\text{sat}} \tag{3.17}$$

Equations (3.15) and (3.17) define the upper segment in Fig. 3.8*b* whereas Eqs. (3.16) and (3.17) define the lower segment in Fig. 3.8*c*.

Figure 3.9*d* shows a typical driving-point characteristic measured from the op-amp circuit in Fig. 3.8*a*. The slopes and breakpoints of this nearly

piecewise-linear characteristic have been found to agree remarkably well with those prediced by Eqs. (3.9), (3.11), and (3.15).[4]

The circuit in Fig. 3.8*a* is called a *negative-resistance converter* because it converts *positive* resistances R_1, R_2, and R_f into a *negative resistance* equal to $-(R_2R_f/R_1)\,\Omega$ in the linear region. We will show in Chap. 6 how this circuit can be easily transformed into an oscillator or a flip-flop.

D. Concave and convex resistors The circuit in Fig. 3.10 contains a *pn*-junction diode described by[5]

$$i_D = \hat{i}(v_D) = \begin{cases} I_s\left(\exp\dfrac{v_D}{v_T} - 1\right) & v_D \geq 0 \\ 0 & v_D < 0 \end{cases} \tag{3.18}$$

in its feedback path. Our objective here is to show that when the op amp is operating in the linear and + Saturation regions, the resulting driving-point

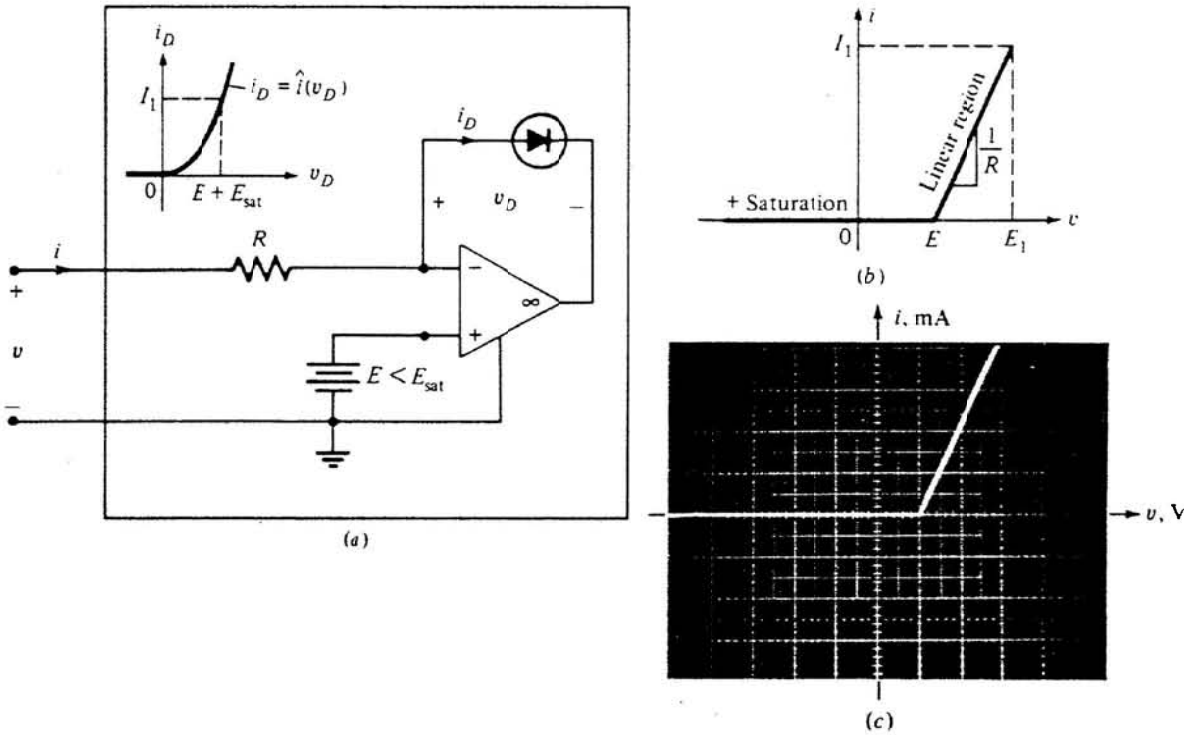


Figure 3.10 (*a*) Practical realization of a nearly ideal concave resistor characteristic. (*b*) Predicted characteristic for $v < E_1$, where $E_1 \triangleq E + R\hat{i}(E + E_{sat})$, provided $E < E_{sat}$. (*c*) Measured characteristic.

[4] For more examples of practical negative-resistance op-amp circuits, see L. O. Chua and F. Ayrom, "Designing Nonlinear Single Op-Amp Circuits: A Cookbook Approach," *Int. J. Circuit Theory Appl.*, pp. 309–326, October 1985.

[5] We assume $i_D = 0$ for $v_D < 0$ to simplify our analysis.

characteristic is identical to that defining a concave resistor for all $v < E_1$, where

$$E_1 \triangleq E + \underbrace{RI_s\left\{\exp\left[\frac{1}{V_T}(E + E_{sat})\right] - 1\right\}}_{I_1} \tag{3.19}$$

provided $E < E_{sat}$. The two equivalent circuits corresponding to these regions are shown in Fig. 3.11*a* and *b*, respectively.

Linear region From Fig. 3.11*a*, we note that $v_d = 0$ implies $e_2 = E$, and hence

$$v = Ri + E \tag{3.20}$$

To determine the range of i for which Eq. (3.20) is valid, we note first that $i = i_D \geq 0$ in view of Eq. (3.18). To determine the upper boundary, note that

$$-E_{sat} < v_o = -v_D + E < E_{sat} \tag{3.21}$$

in the linear region. Hence,

$$E - E_{sat} < v_D < E + E_{sat} \tag{3.22}$$

Since $\hat{i}(v_D)$ in Eq. (3.18) is a strictly monotone increasing function, it follows from Eq. (3.22) that

$$i_D < \hat{i}(E + E_{sat}) \triangleq I_1 \tag{3.23}$$

where $\hat{i}(E + E_{sat})$ denotes the diode current evaluated at $v_D = E + E_{sat}$. Hence

$$0 \leq i < I_1 \tag{3.24}$$

Using Eqs. (3.20), (3.23), and (3.24), the corresponding boundary in terms of

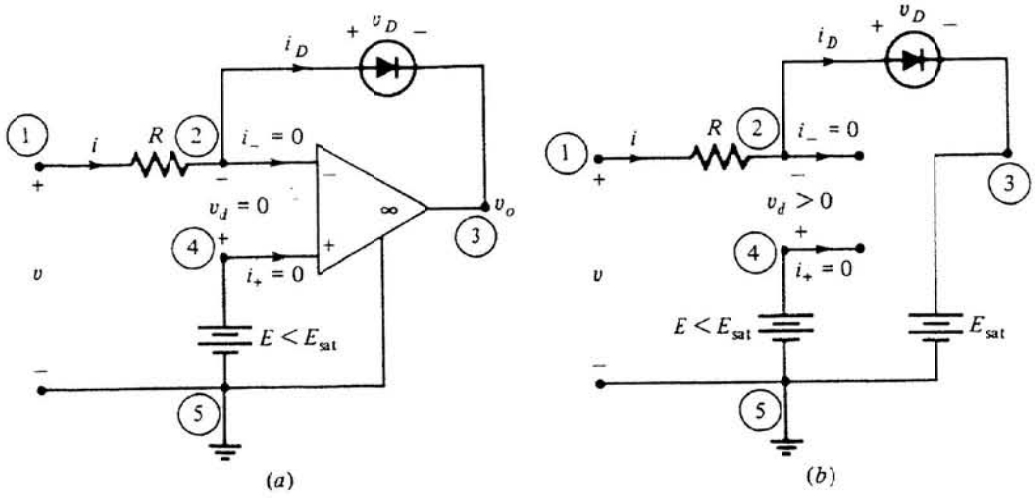


Figure 3.11 Equivalent circuit in (*a*) linear region and (*b*) + Saturation region.

v is seen to be

$$E \leq v < E_1 \tag{3.25}$$

where

$$E_1 \triangleq E + RI_1 = E + R\hat{i}(E + E_{sat}) \tag{3.26}$$

Equations (3.20) and (3.24) or Eqs. (3.25) and (3.26) define the right segment in Fig. 3.10*b*.

+ Saturation region Consider the equivalent circuit of Fig. 3.11*b* where $v_d = E - v + Ri$. Since $v_d > 0$ in the + Saturation region, we have

$$v < E + Ri \tag{3.27}$$

Applying KVL around the closed node sequence ②–①–⑤–③–② and making use of Eq. (3.27) we obtain

$$\begin{aligned} v_D &= v - Ri - E_{sat} < (E + Ri) - Ri - E_{sat} \\ &= E - E_{sat} < 0 \end{aligned} \tag{3.28}$$

because $E < E_{sat}$ by *assumption*. Hence, the diode is reversed biased when the op amp is in the *+ Saturation* region. It follows from Eqs. (3.18) and (3.27) that

$$i = 0 \tag{3.29}$$

$$v < E \tag{3.30}$$

Equations (3.29) and (3.30) define the left segment in Fig. 3.10*b*.

A typical v-i characteristic measured from the op-amp circuit in Fig. 3.10*a* is shown in Fig. 3.10*c*. Note that the "corner" at the breakpoint is remarkably sharp.

Special case Observe that in the limiting case where $R \to 0$ and $E \to 0$, the driving-point characteristic in Fig. 3.10*b* reduces to that of an *ideal diode*, as shown in Fig. 3.12*b*. Laboratory measurements show that even though $A < \infty$ in a real op amp, the resulting driving-point characteristic still nearly approaches that of an ideal diode. Figure 3.12*c* shows a typical *pn*-junction diode characteristic, and Fig. 3.12*d* shows the nearly "ideal" diode characteristic measured from the op-amp circuit in Fig. 3.12*a* with this *pn*-junction diode connected in the negative feedback path.

Convex resistor realization Using the above observation, we can design a nearly ideal convex resistor by first transposing the *pn*-junction diode in Fig. 3.12*a* to obtain the "dual" ideal diode shown in Fig. 3.13.

Substituting this circuit in place of the "transposed" ideal diode in Fig. 2.14 of Chap. 2, we obtain the op-amp circuit in Fig. 3.14*a* which realizes the "ideal" convex resistor characteristic in Fig. 3.14*b*. The driving-point

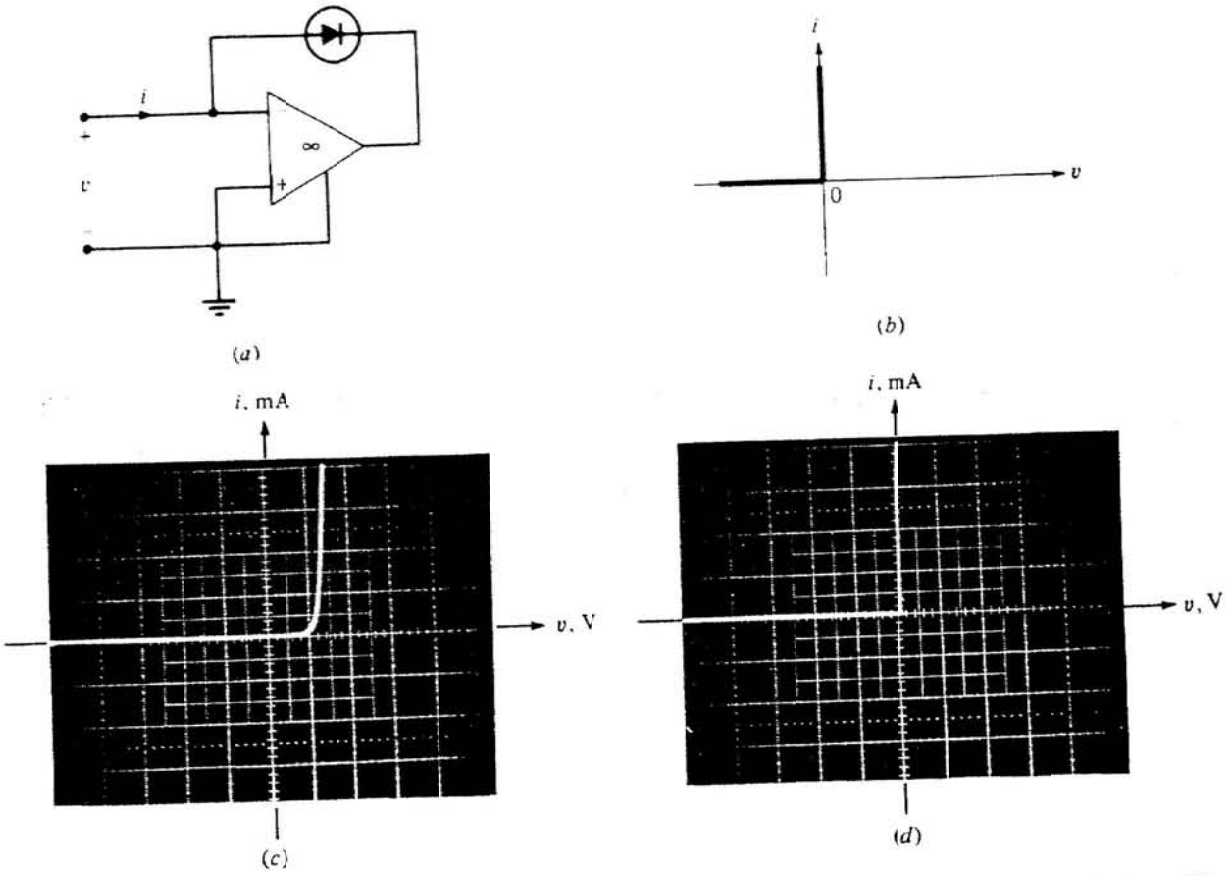


Figure 3.12 (*a*) Op-amp circuit realization of an ideal diode. (*b*) Limiting characteristic from Fig. 3.10*b* when $R \to 0$ and $E \to 0$. (*c*) Characteristic of the *pn*-junction diode in the op-amp circuit. (*d*) Measured driving-point characteristic.

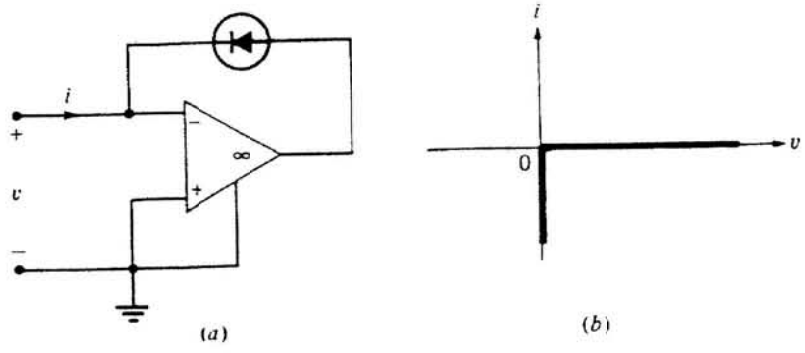


Figure 3.13 Op-amp realization of a transposed ideal diode.

characteristic measured from the circuit in Fig. 3.14*a* is shown in Fig. 3.14*c*. Again, note the sharp corner at the breakpoints.

Using the above concave and convex resistor realizations, any monotone increasing piecewise-linear driving-point characteristic can be designed with high precision.

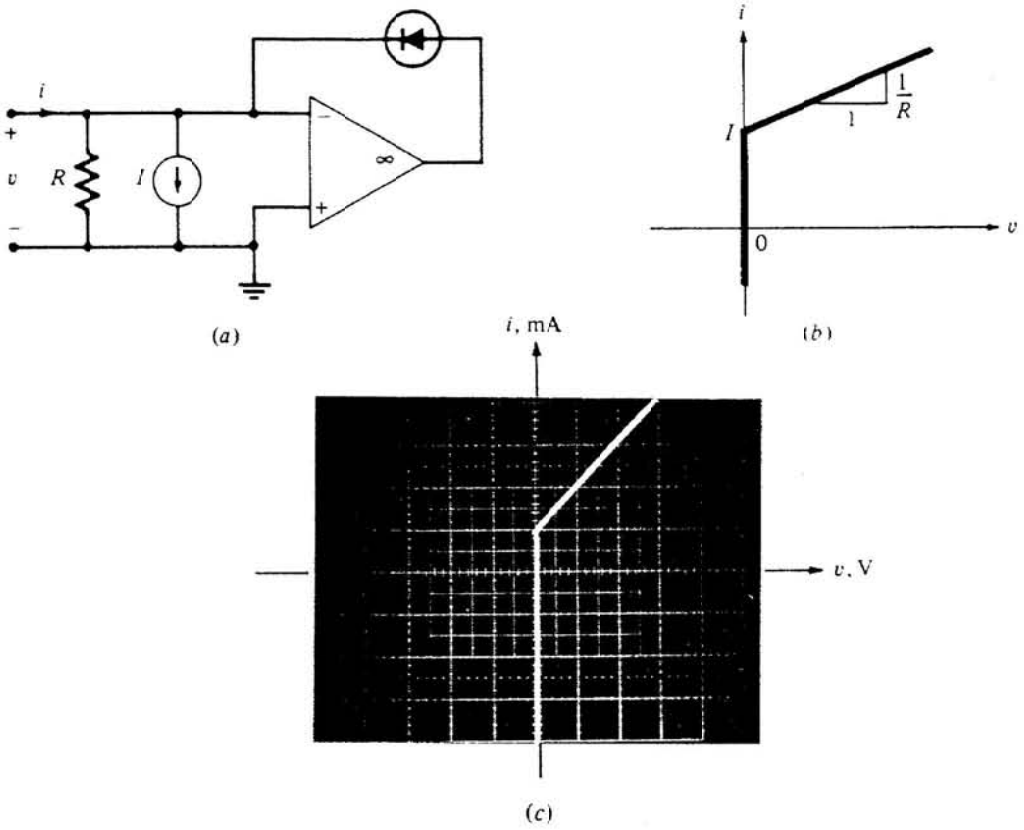


Figure 3.14 (*a*) Op-amp circuit realization of a convex resistor. (*b*) Ideal convex resistor characteristic. (*c*) Measured characteristic.

Exercises

1. Derive the remaining portion of the driving-point characteristic in Fig. 3.10*b* for $v > E_1$.
2. Derive the complete driving-point characteristic of the convex resistor circuit shown in Fig. 3.14*a*.

3.3 Systematic Method

For more complicated circuits which cannot be analyzed by the above method (e.g., feedback circuits containing several op amps), the systematic method presented in Sec. 2.3 can of course be used to derive the segment of the driving-point or transfer characteristic when the op amp is operating in the linear region. This systematic method is a special case of the modified node analysis method to be presented in Chap. 8.

For the + Saturation or − Saturation region, the same procedure can be easily modified for the corresponding equivalent circuits. In fact, the analysis in these regions is easier because the op amp is modeled by a battery.

Exercises

1. Give the procedure for carrying out the systematic method for the + Saturation and − Saturation regions.
2. Use the systematic method to derive the driving-point and transfer characteristics of the negative-resistance converter shown in Fig. 3.8*a*.

4 COMPARISON WITH FINITE-GAIN MODEL

The *ideal* op-amp model used so far in our analysis assumes that the open-loop voltage gain A in the linear region is infinite. When $A < \infty$, the model and equivalent circuits in Fig. 1.6 should be modified as shown in Fig. 4.1. We will henceforth refer to this model as the *finite-gain op-amp model.*

Using the *piecewise-linear* representation given by Eq. (3.9) in Chap. 2, we can describe this model analytically as follows:

Finite-gain op-amp model

$$i_- = 0 \tag{4.1a}$$

$$i_+ = 0 \tag{4.1b}$$

$$v_o = f(v_d) \triangleq \frac{A}{2}|v_d + \epsilon| - \frac{A}{2}|v_d - \epsilon| \tag{4.1c}$$

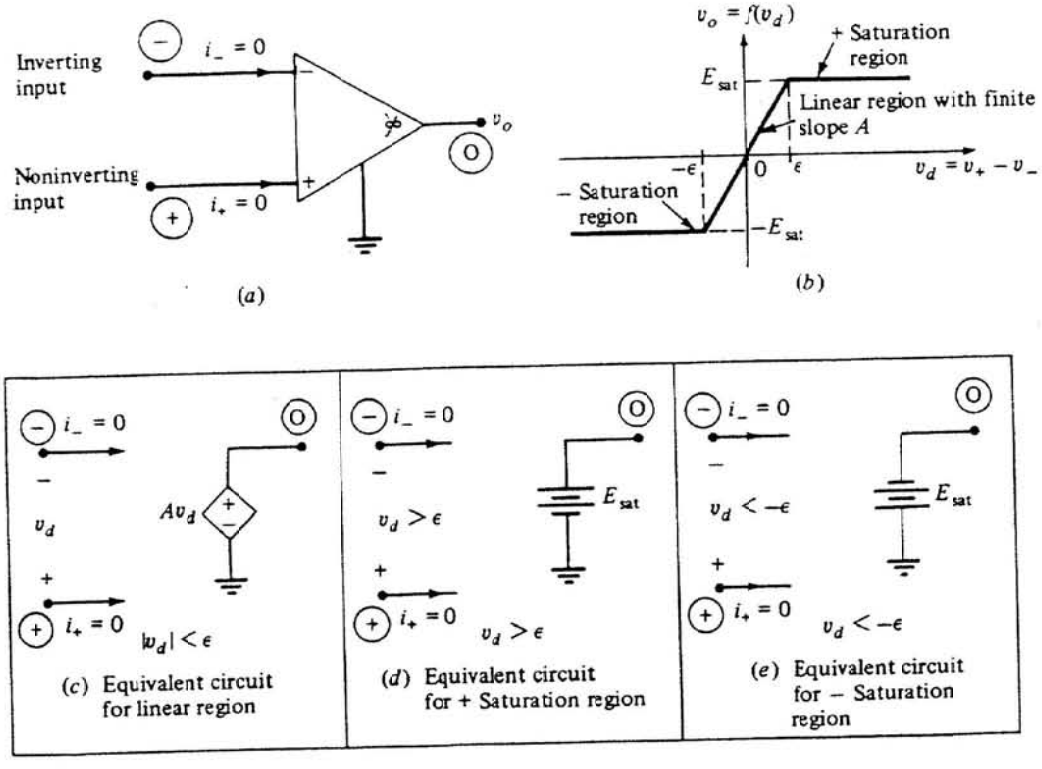


Figure 4.1 Finite-gain op-amp model.

Note that unlike Eq. (1.2*c*) of the ideal model, Eq. (4.1*c*) is a well-defined function for all values of v_d, *including* $v_d = 0$.

Since $i_- = 0$ and $i_+ = 0$ in both Figs. 1.6 and 4.1, we can write $i_- = -i_+$ and interpret both the *ideal* and the *finite-gain* op-amp model as a *two-port*. For example, the model in Fig. 4.1 can be redrawn as shown in Fig. 4.2, where $f(v_d)$ is given by Eq. (4.1*c*). In the linear region, the finite-gain model reduces to a linear *voltage-controlled voltage source* as shown in Fig. 4.3.

In order to compare the answers obtained from using the *ideal* and the finite-gain models, let us consider an example.

Example Let us analyze the *inverting amplifier* circuit in Fig. 2.3 using the finite-gain model. Since the op amp in this circuit is known to be operating in the linear region with a dynamic range given by Eq. (2.7), let us replace the op amp by the linear two-port model shown in Fig. 4.3*b*. The resulting circuit is shown in Fig. 4.4. We can calculate v_o by the *inspection* method as follows:

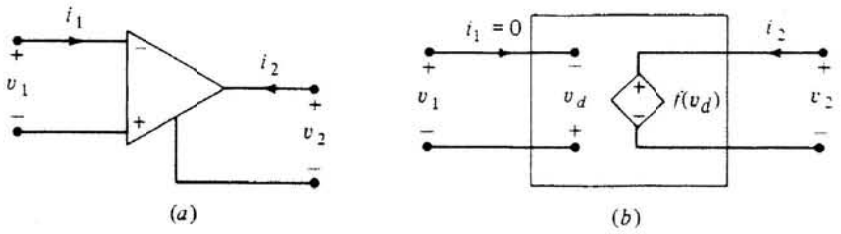


Figure 4.2 Equivalent nonlinear two-port model.

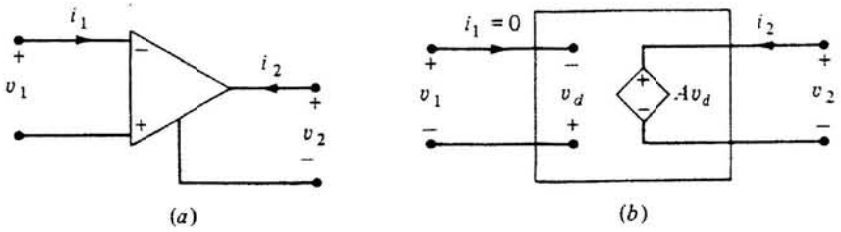


Figure 4.3 Equivalent linear two-port model (valid only if the op amp is operating in the linear region).

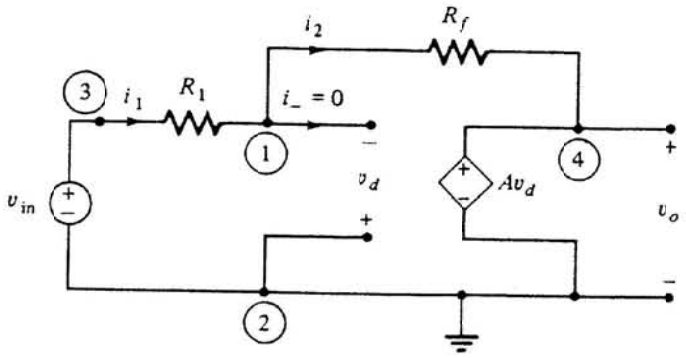


Figure 4.4 Inverting amplifier circuit with op amp modeled by Fig. 4.3*b*.

KCL at node ①:
$$i_2 = \frac{v_{in} + v_d}{R_1} \tag{4.2}$$

KVL at the closed node sequence ①–④–②–①:
$$R_f\left[\frac{v_{in} + v_d}{R_1}\right] + Av_d + v_d = 0 \tag{4.3}$$

Solving for v_d in Eq. (4.3), we obtain
$$v_d = -\left[\frac{1}{(R_1/R_f)A + (1 + R_1/R_f)}\right] v_{in} \tag{4.4}$$

Substituting Eq. (4.4) into $v_o = Av_d$, we obtain
$$v_o = -\left[\frac{1}{(R_1/R_f) + (1/A)(1 + R_1/R_f)}\right] v_{in} \tag{4.5}$$

As a check, note that as $A \to \infty$, Eq. (4.4) implies $v_d \to 0$ and Eq. (4.5) reduces to Eq. (2.6). An analysis of Eqs. (4.4) and (4.5) shows that since $A > 10^5$ in a typical op amp, the more accurate answers given by Eqs. (4.4) and (4.5) are nearly equal to those calculated using the *ideal* op-amp model. The same conclusion has been found to hold for the other circuits as well. Indeed, the measured driving-point characteristics in Figs. 3.9, 3.10, 3.12, and 3.14 all agree remarkably well with those predicted by the ideal op-amp model. This observation justifies our choice of the *ideal* op-amp model since the resulting analysis is usually much simpler.

Exercises

1. (*a*) Show that the linear two-port op-amp model in Fig. 4.3 has a *hybrid* representation. (*b*) Show that the *ideal* op-amp model in the linear region does *not* have a hybrid representation.
2. Some more accurate op-amp models used for high-precision circuit analysis has $i_- \neq -i_+$ in order to account for the small but nonzero currents entering the inverting and noninverting op-amp terminals. In this case, can you redraw the model as a two-port?
3. (*a*) Derive the driving-point and transfer characteristics of the negative-resistance converter circuit in Fig. 3.8 using the finite-gain op-amp model. (*b*) Show that the characteristics from (*a*) tend to those given in Fig. 3.8*b* and *c* as $A \to \infty$.

SUMMARY

- The op amp is a versatile four-terminal device which behaves like a nonlinear four-terminal resistor at dc. For low-frequency circuit applications, it can be modeled realistically by the *ideal op-amp model.*

- The *ideal op-amp model* is described by the following equations involving only its terminal voltages and currents (hence it is a four-terminal resistor by definition):

Ideal op-amp equations

$$i_- = 0$$

$$i_- = 0$$

$$v_o = E_{\text{sat}} \frac{|v_d|}{v_d}, \qquad v_d \neq 0$$

$$v_d = 0, \quad -E_{\text{sat}} < v_o < E_{\text{sat}}$$

where $v_d \triangleq v_- - v_-$.

- The ideal op-amp model has three distinct *operating regions*:

Linear region: $-E_{\text{sat}} < v_o < E_{\text{sat}}$
+ Saturation region: $v_d > 0$
− Saturation region: $v_d < 0$

The *ideal op-amp model* can also be uniquely represented by three *equivalent circuits* (see Fig. 1.6), each one corresponding to one operating region.

- In the *linear region*, the ideal op-amp model is described by

Ideal op-amp equations in the linear region

$$i_- = 0$$

$$i_- = 0$$

$$v_d = 0, \qquad -E_{\text{sat}} < v_o < E_{\text{sat}}$$

This model is equivalent to a *linear two-port* resistor where the input port behaves like an *open circuit* (zero input current) *and* a *short circuit* (zero input voltage) simultaneously. Hence, it is called a *virtual short-circuit model*. The output port behaves like a VCVS with an *infinite* gain.

- The *output* voltage v_o of the ideal op-amp model is *not* defined at $v_d = 0$ because it can assume *any* value between $-E_{\text{sat}}$ and E_{sat}. The actual output voltage is determined only by the *external* circuit constraints. Consequently, we say the *output* voltage v_o of the ideal op-amp model is a *multivalued* function of the input voltage v_d.
- In some situations where it is awkward to deal with *multivalued* functions, it may be more convenient to use the *finite-gain op-amp model* defined by

Finite-gain op-amp model

$$i_- = 0$$

$$i_+ = 0$$

$$v_o = f(v_d) \triangleq \frac{A}{2} |v_d + \epsilon| - \frac{A}{2} |v_d - \epsilon|$$