ESD Protection Circuits: Basics to nano-metric ASICs

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Outline

- Group Introduction
- ESD Basics
- Basic ESD Protection Circuits
- Nano-metric ESD Challenge
- ESD circuits for nano-metric regime
Group Introduction

- 5 PhDs, 2 masters and 2 PDFs
  - Applied, industrially driven research
  - Generous funding levels
- Core strengths in circuit design, testing, quality and reliability
Group: Low Power Research

- Driven by low power signal processing & bio-implantable applications
- Research focus
  - Active power reduction, clocking strategies
  - Dynamic voltage scaling architecture for portable app.
  - Leakage power reduction: Investigation of RBB effectiveness with scaling
Group: High Performance Circuits

- Driven by high speed arithmetic circuits (Adders, register files, ALU), and CDRs
- Research focus
  - To build timing diagnostics into multi-GHz ALUs
  - Leakage and active power reduction
  - Clock de-skewing
  - Thermal issues in high performance circuits
Group: Memory Research

- Driven by embedded SRAMs and Soft Error Robustness
- Research Focus
  - SRAM cell stability & ckt techniques for detection
  - Low power embedded SRAMs
  - Soft Error Robust memories & flip-flops
  - Error Correction Circuit’s for soft error mitigation
Group: ESD Research

- Driven by reducing chip failures due to ESD

- Research Focus
  - ESD strategies for multiple supply domains
  - ESD protection circuits for High speed I/Os
  - Fast response ESD protection circuits
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ESD Basics: Motivation

- Electrostatic Discharge (ESD) is responsible for up to 70% of failures in semiconductor industry.
- An ESD event creates high currents and electric fields in semiconductor devices.
  - High currents may lead to thermal runaway.
  - High electric fields cause dielectric breakdown.
ESD Basics

- When two dissimilar materials are separated an ESD charge may develop
- Caused by the removal of electrons from surface atoms of materials
- Factors
  - Magnitude of static charge
  - Contact quality
  - Rate of separation
Mimics the human touching of the Device Under Test (DUT)

Voltages as high as 10kV can be developed

HBM modeled by series resistance \((R_b = 1.5k\Omega)\) and capacitance \((C_b = 100pF)\)
Machine Model (MM)

- Represents the damage caused by charged machine touching the DUT
- Voltages as high as 100-500V can be generated
- MM is modeled by capacitance (C = 200pF) and series inductance of machine (0.5μH)
Charge Device Model (CDM)

- Discharge event between charged DUT and grounded conductor
- Modeled by Capacitor (Cap) in series with DUT
- Total Capacitance (Cap) is dependant on Device, package impedance
ESD Stress Comparison

- HBM rise time ~ 2-10ns, decay time 130-170ns
- CDM very high amplitude, occurs for 500ps-1000ps
- CDM failures on rise due to automated manufacturing
Zapping Modes

- Positive ESD with respect to $V_{SS}$ (PS-mode)
- Negative ESD with respect to $V_{SS}$ (NS-mode)
Zapping Modes

- Positive ESD with respect to $V_{DD}$ (PD-mode)
- Negative ESD with respect to $V_{DD}$ (ND-mode)
HBM / MM / CDM Testers

- HBM/MM/CDM testers apply ESD stress to the DUT
- Magnitude/polarity of the stress set by the user
- Test can be destructive
  - Results in pass or fail

- The device fails when leakage is increased significantly

ICMS-700 HBM/MM tester
TLP Tester

- Transmission Line Pulse (TLP) is becoming popular
  - Measures I-V characteristic of the DUT
  - Non-destructive
- Programmable current pulse of 100ns are applied to the DUT
- 2\textsuperscript{nd} breakdown current determines the ESD robustness

Barth 4002 TLP tester
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ESD Protection Methods

- **Snapback-based**
  - Turn on before oxide breakdown
  - Minimum parasitics

- **Non-snapback-based**
  - Trigger and conduct during the whole ESD event
  - Do not trigger under normal power-up
Diode Under ESD Conditions

- **Forward biased:**
  - Low trigger voltage
  - Low on resistance

- **Reverse biased:**
  - High trigger voltage
  - High on resistance
MOS Under ESD Conditions

- Has a parasitic bipolar transistor
  - Avalanche breakdown gives $I_{\text{gen}}$ and $I_{\text{sub}}$
  - When $V_{\text{base}} = 0.7V$, $n$pn turns on $\rightarrow$ Snapback
  - When $I(\text{drain}) = I_{t2}$, $n$pn can be destroyed
Snapback Protection: MOSFET

- MOSFET is used in Grounded-Gate configuration (GGNMOS)
  - Substrate and Gate triggering is often needed
ESD Protection Wish List

- $V_{t1} < \text{Oxide breakdown}$
  - To trigger NMOS before oxide breaks down
- $V_{t2} > V_{t1}$
  - To ensure uniform triggering of all fingers
- $V_h > V_{DD}$
  - To enhance latch-up immunity ($V_{DD} + 10\%$)
- $I_{t2}$ as high as possible
  - Increase current carrying capability $\rightarrow \uparrow\text{ESD}$

- A GGNMOS cannot meet all the above requirements for contemporary technologies
SCR Under ESD Conditions

- SCR is a \textit{pn}pn device
  - In CMOS the junctions are: p\textsuperscript{+}-nwell-psub-n\textsuperscript{+}
SCR Characteristic

- Avalanche breakdown of nwell-psub $\uparrow I_{Rnwell}$ and $I_{Rpsub}$
- When $V_{BE}$ reaches 0.7V, $nnp$ (or $pnp$) turns on
- Positive feedback turns on the $pnp$ (or $nnp$) $\rightarrow$ Snapback
ESD Devices: Comparison

- Protection level:
  - SCR and FB diode are the best

- Trigger voltage:
  - FB Diode is too low
  - NMOS is the best
  - SCR should be modified

- Holding voltage:
  - NMOS is ok
  - SCR should be modified

- Figure of merit
  - Protection level/Capacitance
Non-Snapback Protection: Clamps

- ESD event $\rightarrow V(1)$ rises turning on $M_0$
- $R_C C_C +$ inverter should keep $M_0$ “on” to discharge all ESD energy

**Advantages**
- Protect against different zapping conditions

**Disadvantages**
- Can turn on during normal power-up

ESD event:
- $t_r$: between 100ps and 60ns
- duration: up to 1μs

Regular power-up:
- In millisecond range

Hot plug app. power-up:
- as low as 1μs
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Challenges with Scaling

- Breakdown Voltage of CMOS devices is decreasing
  - Traditional ESD structures not scaling with technology scaling
- Larger ULSI, thinner metallization, shallower junctions
  - Increasingly difficult to provide low impedance, low capacitance discharge path
Challenges: Charged Device Model

- Lower Technologies (90nm, 65nm) damage occur at lower voltages
  - Traditional ESD circuits trigger slower
- High speed chips → larger package decoupling cap
  - Higher CDM discharge current!!
- CDM failures on rise due to automated manufacturing
Challenges: Multiple Supply Domains

- Multiple supply domains in SoC’s
  - Pin to pin ESD protection requirement
  - Multiple zapping modes
- Challenge to Overcome Noise Coupling & ground-bouncing issues between analog & digital supplies
Challenges: Multiple Chip Module

- Resistance of the path can be very high (Multiple Chip Module)
- Minimization of Parasitic Capacitance attributed to the High Speed I/O’s due to ESD Circuit
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Strategy – Device Simulation

- MOS models, circuit simulators are not designed to handle snapback behavior
- ESD circuits are designed with device simulators (Medici and Sequoia)
  - Device cross section is created in the simulator
  - Quasi-DC simulation predicts DC characteristic, i.e. $V_{t1}$ and $V_h$
  - $I_{t2}$ is estimated using thermal simulation and monitoring maximum temperature of the ESD protection device
Design Steps

1. Calibrate the device simulator with the desired technology
   - Junction depth and substrate doping are available from technology documents
2. Verify the technology model by simulating a MOS transistor
   - Trial and error is used to achieve the typical $I_{on}$, $V_{th}$, current gain and
3. Draw the cross-section of the ESD device
Mesh of the Low-Voltage-Triggered SCR (LVTSCR) created in Medici

Reducing grid spacing increases accuracy and simulation time
Snapback Protection Requirements

- Reduce first breakdown voltage
  - SCR has higher $V_{t1}$ compared to MOS
  - $V_{t1}$ of both MOS and SCR are higher than oxide breakdown voltage
- Latch-up immunity
  - Very important in SCR devices
- Increasing second breakdown current
  - SCR has higher $I_{t2}$ per width
- Reducing parasitic capacitance
- SCR provides protection with less capacitance

\[ (V_h, I_h) \quad (V_{t1}, I_{t1}) \quad (V_{t2}, I_{t2}) \]
Gate-Coupling

- $\uparrow V_{gs} \rightarrow \uparrow I_{sub} \rightarrow \text{nnp triggers faster} \rightarrow \downarrow V_{t1}$
- For higher $V_{gs}$ (strong inversion region): impact ionization is decreased $\rightarrow V_{t1}$ increases
Substrate Triggering

- \( V_{\text{sub}} \uparrow \rightarrow \text{Transistor triggers with lower}\ V_{t1} \downarrow \)
GST-LVTSCR

- SCR is modified by adding a gate electrode to reduce $V_{t1}$ (LVTSCR)
- $M_G$ provides gate triggering
  - Can be as small as 5$\mu$m
- $M_S$ provides substrate triggering
- Simulation results
  - $V_{t1}$ reduces from 12V to 4.85V

Semenov et. al., Microelectronics Reliability, 2005
GST-LVTSCR (Measurement)

- GST-LVTSCR was fabricated in 0.13μm CMOS technology
- TLP measurements
  - $V_{t1} = 5V$
  - $I_{t2} = 1.8A$
- HBM measurements
  - Device passes ±3kV
Example #2 – Increasing $V_h$

- In holding region both $Q_1$ and $Q_2$ are in saturation
- SCR
  \[ V_h = V_{EB1} + V_{CE2(sat)} \]
- High $V_h$ SCR ($R_E$ is added)
  \[ V_h = V_{EB1} + V_{CE(sat)} + R_E I_1 \]
  \[ V_h = V_{EB1} + V_{CE(sat)} + V_{EB1} R_E / R_{n-well} \]
- $R_E \uparrow \rightarrow V_h \uparrow$

Semenov et. al., ISQED, 2004
Increasing Holding Voltage

- Simulation results
  - Applied to SCR
  - $V_h$ is increased without an increase in $V_{t1}$
- $R_E$ is implemented with diode and MOS and applied to LVTSCR
- TLP Measurement results
  - $V_h$ is increased from 2.29V to 3.49V and 4.55V
  - Increase in $V_{t1}$ is less than 8%
Example #3 – ESD Clamps

- To solve false triggering, the triggering circuit is divided into rise time detector and delay element.
- Time constant is approximately 40ns.
- Delay of the delay element should be more than 1μs.
Thyristor-Based Clamp

- CMOS thyristor is used to create the delay element
- $R_C C_C = 40\text{ns}$
- $R_1$ to keep $M_0$ off under normal conditions

Hossein et. al., ESD Symposium 2007
Circuit-Level Simulation

- The clamp is circuit simulated with 2kV HBM stress
- V(3) shows that clamp turns off after 1μs
- Peak voltage of the clamp is less than 6V
Device-Level Simulation

- Device simulation is done with Sequoia
- Peak temperature is in transistor M₀
- During a 2kV HBM stress $T_{max}$ of the clamp is 375K
- Hot-spot is in the gate-drain boundary
Measurements

- Clamp was fabricated in 0.18μm technology
- HBM test
  - Clamp passes 3kV stress and fails at 3.5kV
- TLP test
  - Leakage current is 7nA
  - Second breakdown current is 1.8A
Example #4 – CML Driver Design

- Two stage 3Gbps CML driver is designed in 0.13μm CMOS tech.
- Bias of the driver is provided through an external resistor

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<thead>
<tr>
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<tbody>
<tr>
<td><strong>Diff. Input</strong></td>
<td>400mV</td>
</tr>
<tr>
<td><strong>Diff. Output</strong></td>
<td>800mV</td>
</tr>
<tr>
<td><strong>Rise/fall time</strong></td>
<td>150ps</td>
</tr>
<tr>
<td><strong>Jitter</strong></td>
<td>1ps</td>
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## Measured Results

<table>
<thead>
<tr>
<th></th>
<th>$V_{out}$</th>
<th>$t_r$</th>
<th>Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>CML (simulation)</td>
<td>850mV</td>
<td>116ps</td>
<td>229fs</td>
</tr>
<tr>
<td>CML+MOS (measured)</td>
<td>500mV</td>
<td>315ps</td>
<td>3.7ps</td>
</tr>
<tr>
<td>CML+LVTSCR (measured)</td>
<td>700mV</td>
<td>148ps</td>
<td>700fs</td>
</tr>
</tbody>
</table>

- Both Protection schemes achieved 3kV HBM protection

- Beyond $C_{ESD}=150fF$, jitter increases significantly

Hossein et. al., CICC 2007
Conclusion

- ESD remains major cause of chip failures
  - ESD affects entire manufacturing from devices → systems
- Significant challenges for nano-metric technologies
- ESD circuit design is an art
  - Device simulator are useful in design process
Acknowledgement

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