ASIC/FPGA Chip Design

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Assignment #5 – Winter 2014

For this assignment, please write a report describing all the details, show your work, attach all the Verilog codes, as well as the waveforms from the simulation results.

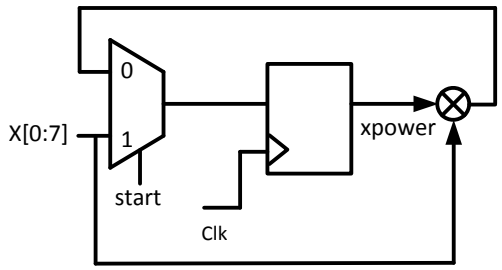
1- Consider the following recursive filter:

$$Y(n) = X(n) + aY(n-1)$$

a) Write a Verilog code to implement this filter. (A complete module that is synthesizable)
b) Show its corresponding architecture.
c) What is the critical path of the above architecture?
d) Come up with an architecture that implements the above filter with twice as much throughput.
e) Can we decrease the critical path with the simple pipelining technique? Why?
f) The pipelining technique can be applied to the above architecture with a minor modification to the above architecture. Show how to do it on the architecture to reduce the critical path and show the final pipelined design. (Hint: write the above equation for a few consecutive iterations).

2- Loop Unrolling using Pipelining to Improve Throughput

In this question, you are about to learn the loop unrolling technique. This technique is used to improve the throughput of a design. Let's assume that we want to calculate the fourth power of an 8-bit variable X, i.e., X^4. One way to do this is to use the following architecture,



where each power is calculated after four clock cycles.

a) What is the benefit of this design?
b) Write the RTL code to describe the above design
c) What is the throughput of the above architecture?

Now, we want to design a new architecture with a higher throughput but the same functionality.

d) Design a new architecture with a higher throughput. Use only coarse-grain pipelining

e) Write its RTL code.

f) Write a testbench and show the simulation results based on this testbench (using either Quartus or Modelism)

Since both of the above designs have non-zero latency, can you think of a design with zero latency?

g) Show your proposed architecture

h) What is the cost we pay to achieve zero latency?