FPGA Logic Cells Comparison

In this article we compare logic cells architectures that are used in modern FPGAs: Xilinx (both Virtex-5 and earlier), Altera and Actel.

Introduction

FPGA (Field Programmable Gate Array) is an integrated circuit containing a matrix of user-programmable logic cells, being able to implement complex digital circuitry.

These gates are designed to implement user-defined combinational and sequential functions. FPGA families from different vendors use different logic cells architecture.

Below you can find a short overview of different FPGA logic cells architectures, as well as an attempt to elaborate a universal method of their comparison.

Xilinx Slices (Virtex-4 and earlier)

The elementary programmable logic block in Xilinx FPGAs is called *slice.*

This architecture (with minor modifications) is used in all *Virtex* FPGA families before *Virtex-5* and all *Spartan* FPGA families so far (at least, up to *Spartan-3A*).

The Virtex-4 FPGA slice includes:

- Two **4-input LUTs** (Look-Up Tables) that can implement any 4-input boolean function, used as combinational function generators (one LUT is marked "F", the other one is marked "G").

- Two dedicated user-controlled **multiplexers** for combinational logic (MUXF5 and MUXFX). MUXF5 can be used to combine outputs of the slice's LUTs and so to implement 5-input combinational circuit. MUXFX is used to combine outputs of the other MUXF5 and MUXFX (from the other slices).

- Dedicated **arithmetic logic** (two 1-bit adders, carry chain and two dedicated AND gates for fast and efficient multiplication).

- Two **1-bit registers** that can be configured either as **flip-flops** or as **latches**. The input to these registers is selected by YMUX and XMUX multiplexers. Note that these multiplexers aren't user-controlled: the path is selected during FPGA programming.

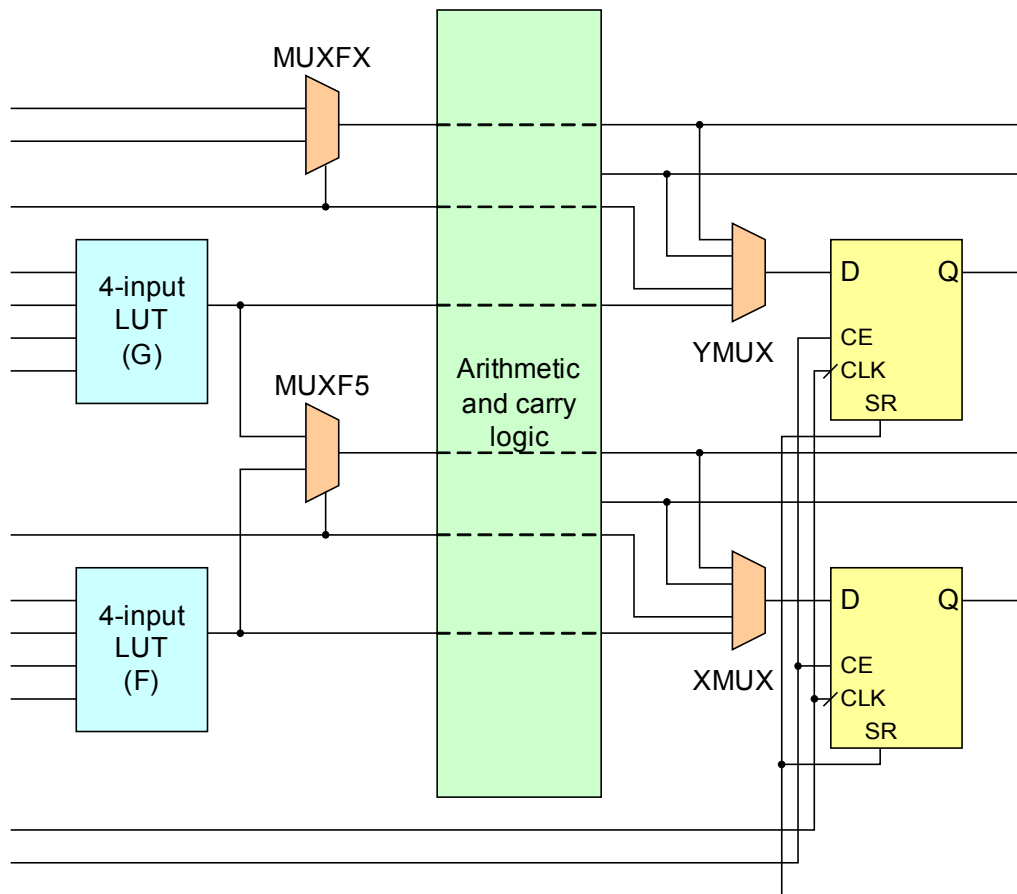The simplified diagram of a Virtex-4 slice is presented below.

Fig. 1: A simplified diagram of a Xilinx Virtex-4 FPGA slice

This 4-input LUT-based architecture became can be considered classic.

To implement a a 4-input LUT one need 16 bits of memory. Then, we can measure an amount of combinational logic that can be fitted in the slice by calculating the total number of LUT bits.

Xilinx Virtex-4 slice	
Combinational logic density (in LUT bits)	32
Register bits	2

Xilinx Virtex-5 Slices

The Virtex-5 slices include:

- *Four* **LUTs** (Look-Up Tables) that can be configured as 6-input LUTs with 1-bit output or 5-input LUTs with 2-bit output.

- *Three* dedicated user-controlled **multiplexers** for combinational logic (F7AMUX, F7BMUX and F8MUX). F7AMUX and F7BMUX combine outputs of the slice's LUTs to implement 7-input combinational circuits. F8MUX is used to combine outputs of the F7AMUX and F7BMUX.

- Dedicated **arithmetic logic** (two 1-bit adders and a carry chain).

- *Four* **1-bit registers** that can be configured either as **flip-flops** or as **latches**. The input to these registers is selected by AMUX – DMUX multiplexers. Note that these multiplexers aren't user-controlled: the path is selected during FPGA programming.

The main differences from the previous architecture:

- Configurable 6-to-1 or 5-to-2 LUTs instead of 4-to-1 LUTs.
- 4 LUTs and 4 register bits per slice.
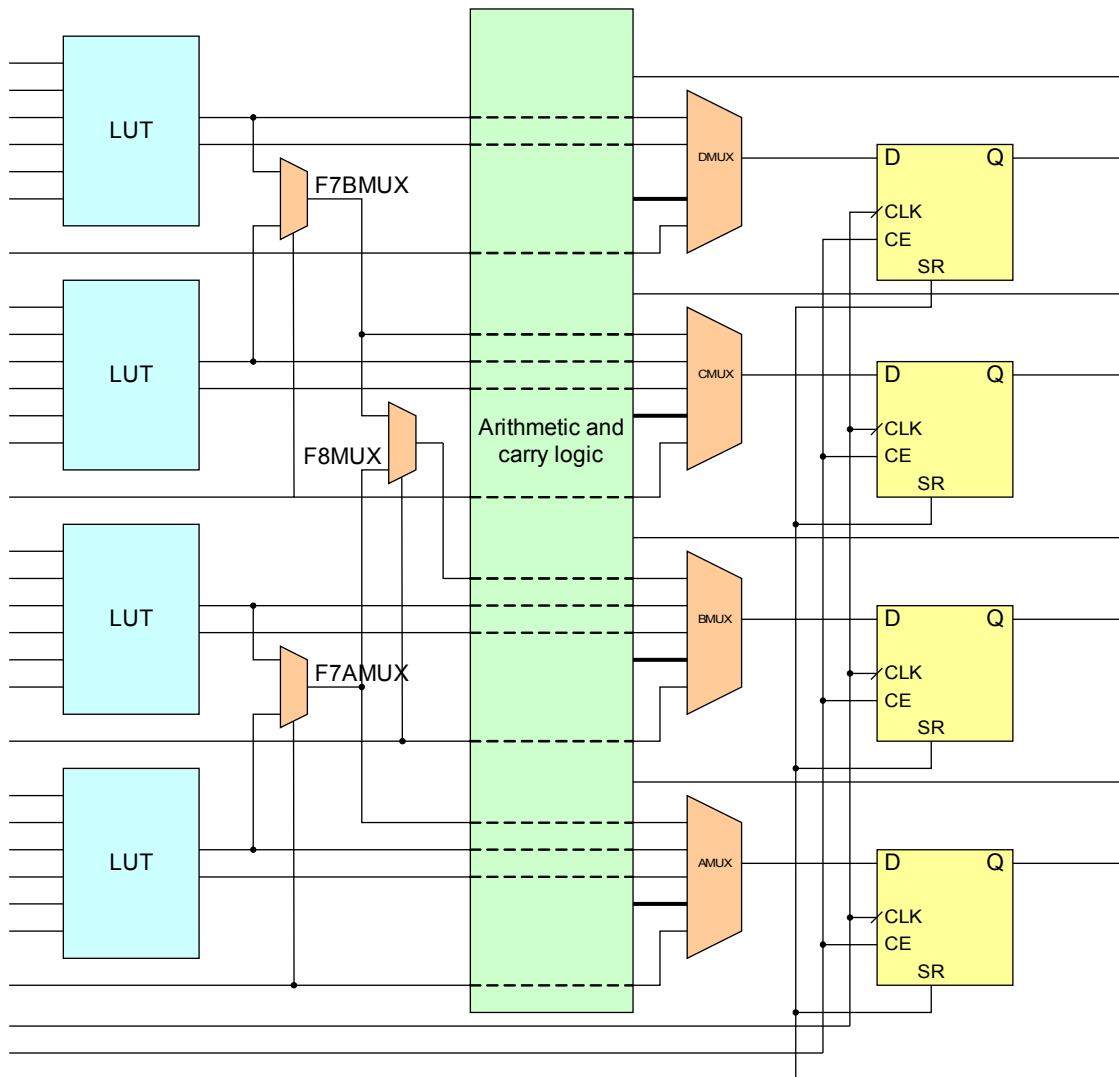- Dedicated arithmetic logic circuitry doesn't include dedicated AND gate.

Fig. 2: A simplified diagram of a Virtex-5 FPGA slice

For example, it is possible in Virtex-5 to implement a full 4-to-1 multiplexer with just one LUT.

Xilinx Virtex-5 slice	
Combinational logic density (in LUT bits)	256
Register bits	4

Altera ALMs

Altera FPGAs (*Stratix* and *Cyclone* families) uses slightly different logic blocks called "Adaptive Logic Modules" (ALMs).

ALM resources include:

- Two **4-input LUTs** and four **3-input LUTs** for combinational logic implementation.

- Dedicated **arithmetic and carry logic**.
- **Two programmable registers**.

It should be noted that an ALM has only 8 inputs, which is less than a total number of LUT inputs. This means that some input signals are connected to more than one LUT. There are several input signal multiplexers in the ALM that forms a kind of interconnect matrix programmable by the user (at the time of configuration). Note that not every connection is possible. Refer to the *Stratix-IV Device Handbook* for more details.
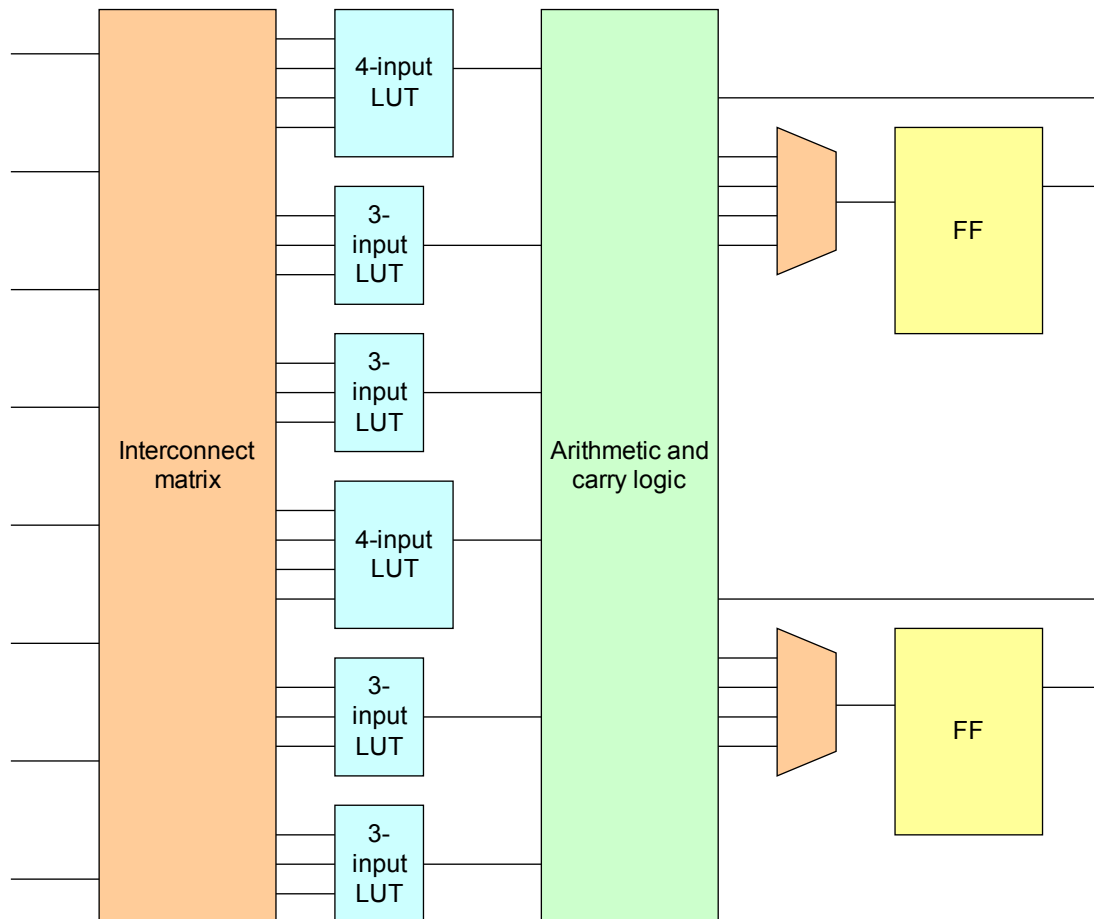

Fig. 3: A simplified diagram of the Altera ALM

Altera ALM	
Combinational logic density (in LUT bits)	64
Register bits	2

Actel VersaTile

Actel produces FPGAs mainly for aerospace and military applications. Compared with top Xilinx and Altera devices, Actel FPGAs provide less logic resources.

The basic building block for Actel flash-based FPGAs (such as *ProASIC-3*) is called *VersaTile*. Each VersaTile cell can implement any of the following:

- Any 3-input combinational logic function, OR
- D flip-flop or latch.

One VersaTile can implement only one of these, not both. Therefore, for the purpose of our comparison, we will divide LUT and register bits by 2.

Actel VersaTile	
Combinational logic density (in LUT bits)	4
Register bits	0.5

Conclusion

The architectures are very different, so it's difficult to compare them objectively. It should be understood that the results of such comparison have limited application.

It is usually the number of LUTs (and not the number of registers) that is a bottleneck for FPGA designs. From this perspective, it could be stated that one Virtex-5 slice can *in theory* substitute 8 Virtex-4 slices or 4 ALM's. But in real-world designs it is impossible to utilize all the resources.

Experiments with real-world designs show the following approximate relationship between different FPGA logic blocks:

Logic block	Virtex-4 slices equivalent
Xilinx Virtex-4 slice (reference)	1
Xilinx Virtex-5 slice	2
Altera ALM	1.3
Actel VersaTile	0.25