ASIC & FPGA Chip Design:

Introduction

Mahdi Shabany

Department of Electrical Engineering
Sharif University of technology
Course Code: 25776
Course Outline

• Course Outline
• Introduction to IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Course Outline

• Course Outline

• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Course Description

- How to go from Idea/Algorithm to the actual hardware

```verilog
module RippleCarryAdderII (Cin, X, Y, S, Cout);
    parameter n = 4; input Cin; input [n-1:0] X, Y; output [n-1:0] S;
    wire [n-1:0] C;
    Full_Adder stage0 (Cin, X[0], Y[0], S[0], C[1]);
    Full_Adder stage1 (C[1], X[1], Y[1], S[1], C[2]);
    Full_Adder stage2 (C[2], X[2], Y[2], S[2], C[3]);
    Full_Adder stage3 (.Cout(Cout), .Cin(C[3]), .x(X[3]), .y(Y[3]), .S(S[3]));
endmodule
```

ASIC

FPGA
Course Description

- Hardware Description Language (HDL) : Verilog
- Professional Verilog Coding for Synthesis
- Verification Techniques
- FPGA Architectures
- Digital System Design with Xilinx FPGAs
- ASIC Digital Design Flow (from Verilog to the actual Chip!)
- Synthesis Algorithms
- Power Dissipation
- Power Grid and Clock Design
- Fixed-point Simulation Methodology
- Xilinx Core Generator
Course Description:

1. HDL Coding
2. Simulation
3. Synthesis
4. Placement & routing
5. Timing Analysis & Verification

- In this course we learn all the above steps in detail for
  - ASIC Platform
  - FPGA Platform
Course Description:

- **Hardware Description Language**
  - **Verilog Fundamentals**
    - Language Fundamentals
    - Modeling Combinational/Sequential Logic Circuits
    - Modeling Finite State Machines
  - **Verilog for Verification**
    - Verification/Simulation techniques with test-benches
  - **Verilog for synthesis**
    - Verilog Styles for Synthesis
    - Architectural techniques for high-speed designs
      - Parallel proc., pipelining, retiming, ...
    - Implementations of common operations
      - Complex multiplication, division, complex norm, CORDIC
    - Fundamentals of fixed-point realization
Course Description:

- **PLDs & FPGA Architectures**
  - **FPGA Technologies**
    - SPLDs (PAL and PLA architectures)
    - Commercial CPLD Architectures
    - SRAM/LUT Based FPGAs
    - Anti-fuse/MUX Based FPGAs
    - Flash Based FPGAs
  - **FPGA Architectures**
    - Heterogeneous/Homogeneous FPGAs
    - Fine-grained, coarse-grained and platform FPGAs
  - **FPGA Elements & Design Trade-offs**
    - Logic Cells Common Architectures
    - Programmable Routing Channels Design
    - I/O & Pad architectures
  - **Commercial FPGAs**
    - Altera (FLEX 10K, Stratix III), Xilinx (XC4000, Virtex II,4,5), Actel (Act3, Axcelerator)
Course Description:

Advanced Digital System Design with Xilinx FPGAs

- Design Creation
- Synthesize
- Simulation
- Constraints Entry
- Implementation
- Implementation Results Analysis – Timing Analysis
- Implementation Results Analysis – Power Analysis
- Implementation Results Improvement
- Device Configuration and Programming
- Design Debugging
Course Description:

- **Core Generator**
  - CORE Generator Tool
  - Intellectual Property (IP) Cores
  - CORE Generator Tool files
  - Design Flows
  - Defining Memory Contents for RAM and ROM
  - Defining Coefficient Values in a COE File
Course Description:

- ASIC Design Flow:
  - HDL Coding & Verification
  - Synthesis & Timing Optimization
    - Complete Synopsys Design Compiler Design Flow
  - Physical Design
    - Cadence First Encounter
    - Floorplan (Initial floorplan and power planning)
    - Placement (Full-scale floorplan and clock tree insertion)
    - Routing (power routing & Nanoroute)
    - Timing Closure (Analysis & Optimization of setup and hold time violations)
    - Fill (Filler Cells, Metal Fill, and Verify Geometry)
Course Description:

- CAD Tool Algorithms:
  - Synthesis Algorithms
    - Two-level Optimization
    - Multi-level Logic Optimization
    - Technology Mapping
Course Description:

- Power Dissipation
  - Power Dissipation concept
  - Dynamic Power
  - Static Power
  - Challenges
Course Description:

- **Power Grid and Clock Design**
  - Power Distribution Design
    - Introduction
    - IR Drop
    - Ldi/dt Drop
  - Decoupling Capacitances
  - Clock Considerations
  - PLL/DLL Architecture
Course Description:

- **Prerequisites:**
  - Only Digital Logic!
  - All the skills you need will be taught in the course

- **Softwares you will learn:**
  - Altera Quartus
  - Xilinx ISE
  - Mentor Graphics Modelsim
  - TCL Scripting
  - Synopsys Design Compiler
  - Cadence SOC Encounter
Course Description:

- Implementation Platform:
  - Altera DE2 Board
  - Atlys Xilinx Board

- You will do several practical assignments including Verilog Coding, FPGA implementation and testing based on the DE2 and Atlys Boards
Course Description:

- **Assignments (8)**
  - 6 implementation assignments on DE2 Board (3 Marks)
  - 1 synthesis algorithms (3 marks)
  - 1 comprehensive project from A to Z (5 marks)

- **Workshop Labs on Xilinx Boards**

**Soft deadlines:** 20% daily penalty for the late submissions
### Course Evaluation:

<table>
<thead>
<tr>
<th>Section</th>
<th>Quantity</th>
<th>Value each</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assignments</td>
<td>7</td>
<td>3</td>
<td>21</td>
</tr>
<tr>
<td>Project</td>
<td>1</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>Midterm</td>
<td>1</td>
<td>26</td>
<td>30</td>
</tr>
<tr>
<td>Final Exam</td>
<td>1</td>
<td>40</td>
<td>40</td>
</tr>
</tbody>
</table>

**Total:** 100

If both the midterm and final marks are less than 50%, the total mark is calculated only based on the exams and assignments will not be taken into account.
Course Outline: References

- **HDL:**

- **IC Design Flow:**
  - Course Lecture notes, 2014
  - Digital IC Design Flow, provided by the instructor, 2014
Course Outline

• Course Outline

• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Integrated Circuit (IC) History

Discrete Circuits
- Limited applications
- Power hungry
- Large area
- Moderate speed

Integrated Circuits
- Many applications
- Low power
- Small area
- High speed
## Integrated Circuits (IC) History

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1940</td>
<td>Ohl built the PN Junction</td>
</tr>
<tr>
<td>1945</td>
<td>Shockley Lab was established</td>
</tr>
<tr>
<td>1947</td>
<td>Brattain and Bardeen invented the first transistor (US Patent 2524035)</td>
</tr>
</tbody>
</table>

*Image of the PN Junction and the filed patent.*

© M. Shabany, ASIC & FPGA Chip Design
Integrated Circuits (IC) History


1951: Shockley invented the first junction transistor for mass production

(US Patent 2623105)

A picture of the filed patent
Integrated Circuits (IC) History


Shockley українська Noyce: 1955
Hoerni українська Fairchild є частиною Noyce: 1957

Turk کرد Gorden Moore و

1958: تکنیکی را برای افشاندن ناخالصی‌ها به روزی ابداع کرد و به این Si توانست یک ترانزیستور مسطح با کمک عایق 2 بسازد

1959: اولین مدار مجتمع را با استفاده از ترانزیستورهای مسطح ساخت Noyce.
### Integrated Circuits (IC) History

<table>
<thead>
<tr>
<th>Year</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1940</td>
<td></td>
</tr>
<tr>
<td>1945</td>
<td></td>
</tr>
<tr>
<td>1947</td>
<td></td>
</tr>
<tr>
<td>1951</td>
<td></td>
</tr>
<tr>
<td>1955</td>
<td></td>
</tr>
<tr>
<td>1957</td>
<td></td>
</tr>
<tr>
<td>1958</td>
<td></td>
</tr>
<tr>
<td>1959</td>
<td></td>
</tr>
<tr>
<td>1961</td>
<td></td>
</tr>
<tr>
<td>1962</td>
<td></td>
</tr>
<tr>
<td>1968</td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td></td>
</tr>
<tr>
<td>1971</td>
<td></td>
</tr>
</tbody>
</table>
## Integrated Circuits (IC) History

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1940</td>
<td></td>
</tr>
<tr>
<td>1945</td>
<td></td>
</tr>
<tr>
<td>1947</td>
<td></td>
</tr>
<tr>
<td>1951</td>
<td></td>
</tr>
<tr>
<td>1955</td>
<td></td>
</tr>
<tr>
<td>1957</td>
<td></td>
</tr>
<tr>
<td>1958</td>
<td></td>
</tr>
<tr>
<td>1959</td>
<td></td>
</tr>
<tr>
<td>1961</td>
<td></td>
</tr>
<tr>
<td>1962</td>
<td></td>
</tr>
<tr>
<td>1968</td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td></td>
</tr>
<tr>
<td>1971</td>
<td></td>
</tr>
</tbody>
</table>

1961: 
Fairchild and TI produced the first ICs (50$).

1962: 
Ripple Carry Adder was invented by Fairchild.

Fairchild bipolar RTL Flip-Flop
RCA 16-transistor MOSFET IC

© M. Shabany, ASIC & FPGA Chip Design
### Integrated Circuits (IC) History

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1940</td>
<td></td>
</tr>
<tr>
<td>1945</td>
<td></td>
</tr>
<tr>
<td>1947</td>
<td></td>
</tr>
<tr>
<td>1951</td>
<td></td>
</tr>
<tr>
<td>1955</td>
<td></td>
</tr>
<tr>
<td>1957</td>
<td></td>
</tr>
<tr>
<td>1958</td>
<td></td>
</tr>
<tr>
<td>1959</td>
<td></td>
</tr>
<tr>
<td>1961</td>
<td></td>
</tr>
<tr>
<td>1962</td>
<td></td>
</tr>
<tr>
<td>1968</td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td></td>
</tr>
<tr>
<td>1971</td>
<td></td>
</tr>
</tbody>
</table>

- **1968**: Moore و Noyce را پایه گذاری کردند که Intel را راه‌آفرین کردند.
- **1970**: Fairchild Static RAMs 256-bit، Fairchild
- **1970**: Intel Dynamic RAMs 1-K bit، Intel

**Fairchild 4100 256-bit SRAM**

**Intel 1103 1K-bit DRAM**
# Integrated Circuits (IC) History

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1940</td>
<td></td>
</tr>
<tr>
<td>1945</td>
<td></td>
</tr>
<tr>
<td>1947</td>
<td></td>
</tr>
<tr>
<td>1951</td>
<td></td>
</tr>
<tr>
<td>1955</td>
<td></td>
</tr>
<tr>
<td>1957</td>
<td></td>
</tr>
<tr>
<td>1958</td>
<td></td>
</tr>
<tr>
<td>1959</td>
<td></td>
</tr>
<tr>
<td>1961</td>
<td></td>
</tr>
<tr>
<td>1962</td>
<td></td>
</tr>
</tbody>
</table>
| 1968 | Intel 4004 first introduced  
| 1970 | |  
| 1971 | |  

Intel 4004 first introduced in 1971.

The first commercially available microcomputer was introduced by Intel in 1971.

© M. Shabany, ASIC & FPGA Chip Design
IC History

Number of Transistors doubled every 18 months!

(Moore’s Law)
Scaling still continues...

Source: Intel

© M. Shabany, ASIC & FPGA Chip Design
IC History

1971 ................................................................................................................................................. 2010

- Amazingly visionary – million transistors/chip barrier was crossed in the 1980’s.
  - 2300 transistors, 1 MHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

Integration Levels

SSI: 10 gates
MSI: 1000 gates
LSI: 10,000 gates
VLSI: > 10k gates
IC History

Early Designs

- 1000 Transistors (1 MHz)
- Process: 10um
- Fully Handcrafted
- Manual Layout
- Individually Optimized

Advanced Designs

- Intel Corei7 (~ 1.6 GHz)
- Process: 32nm
- Fully Automated
- Automated Layout
- Hierarchical Design

(1971) to (2010)

Digital Very Large Scale Integration (VLSI) (Not Analog!)
Process Improvement

- Higher the density
- Lower the power
- More system Integration
- More Process Features

Power density too high to keep junctions at low temp

up frequency doubles every 2 years

© M. Shabany, ASIC & FPGA Chip Design
## Technology Direction

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size (nm)</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>$M$ trans/cm$^2$</td>
<td>7</td>
<td>14-26</td>
<td>47</td>
<td>115</td>
<td>284</td>
<td>701</td>
</tr>
<tr>
<td>Chip size (mm$^2$)</td>
<td>170</td>
<td>170-214</td>
<td>235</td>
<td>269</td>
<td>308</td>
<td>354</td>
</tr>
<tr>
<td>Signal pins/chip</td>
<td>768</td>
<td>1024</td>
<td>1024</td>
<td>1280</td>
<td>1408</td>
<td>1472</td>
</tr>
<tr>
<td>Clock rate (MHz)</td>
<td>600</td>
<td>800</td>
<td>1100</td>
<td>1400</td>
<td>1800</td>
<td>2200</td>
</tr>
<tr>
<td>Wiring levels</td>
<td>6-7</td>
<td>7-8</td>
<td>8-9</td>
<td>9</td>
<td>9-10</td>
<td>10</td>
</tr>
<tr>
<td>Power supply (V)</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>0.9</td>
<td>0.6</td>
<td>0.6</td>
</tr>
</tbody>
</table>
Why Scaling?

- Technology shrinks by ~0.7 per generation
- With every generation can integrate 2x more functions on a chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But ...
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years...
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction
IC Manufacturing Process

Silicon Cylinder

Unpackaged Die

Silicon Wafer

Patterned Silicon Wafer

Circuit Core

Packaged Die

Final Test

© M. Shabany, ASIC & FPGA Chip Design
Course Outline

• Course Outline
• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Digital vs. Analog Design: Analog Circuits

Transmitter:

- Voice
- Modulator
- High-frequency carrier
- Power Amplifier
- Analog/RF

Receiver:

- Low-Noise Amplifier
- Down Converter
- Demodulator
- Audio Amplifier
- Analog/RF
Digital vs. Analog Design: Analog-Digital Circuit

Transmitter:
- Voice
- ADC
- Voice Compression
- Coding Interleaving
- Pulse shaping
- Modulator
- Power Amplifier

Receiver:
- Low-Noise Amplifier
- Down Converter
- ADC
- Demodulator
- Equalizer
- De-interleaving
- De-Compression
- DAC
- Audio Amplifier

This Course
Digital vs. Analog Design

- Digital Design Advantages:
  - More noise reliability
  - Allows signal decoding and amplification
  - Allows coding to achieve higher performance
  - Allows encryption for higher security
  - Provides a perfect vehicle for digital signal processing
  - Allows modular chip design
  - Enjoys the benefit of advanced sophisticated CAD tools
  - Can be verified on programmable devices before tape-out
  - Provides a platform to merge multiple networks such as telephone, terrestrial TV and computer networks.
Digital vs. Analog Design

- **Digital processing systems** consist of a datapath, memory, and control. Early machines for arithmetic had insufficient memory, and often depended on users for control.

- Today’s digital systems are increasingly embedded into everyday places and things.

- Richer interaction with the user and environment.
Digital System Design Steps

- Specific application (e.g., Digital Image Processor)
  - As opposed to a general microprocessor
- Design requirements
  - Images to be processed per second
  - Required processing
  - Interfacing
  - Dimension, power, price, ...
- General design and simulation
- RTL level design to verify and simulate the design
- Higher levels: Few complicated blocks
- Lower levels: Many simple blocks
- To avoid any problem in lower levels, many simulations in higher levels
Design Flow

- Idea
- Architecture Design
- Block diagram
- Circuit & Layout Design
- Layout

IC Fabrication
- Wafer (hundreds of dies)
- Sawing & Packaging
- Final chips

Testing
- customers
- Bad chips
- Good chips

© M. Shabany, ASIC & FPGA Chip Design
Digital Systems Components

- Printed Circuit Board (PCB)
- Embedded Software
  - Microprocessor (general Purpose)
  - Microcontroller
  - Digital Signal Processor (DSP)
- Programmable Logic Devices
  - Simple Programmable Logic Device (SPLD)
  - Complex Programmable Logic Device (CPLD)
  - Field Programmable Gate Arrays (FPGAs)
- Application Specific Integrated Circuits (ASICs)
DSPs

- Easy to program (usually standard C)
- Very efficient for complex sequential math-intensive tasks
- Fixed datapath-width. Ex: 24-bit adder, is not efficient for 5-bit addition
- Limited resources
Digital Systems Components

Microprocessors/Microcontrollers

- Lessens the risk of system development by reducing design complexity
- Fixed hardware so more effort on developing a good code

- Fixed HW not suitable for high level of parallelism/computations
- Many sequential nature
- One order of magnitude less performance than to-date FPGA/ASICs
Digital Systems Implementation Platforms

Digital IC

- PLDs
  - SPLD
  - PLA
  - PAL
- CPLD
- FPGA
- Semi-Custom
  - Standard cell
- Full-Custom
  - Gate Array

ASIC

This course
The white portions of the timeline bars indicate that although early incarnations of these technologies may have been available, they weren’t enthusiastically received by the engineers working in the trenches during this period. For example, although Xilinx introduced the world’s first FPGA as early as 1984, design engineers didn’t really start using it until the early 1990s.
Course Outline

• Course Outline

• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
FPGA vs. ASIC

- **Field Programmable Gate Array (FPGA) Advantages:**
  - Fast programming and testing time by the end user (instant turn-around)
  - Excellent for prototyping
    - Easy to migrate from prototype to the final design
  - Can be re-used for other designs
  - Cheaper (in small volumes) → lower start-up costs
  - Re-programmable
  - Lower financial risk
  - Ease of design changes/modifications
  - Cheaper design tools
FPGA vs. ASIC

- **FPGA Drawbacks:**
  - Slower than ASIC (2-3 times slower)
  - Power hungry (up to 10 times more dynamic power)
  - Use more transistors per logic function
  - More area (20 to 35 times more area than a standard cell ASIC)
FPGA vs. ASIC

- **Application Specific Integrated Circuit (ASIC) Advantages:**
  - Faster
  - Lower power
  - Cheaper (if manufactured in large volumes)
  - Use less transistors per logic function

- **ASIC Drawbacks:**
  - Implements a particular design (not programmable)
  - Takes several months to fabricate (long turn-around)
  - More expensive design tools
  - Very expensive engineering/mask cost for the first successful design
The ASIC is accompanied by increasing nonrecurrent engineering (NRE) costs which meant that there was an increased emphasis on “right first time” design.

These NRE costs is largely due to the cost of generating masks as it is becoming more expensive to generate the masks for finer geometries needed by shrinking silicon technology dimensions.
Implementation Approaches (ASIC vs. FPGA)

ASIC
- Application Specific Integrated Circuit
- Expensive & time consuming fabrication in semiconductor foundry
- Designed all the way from behavioral description to physical layout

FPGA
- Field Programmable Gate Array
- Bought off the shelf & reconfigured by the end designers
- No physical layout design
- Design ends with a bitstream used to configure a device
Implementation Approaches (ASIC vs. FPGA)

**ASICs**

- High performance
- Low power
- Low cost in high volumes

**FPGAs**

- Off-the-shelf
- Low development cost
- Short time to market
- Re-configurability

© M. Shabany, ASIC & FPGA Chip Design
Course Outline

• Course Outline

• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Design Abstraction Levels

- **Divide-and-Conquer**
  - Design modules once
  - Instantiate them thereafter
  - Standard Cells
    - Already laid out
  - Avoid re-design
  - Same as programming

- **Designer cares about module’s:**
  - Functionality
  - Delay characteristics
  - Area

- **NOT:**
  - How the module was designed
  - Detailed solid-state behavior

© M. Shabany, ASIC & FPGA Chip Design
Design Abstraction Levels

**System Level**

- **I/O**
- **Processor**
- **RAM**
- **ROM**

**Algorithmic Level**

- \( A := A \times B + F \)
- \( \text{IF}(C = \text{TRUE}) \text{ THEN } A := A + 2 \times F \text{ ELSE } A := A - 1 \text{ ENDIF} \)

**Register Transfer Level**

- **MUX**
- **ALU**
- **Register**

**Logic Level**

- \&
- I
- C
- D
- Q
- Qn

**Circuit Level**

- Diagram of circuit components and interconnections.

---

© M. Shabany, ASIC & FPGA Chip Design
Device Metrics

Performance Metrics of a Digital Chip:

- **Cost**
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test

- **Speed**
  - Delay (ns) \(\rightarrow\) Operating Frequency (MHz)

- **Power Dissipation**

- **Energy to Perform a Function**
  - Energy per bit (nJ/b)

- **Reliability**
  - Noise immunity
  - Noise margin

- **Scalability**
  - Larger Designs

- **Time-to-Market**

Diameter: 10-30 cm
Thickness: 1 mm
Device Metrics

Performance Metrics of a Digital Chip:

- **Cost**
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test

- **Speed**
  - Delay (ns) → Operating Frequency (MHz)

- **Power Dissipation**

- **Energy to Perform a Function**
  - Energy per bit (nJ/b)

- **Reliability**
  - Noise immunity
  - Noise margin

- **Scalability**
  - Larger Designs

- **Time-to-Market**
Cost of Integrated Circuits

- **NRE (non-recurring engineering) costs**
  - Fixed cost to produce the design
    - Design effort
    - Design verification effort
    - Mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products

- **RE (Recurring costs) – proportional to the product volume (i.e., Variable)**
  - Silicon processing
    - also proportional to chip area
  - Assembly (packaging)
  - Test

\[
\text{Cost per IC} = \frac{\text{variable cost per IC}}{\text{volume}} + \frac{\text{fixed cost}}{\text{volume}}
\]
Recurring Costs

variable cost = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}

cost of die = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}

\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}

die yield = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}

\alpha \text{ depends on the complexity of the manufacturing process (roughly proportional to the number of masks)}
Yield Example

Example

- Wafer size of 12 inches, die size of 2.5 cm², 1 defects/cm²,
  - $\alpha = 3$ (measure of manufacturing process complexity)
- 252 dies/wafer (remember, wafers round & dies square)
- Die yield of 16%
- $252 \times 16\% = \text{only 40 dies/wafer die yield!}$

Die cost is a strong function of the die area

- Proportional to the third or fourth power of the die area

Cost of die = $f(\text{die area})^4$
# Examples of Cost Metrics (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Defects /cm²</th>
<th>Area (mm²)</th>
<th>Dies /wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>PowerPC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super SPARC</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
Device Metrics

Performance Metrics of a Digital Chip:

- **Cost**
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test

- **Speed**
  - Delay (ns) → Operating Frequency (MHz)

- **Power Dissipation**

- **Energy to Perform a Function**
  - Energy per bit (nJ/b)

- **Reliability**
  - Noise immunity
  - Noise margin

- **Scalability**
  - Larger Designs

- **Time-to-Market**
Performance

- Frequency of operation: $1/T$
  - Dependent on the propagation delay of signal through the logic
  - Time to get the data out/in of the registers
  - Clock uncertainty

- $t_p$ is a typical measure (not an accurate one)
  - The delay experienced by a signal when passing through a gate
  - 50% transition points of the input and output waveforms
    - Two types LH and HL
    - Good for comparison

- Rise time/fall time affects delay
  - 10% - 90% definitions
Delay Definitions

\[ t_p = \frac{t_{pHL} + t_{pLH}}{2} \]

Propagation delay

Signal slopes

\[ t_f, t_r \]

Input waveform

Output waveform
Performance Metrics of a Digital Chip:

- **Cost**
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test

- **Speed**
  - Delay (ns) → Operating Frequency (MHz)

- **Power Dissipation**

- **Energy to Perform a Function**
  - Energy per bit (nJ/b)

- **Reliability**
  - Noise immunity
  - Noise margin

- **Scalability**
  - Larger Designs

- **Time-to-Market**
Power Consumption

- **Peak transient power**
  - Power line sizing, decoupling, etc.
  
  \[ P_{\text{peak}} = i_{\text{peak}} V_{\text{supply}} = \max[p(t)] \]

- **Average power**
  - Battery current delivery, cooling system

- **Static power vs. Dynamic power**
  - Static current ➔ no computation, etc
  - Dynamic current ➔ Switching on/off the gates
    - The higher the number of switching events, the higher the dynamic power consumption

- **Dynamic Energy ➔** Amount of energy that is needed to be spent to do a job
  - Time is no matter
Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate
- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
  - Power-delay product (PDP) – energy consumed by the gate per switching event
- An ideal gate is the one that is fast and consumes little energy, so the ultimate quality metric is
  - Energy-delay product (EDP) = power-delay
Device Metrics

Performance Metrics of a Digital Chip:

- **Cost**
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test

- **Speed**
  - Delay (ns) → Operating Frequency (MHz)

- **Power Dissipation**

- **Energy to Perform a Function**
  - Energy per bit (nJ/b)

- **Reliability**
  - Noise immunity
  - Noise margin

- **Scalability**
  - Larger Designs

- **Time-to-Market**
Noise: unwanted variations of voltages and currents at the logic nodes

- from two wires placed side by side
  - Capacitive coupling
    - Voltage change on one wire can influence signal on the neighboring wire
    - Cross talk
  - Inductive coupling
    - Current change on one wire can influence signal on the neighboring wire

- from noise on the power and ground supply rails
  - May influence signal levels in the gate
Noise Margins

- For robust circuits, want the “0” and “1” intervals to be as large as possible.

\[
\begin{align*}
\text{Noise Margin High:} & \quad NM_H = V_{OH} - V_{IH} \\
\text{Noise Margin Low:} & \quad NM_L = V_{IL} - V_{OL}
\end{align*}
\]

Noise margin represents the levels of noise that can be sustained when gates are cascaded.

© M. Shabany, ASIC & FPGA Chip Design
Noise Immunity

- **Noise margin** expresses the ability of a circuit to overpower a noise source
  - Noise sources: supply noise, cross talk, interference, offset

- Absolute noise margin values are deceptive
  - Floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)

- **Noise immunity** expresses the ability of the system to process and transmit information correctly in the presence of noise (noise rejection)

- For good noise immunity, the signal swing (i.e., the difference between $V_{OH}$ and $V_{OL}$) and the noise margin have to be large enough to overpower the impact of fixed sources of noise
Course Outline

- Course Outline
- Introduction to ASIC/FPGA IC Design
  - Integrated Circuits (IC) History
  - Digital Design vs. Analog Design
  - ASIC vs. FPGA
  - Design Abstraction and Metrics
  - CMOS as the building block of Digital ASICs
  - Layout
  - Packaging
MOS Device Theory

- **Bipolar Junction Transistor (BJT)**
  - Small current in Base drives a larger current b/w Emitter & Collector.
  - Quiescent power dissipation due to the Base current
  - High power dissipation limits the number of transistors on a single chip
  - Not suitable for Very Large Scale Integration (VLSI)

- **Metal Oxide Semiconductor Field Effect Transistors (MOSFET)**
  - Come with almost zero control current (Gate voltage controls the drain current)
  - Higher integration
  - Much lower power consumption than BJT
  - Come in two flavors: n-MOS (n-type dopants), p-MOS (p-type dopants)

- **Complementary Metal Oxide Semiconductor (CMOS)**
  - Utilizing both n-MOS and p-MOS transistors

© M. Shabany, ASIC & FPGA Chip Design
MOS Device Theory

- Transistors are built on a silicon substrate
- Silicon is a Group IV material \( \rightarrow \) covalent bonds with 4 adjacent atoms
- Silicon is a poor conductor \( \rightarrow \) can be raised by adding dopants

**n-type**
- Group V dopants
- Five valence electrons
- Extra electron free to move
- Negative carrier
- Example:
  - Arsenic, Phosphorus

**p-type**
- Group III dopants
- 3 valence electrons
- Missing electron (hole) free to move
- Positive carrier
- Example:
  - Boron
MOS Device Theory

- Four terminals:
  1. Gate
  2. Source
  3. Drain
  4. Body

- Consists of:
  - Gate (Metal (old), Polysilicon (now))
  - Insulating layer (SiO₂ (oxide-glass))
  - Source (n+ in nMOS, p+ in pMOS)
  - Drain (n+ in nMOS, p+ in pMOS)
  - Body (conductor)
  - n+: Heavily doped n-type
  - P+: Heavily doped p-type
nMOS Transistors

- Gate–oxide–body stack looks like a capacitor

- **Body** is commonly tied to ground (0 V)

- **Gate** at low voltage:
  - Body is at low voltage
  - Source-body diode is OFF
  - Drain-body diode is OFF
  - No current flows
  - Transistor is OFF
nMOS Transistors

- **Gate** at high voltage:
  - Positive charge on gate
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Current flow in this channel b/w source and drain when drain voltage is nonzero
  - Transistor is **ON**
pMOS Transistors

- Similar to nMOS with reversed doping and voltages
- Body is commonly tied to high voltage (VDD)
- Gate low: transistor **ON**
- Gate high: transistor **OFF**
- Bubble indicates inverted behavior
MOS Transistors

- L is the channel length
- L: Process parameter, technology
- Smaller L → Faster transistors → higher speed circuits
- Typical process values: 0.35μm, 0.18μm, 0.13μm, 90nm, 60nm, ...
- VDD decreases by technology
  - 1.5 V for 0.18 μm
  - 1.2 V for 0.13 μm
- Lower VDD saves power consumption
- GND = 0 V
CMOS

- Silicon wafer is the base material
  - Diameter: 10-30 cm
  - Thickness: 1 mm

- CMOS: both nMOS and pMOS transistors fabricated on a single wafer
- Wells: special regions to separate bulks of nMOS and pMOS
CMOS

- Substrate must be tied to GND and n-well to VDD
- Poor connection of metal to lightly-doped semiconductor (Shottky Diode)
- Use heavily doped well and substrate contacts

Top View

Cross Section along Dashed Line

GND
V_{DD}

V_{DD}

© M. Shabany, ASIC & FPGA Chip Design
CMOS

ارزان

• اتصال به

• زمین مشترک

ارزان

اتصال به

• بزرگترین منبع

گران

• دو درجه آزادی

• ایزوله از

Twin-WELL

© M. Shabany, ASIC & FPGA Chip Design
Course Outline

• Course Outline

• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Layout

- Chips are specified with set of masks.
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power).
- “Feature size” \( L_{\text{min}} \) = distance between source and drain (channel) (minimum width of Polysilicon)
- Feature size improves 30% every 3 years or so.
- Can integrate 2\( \times \) more functions per chip \( \rightarrow \) \( \sim \) 2\( \times \) less cost per function.
- Normalize for feature size when describing design rules \( (\lambda = L_{\text{min}} / 2) \)
  - E.g., \( \lambda = 90\text{nm} \) in 0.18 \( \mu \text{m} \) process.
Layout Layers

- Each layout consists of various levels described by different colors.
Design Rules

- Circuit engineer designs a circuit
- Process engineer fabricates the design
- DRC: constraints on patterns in terms of minimum width and separation
- DRC: guarantees that the circuit to be manufacturable
Digital VLSI Layout

- Designed and laid-out standard cells
- They are placed & abutted in a chip

Several metal layers used for routing

Metal 1

Metal 2

Via 12
Digital VLSI Layout

- Standard cells are automatically placed and routed using different metal layers through the corresponding CAD tools.
Chip Floorplan

- Start with the pin count (# of I/O and VDD, VSS pads)
- Pads are already designed (provided in the design kit)
Chip Floorplan: Pads

VDD/GND wires form continuous ring through the pad frame.

Spacer pad if no signal.

Layout View

Design View
Course Outline

• Course Outline
• Introduction to ASIC/FPGA IC Design
  ➢ Integrated Circuits (IC) History
  ➢ Digital Design vs. Analog Design
  ➢ ASIC vs. FPGA
  ➢ Design Abstraction and Metrics
  ➢ CMOS as the building block of Digital ASICs
  ➢ Layout
  ➢ Packaging
Packaging

- **Package:**
  - Die interface to outside world
  - Removes heat from chip
  - Mechanical support
  - Protects die against humidity
  - Introduces delay/parasitics to the chip

- **Advanced Package Requirements:**
  - **Electrical:** Low Parasitics
  - **Mechanical:** Reliable and Robust
  - **Thermal:** Efficient Heat Removal
  - **Economical:** Cheap
Die to Package Substrate

Wire Bonding
- Small pin count
- Must be attached serially
- Large inductance
- Cross talk b/w wires
- Pads on four sides of the chip

Flip-Chip Bonding
- Large pin count
- Connections made simultaneously
- Superior electrical performance
- Small cross talk
- Pads at any position on the chip
Packaging

- Package-Socket-PCB interconnection:

- Performance bottlenecks:
  - Chip itself
  - Package
  - Socket
  - Board
Package/Socket to Board Interconnection

**Through-Hole Mounting**
- ✓ Mechanically reliable
- ❌ Low package density
- ❌ Limits routing on the board
  - ▪ Dualin-Line (DIP) (up to 64 pins)
  - ▪ PGA (up to 400 pins)

**Surface Mount**
- ✓ More wiring space
- ✓ Higher package density
- ✓ Chips at both sides of the board
- ❌ Weak chip-board connection
- ❌ Non-accessible pins for testing
Package/Socket to Board Interconnection

- For very large pin-counts, even surface-mount packaging is not enough!
  - Ball Grid Array (BGA)

Solder bumps are used to connect both the die to the package substrate and the package to the board.
Packaging Material/Type

- **Package Material:**
  - Plastics (cheaper)
  - Ceramic (Better heat removal)

- **Package Types:**
  - 84-pin PLCC
  - 14-pin DIP
  - 44-pin PLCC
  - 86-pin TSOP
  - 280-pin QFP
  - 387-pin PGA Multichip Module
  - 560-pin BGA
  - 40-pin DIP
  - 296-pin PGA
Packaging Types

- Pin Grid Array (PGA)
- Quad Flat Pack (QFP)
- Ball Grid Array (BGA)
- Plastic Leader Chip Carrier (PLCC)