Digital VLSI Architecture

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Assignment #1 - Fall 2011

DVB Standard PHY Implementation (Phase I)

Due Date: Mehr 24, 1390

- Consider the Figure 1 of the DVB standard in page 10. In this phase of the standard implementation we would like to implement the first two blocks of the system, i.e., MUX adaptation Energy dispersal. Please perform the following steps

    1) Read Sections 4.3.1 and 4.3.2 (Only the Outer coding for this phase) of the Standard.

    2) The definition of a packet is brought in Figure 3.a on page 13 of the Standard. Generate a random input of length 100 packets.

    3) Implement the MUX adaptation Energy dispersal in both Matlab and Verilog.
        a) In Matlab show that your code is working properly by providing the input signal and golden output as a text file.
        b) In Verilog write the modules as well as the testbenches to simulate the core. The simulation has to be done using Modelsim.

    4) Implement the inverse of the MUX adaptation and RS decoding at the receiver side.
        - Show that your Matlab and Verilog codes can generate the original input signal at the transmitter side. To support this in Matlab, write a wrapper that calls the transmitter and receiver codes and compares the detected bits with the original transmitted bit stream.

    5) Write a report describing all the required steps.

    6) All the codes should be provided at the end as a soft copy of your project.

    7) Support your implementation platform with references you used for.