Digital VLSI Architecture

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Assignment #2 - Fall 2011

Pipelining and Parallel Processing

Due Date: Aban 1, 1390

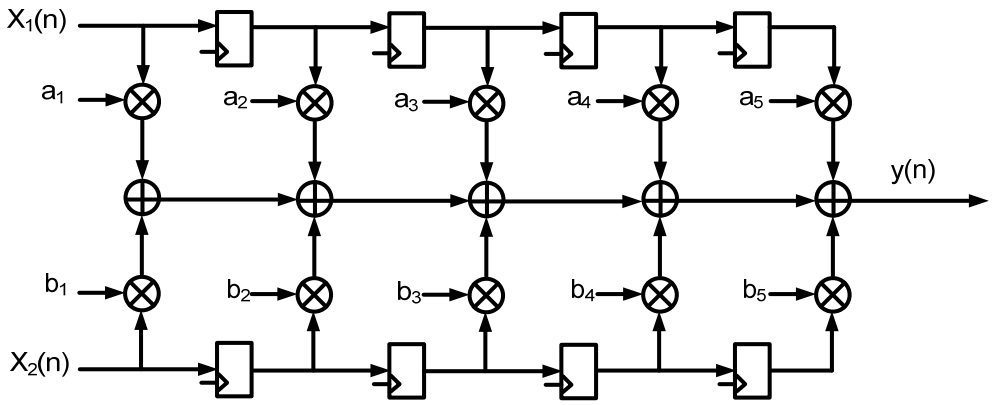
1. Consider a direct-form implementation of the FIR filter

$$y(n) = ax(n) + bx(n-2) + cx(n-3).$$

Assume that the time required for 1 multiply-add operation is T.

(a) Pipeline this filter such that the clock period is approximately T.
(b) Draw a block filter architecture for a block size of three (i.e., parallel factor 3). Pipeline this block filter such that the clock period is about T. What is the system sample rate?
(c) Pipeline the block filter in part (b) such that the clock period is about T/2. Show the appropriate cutsets and label the outputs clearly. What is the system sample rate now?

2. Consider the non-recursive signal processing structure shown below. Find an equivalent data-broadcast implementation of this algorithm to improve the speed of the system. Do not use any additional latches. Calculate the throughput or sample speed of the broadcast architecture.



3. Consider a datapath with a total capacitance of C_{total}. This datapath is pipelined by M levels. Let C_{latch} represent the total capacitance of the latches used for 1 pipelining stage. The pipelined system is operated with lower supply voltage to reduce the power consumption. Assume both systems are operated at same speed and assume the propagation delay of the latch to be negligible. Let C_{total} = 10 C_{latch}, VDD = 4 V and V_t =0.6 V. Calculate the power consumption of the pipelined system as a percentage of that of the sequential system for different values of M. What is the optimal M for least power consumption? (Find the solution using Matlab and provide the curves required to justify your answer).