Digital VLSI Architectures

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Spring 1388-1389
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Description & Aim:

Comprehensive understanding of the digital design flow, including the algorithmic level issues, architecture optimization, hardware description languages, as well as the digital Application Specific Integrated Circuit (ASIC) design concerns in the transistor/system level is extremely important for today's digital designers. This course is designed to address most of these issues through lectures, projects and lab assignments. The course will give insight on how to get from a signal processing algorithm to an efficient VLSI implementation using various architectural techniques while considering a given set of criteria. In fact, the course provides a practical understanding of the implementation strategies for digital ICs, existing VLSI technologies, fundamentals of digital ASIC design, RTL coding for synthesis, common digital signal processing algorithms, efficient techniques for floating-point and fixed-point simulations, as well as VLSI techniques for high-speed/low-power designs. The main part of the course will be focused on the design of application specific architectures that can be implemented on either reconfigurable hardware, e.g. Field Programmable Gate Arrays (FPGAs), or ASIC. State-of-the-art design tools will be used to support the course work. As a part of the course requirement is a term project on the design and ASIC implementation (full chip) of a digital sub-system, which is assigned at the beginning of the semester and will be completed in parallel to the lectures.

Tools:

- Synopsys DC, First Encounter, Quartus II, ISE, MATLAB, C++

Course Composition:

- Lectures, Seminars, Assignments, Project, Midterm, Final exam.

References:

- K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, 1999.
- S. Y. Kung, VLSI Array Processors, Prentice Hall, 1988.
- Lars Wanhammer, *DSP Integrated Circuits.* San Diego: Academic Press, 1999.
- M. J. Smith, ``*Application-Specific Integrated Circuits*'', Addison Wesley, ISBN 0-201-50022-1.
- D. E. Thomas, ``*The Verilog Hardware Description Language*'', 3rd edition, Kluwer Academic.
- W. F. Lee, "*Verilog coding for logic synthesis*", Wiley-interscience, 2003.
- H. Bhatnagar, "Advanced ASIC Chip Synthesis Using Synopsys DC, Physical Compiler & PrimeTime".
- Major IEEE journals and conferences.

Prerequisites:

- Verilog, MATLAB, Signals and Systems, Digital Logic.

1. VLSI Technology and ASIC Design

- **Implementation Strategies for Digital ICs**
  - o CAD Tool for ASICs
  - o Full-Custom/Custom ASICs
  - o Custom FPGA Platforms
- **Digital ASIC Design**
  - o Issues in Digital Integrated Circuit Design
  - o Quality Metrics of Digital Designs
  - o Digital IC Components
  - o Timing Issues in Digital ICs

2. VLSI Digital Signal Processing Architectures

- **Introduction to Digital Signal Processing Systems**
  - o Typical DSP Algorithms (FFT, DFT, LMS, RLS,…)
  - o Representation of Signal Processing Algorithms
  - o Signal-flow, Data-flow and Dependence Graphs
  - o Iteration Bound
- **VLSI Architecture Techniques**
  - o Pipelining
  - o Parallel Processing
  - o Pipelining and Parallel Processing for Low Power Design
  - o Retiming Techniques
  - o Unfolding
  - o Folding
  - o Register Minimization Techniques
  - o Systolic Architecture Design
  - o FIR Systolic Arrays
- **Synchronous and Asynchronous Pipeline**
  - o Synchronous Pipeline and Clocking Styles
  - o Wave Pipelining
  - o Asynchronous Pipeline
  - o Implementation of Computational Units
- **Bit-Level Arithmetic Architectures**
  - o Arithmetic Circuits Number Systems and their Effect on Implementation
  - o Redundant, Floating-point Representations/Operations
  - o Shifters/Adders/ Comparators
  - o Parallel/Bit-serial Multipliers
- **Redundant Arithmetic**
- **Finite Word Length Effect**
- **Floating-point to Fixed-point simulation techniques**
- **Parallel and Pipelined Digital Filter Design**
- **Low-Power Design**