BJT Amplifier Circuits

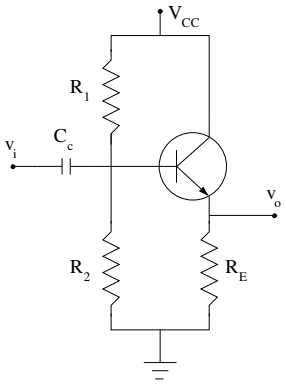
As we have developed different models for DC signals (simple large-signal model) and AC signals (small-signal model), analysis of BJT circuits follows these steps:

DC biasing analysis: Assume all capacitors are open circuit. Analyze the transistor circuit using the simple large signal mode as described in pages 77-78.

AC analysis:
1) Kill all DC sources
2) Assume coupling capacitors are short circuit. The effect of these capacitors is to set a lower cut-off frequency for the circuit. This is analyzed in the last step.
3) Inspect the circuit. If you identify the circuit as a prototype circuit, you can directly use the formulas for that circuit. Otherwise go to step 4.
4) Replace the BJT with its small signal model.
5) Solve for voltage and current transfer functions and input and output impedances (node-voltage method is the best).
6) Compute the cut-off frequency of the amplifier circuit.

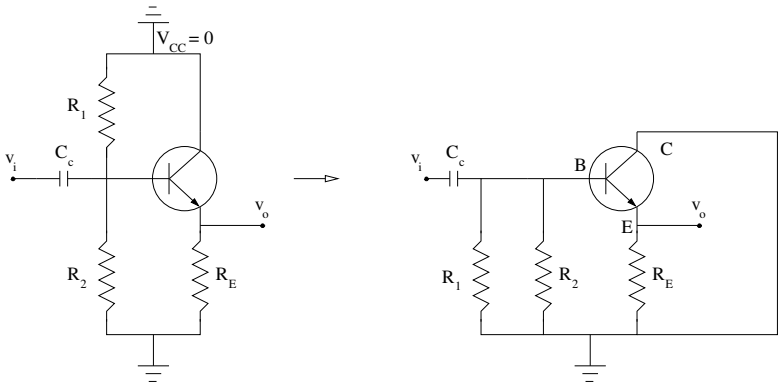
Several standard BJT amplifier configurations are discussed below and are analyzed. For completeness, circuits include standard bias resistors R_1 and R_2. For bias configurations that do not utilize these resistors (*e.g.,* current mirror), simply set $R_B = R_1 \parallel R_2 \to \infty$.

Common Collector Amplifier (Emitter Follower)

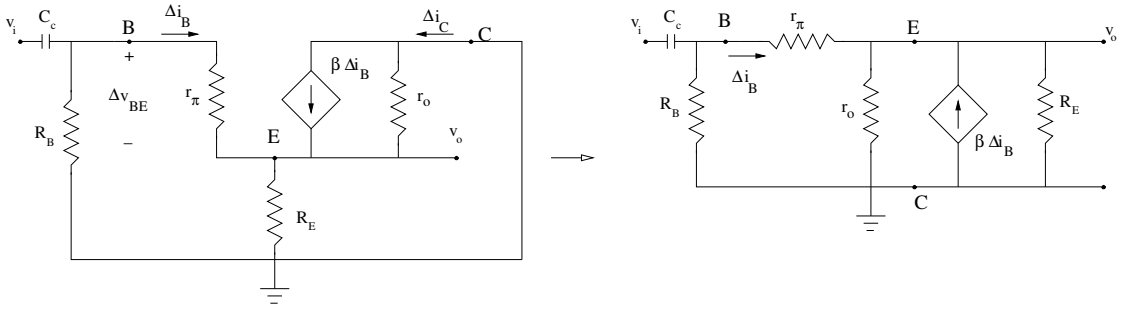


DC analysis: With the capacitors open circuit, this circuit is the same as our good biasing circuit of page 110 with $R_C = 0$. The bias point currents and voltages can be found using procedure of pages 110-112.

AC analysis: To start the analysis, we kill all DC sources:



We can combine R_1 and R_2 into R_B (same resistance that we encountered in the biasing analysis) and replace the BJT with its small signal model:



The figure above shows why this is a common collector configuration: collector is shared between input and output AC signals. We can now proceed with the analysis. Node voltage method is usually the best approach to solve these circuits. For example, the above circuit will have only one node equation for node at point E with a voltage v_o:

$$\frac{v_o - v_i}{r_\pi} + \frac{v_o - 0}{r_o} - \beta \Delta i_B + \frac{v_o - 0}{R_E} = 0$$

Because of the controlled source, we need to write an "auxiliary" equation relating the control current (Δi_B) to node voltages:

$$\Delta i_B = \frac{v_i - v_o}{r_\pi}$$

Substituting the expression for Δi_B in our node equation, multiplying both sides by r_π, and collecting terms, we get:

$$v_i(1+\beta) = v_o \left[1 + \beta + r_\pi \left(\frac{1}{r_o} + \frac{1}{R_E}\right)\right] = v_o \left[1 + \beta + \frac{r_\pi}{r_o \parallel R_E}\right]$$

Amplifier Gain can now be directly calculated:

$$A_v \equiv \frac{v_o}{v_i} = \frac{1}{1 + \dfrac{r_\pi}{(1+\beta)(r_o \parallel R_E)}}$$

Unless R_E is very small (tens of Ω), the fraction in the denominator is quite small compared to 1 and $A_v \approx 1$.

To find the input impedance, we calculate i_i by KCL:

$$i_i = i_1 + \Delta i_B = \frac{v_i}{R_B} + \frac{v_i - v_o}{r_\pi}$$

Since $v_o \approx v_i$, we have $i_i = v_i/R_B$ or

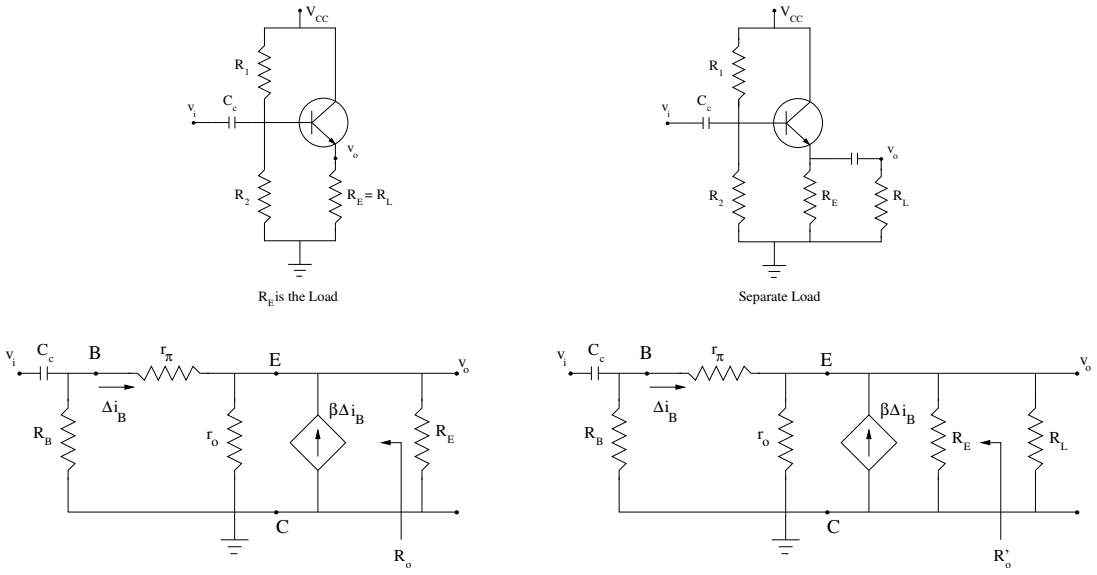
$$R_i \equiv \frac{v_i}{i_i} = R_B$$

Note that R_B is the combination of our biasing resistors R_1 and R_2. With alternative biasing schemes which do not require R_1 and R_2, (and, therefore $R_B \to \infty$), the input resistance of the emitter follower circuit will become large. In this case, we cannot use $v_o \approx v_i$. Using the full expression for v_o from above, the input resistance of the emitter follower circuit becomes:

$$R_i \equiv \frac{v_i}{i_i} = R_B \parallel [r_\pi + (R_E \parallel r_o)(1+\beta)]$$

and it is quite large (hundreds of kΩ to several MΩ) for $R_B \to \infty$. Such a circuit is in fact the first stage of the 741 OpAmp.

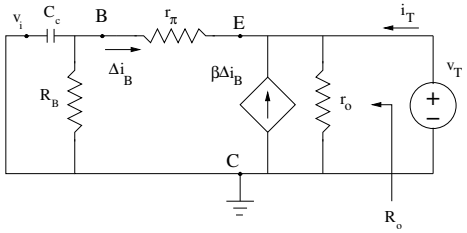
The output resistance of the common collector amplifier (in fact for all transistor amplifiers) is somewhat complicated because the load can be configured in two ways (see figure): First, R_E, itself, is the load. This is the case when the common collector is used as a "current amplifier" to raise the power level and to drive the load. The output resistance of the circuit is R_o as is shown in the circuit model. This is usually the case when values of R_o and A_i (current gain) is quoted in electronic text books.



Alternatively, the load can be placed in parallel to R_E. This is done when the common collector amplifier is used as a buffer ($A_v \approx 1$, R_i large). In this case, the output resistance is denoted by R'_o (see figure). For this circuit, BJT sees a resistance of $R_E \parallel R_L$. Obviously, if we want the load not to affect the emitter follower circuit, we should use R_L to be much

larger than R_E. In this case, little current flows in R_L which is fine because we are using this configuration as a buffer and not to amplify the current and power. As such, value of R'_o or A_i does not have much use.

When R_E is the load, the output resistance can be found by killing the source (short v_i) and finding the Thevenin resistance of the two-terminal network (using a test voltage source).



$$\text{KCL:} \qquad i_T = -\Delta i_B + \frac{v_T}{r_o} - \beta \Delta i_B$$

$$\text{KVL (outside loop):} \qquad -r_\pi \Delta i_B = v_T$$

Substituting for Δi_B from the 2nd equation in the first and rearranging terms we get:

$$R_o \equiv \frac{v_T}{i_T} = \frac{(r_o)\, r_\pi}{(1+\beta)(r_o) + r_\pi}$$

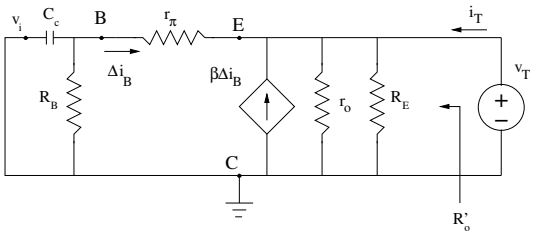
Since, $(1+\beta)(r_o) \gg r_\pi$, the expression for R_o simplifies to

$$R_o \approx \frac{(r_o)\, r_\pi}{(1+\beta)(r_o)} = \frac{r_\pi}{(1+\beta)} \approx \frac{r_\pi}{\beta} = r_e$$

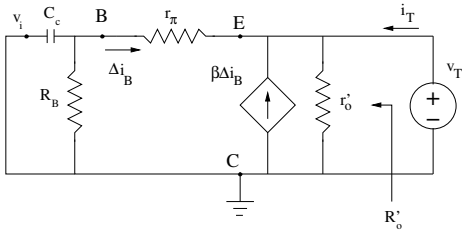
As mentioned above, when R_E is the load the common collector is used as a "current amplifier" to raise the current and power levels . This can be seen by checking the current gain in this amplifier: $i_o = v_o/R_E$, $i_i \approx v_i/R_B$ and

$$A_i \equiv \frac{i_o}{i_i} = \frac{R_B}{R_E}$$

We can calculate R'_o, the output resistance when an additional load is attached to the circuit (*i.e.,* R_E is not the load) with a similar procedure: we need to find the Thevenin resistance of the two-terminal network (using a test voltage source).



We can use our previous results by noting that we can replace r_o and R_E with $r'_o = r_o \parallel R_E$ which results in a circuit similar to the case with no R_L. Therefore, R'_o has a similar expression as R_O if we replace r_o withr'_o:



$$R'_o \equiv \frac{v_T}{i_T} = \frac{(r'_o)\, r_\pi}{(1+\beta)(r'_o) + r_\pi}$$

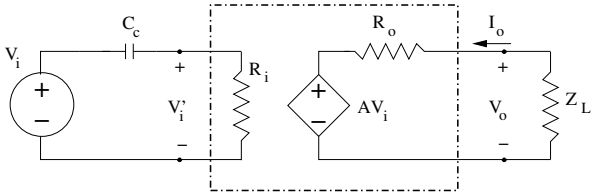
In most circuits, $(1+\beta)(r'_o) \gg r_\pi$ (unless we choose a small value for R_E) and $R'_o \approx r_e$

In summary, the general properties of the common collector amplifier (emitter follower) include a voltage gain of unity ($A_v \approx 1$), a very large input resistance $R_i \approx R_B$ (and can be made much larger with alternate biasing schemes). This circuit can be used as buffer for matching impedance, at the first stage of an amplifier to provide very large input resistance (such in 741 OpAmp). The common collector amplifier can be also used as the last stage of some amplifier system to amplify the current (and thus, power) and drive a load. In this case, R_E is the load, R_o is small: $R_o = r_e$ and current gain can be substantial: $A_i = R_B/R_E$.

Impact of Coupling Capacitor:

Up to now, we have neglected the impact of the coupling capacitor in the circuit (assumed it was a short circuit). This is not a correct assumption at low frequencies. The coupling capacitor results in a lower cut-off frequency for the transistor amplifiers. In order to find the cut-off frequency, we need to repeat the above analysis and include the coupling capacitor impedance in the calculation. In most cases, however, the impact of the coupling capacitor and the lower cut-off frequency can be deduced be examining the amplifier circuit model.

Consider our general model for any amplifier circuit. If we assume that coupling capacitor is short circuit (similar to our AC analysis of BJT amplifier), $v'_i = v_i$.



Voltage Amplifier Model

When we account for impedance of the capacitor, we have set up a high pass filter in the input part of the circuit (combination of the coupling capacitor and the input resistance of the amplifier). This combination introduces a lower cut-off frequency for our amplifier which is the same as the cut-off frequency of the high-pass filter:

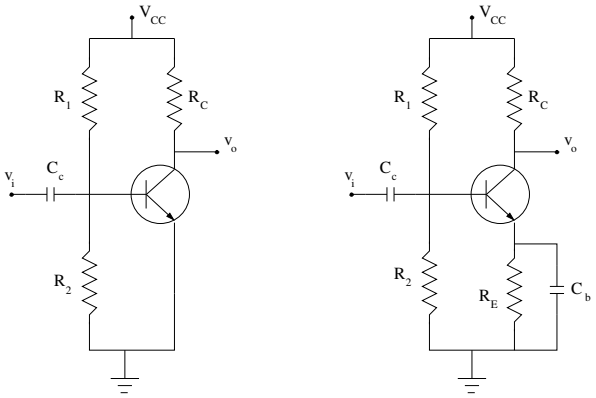
$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c}$$

Lastly, our small signal model is a low-frequency model. As such, our analysis indicates that the amplifier has no upper cut-off frequency (which is not true). At high frequencies, the capacitance between BE , BC, CE layers become important and a high-frequency small-signal model for BJT should be used for analysis. You will see these models in upper division

courses. Basically, these capacitances results in amplifier gain to drop at high frequencies. PSpice includes a high-frequency model for BJT, so your simulation should show the upper cut-off frequency for BJT amplifiers.

Common Emitter Amplifier

DC analysis: Recall that an emitter resistor is necessary to provide stability of the bias point. As such, the circuit configuration as is shown has as a poor bias. We need to include R_E for good biasing (DC signals) and eliminate it for AC signals. The solution to include an emitter resistance and use a "bypass" capacitor to short it out for AC signals as is shown.



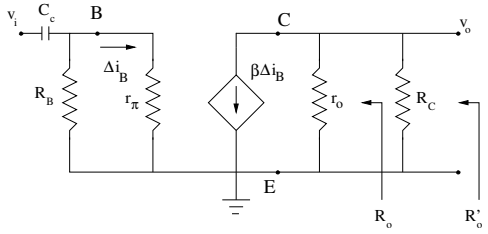
For this new circuit and with the capacitors open circuit, this circuit is the same as our good biasing circuit of page 110. The bias point currents and voltages can be found using procedure of pages 110-112.

AC analysis: To start the analysis, we kill all DC sources, combine R_1 and R_2 into R_B and replace the BJT with its small signal model. We see that emitter is now common between input and output AC signals (thus, common emitter amplifier. Analysis of this circuit is straightforward. Examination of the circuit shows that:

$$v_i = r_\pi \Delta i_B \qquad v_o = -(R_C \parallel r_o)\,\beta \Delta i_B$$

$$A_v \equiv \frac{v_o}{v_i} = -\frac{\beta}{r_\pi}(R_C \parallel r_o) \approx -\frac{\beta}{r_\pi} R_C = -\frac{R_C}{r_e}$$

$$R_i = R_B \parallel r_\pi$$



The negative sign in A_v indicates 180° phase shift between input and output. The circuit has a large voltage gain but has a medium value for input resistance.

As with the emitter follower circuit, the load can be configured in two ways: 1) R_C is the load; or 2) load is placed in parallel to R_C. The output resistance can be found by killing the source (short v_i) and finding the Thevenin resistance of the two-terminal network. For this circuit, we see that if $v_i = 0$ (killing the source), $\Delta i_B = 0$. In this case, the strength of

the dependent current source would be zero and this element would become an open circuit. Therefore,

$$R_o = r_o \qquad R'_o = R_C \parallel r_o$$

Lower cut-off frequency: Both the coupling and bypass capacitors contribute to setting the lower cut-off frequency for this amplifier, both act as a high-pass filter with:

$$\omega_l(coupling) = 2\pi\, f_l = \frac{1}{R_i C_c}$$
$$\omega_l(bypass) = 2\pi\, f_l = \frac{1}{R'_E C_b}$$
$$\text{where} \quad R'_E \equiv R_E \parallel r_e$$

Note that usually $R_E \gg r_e$ and, therefore, $R'_E \approx r_e$.

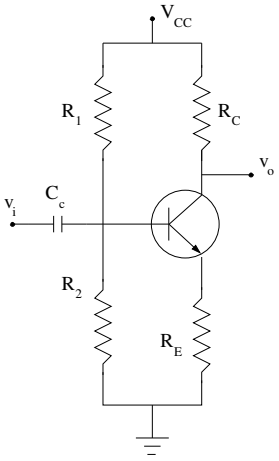
In the case when these two frequencies are far apart, the cut-off frequency of the amplifier is set by the "larger" cut-off frequency. *i.e.,*

$$\omega_l(bypass) \ll \omega_l(coupling) \quad \rightarrow \quad \omega_l = 2\pi\, f_l = \frac{1}{R_i C_c}$$
$$\omega_l(coupling) \ll \omega_l(bypass) \quad \rightarrow \quad \omega_l = 2\pi\, f_l = \frac{1}{R'_E C_b}$$

When the two frequencies are close to each other, there is no exact analytical formulas, the cut-off frequency should be found from simulations. An approximate formula for the cut-off frequency (accurate within a factor of two and exact at the limits) is:

$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

Common Emitter Amplifier with Emitter resistance



A problem with the common emitter amplifier is that its gain depend on BJT parameters $A_v \approx (\beta/r_\pi)R_C$. Some form of feedback is necessary to ensure stable gain for this amplifier. One way to achieve this is to add an emitter resistance. Recall impact of negative feedback on OpAmp circuits: we traded gain for stability of the output. Same principles apply here.

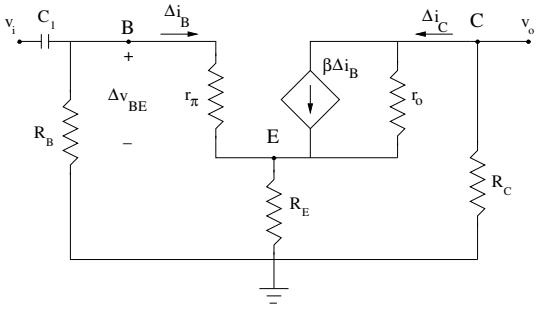
DC analysis: With the capacitors open circuit, this circuit is the same as our good biasing circuit of page 110. The bias point currents and voltages can be found using procedure of pages 110-112.

AC analysis: To start the analysis, we kill all DC sources, combine R_1 and R_2 into R_B and replace the BJT with its small signal model. Analysis is straight forward using node-voltage method.

$$\frac{v_E - v_i}{r_\pi} + \frac{v_E}{R_E} - \beta\Delta i_B + \frac{v_E - v_o}{r_o} = 0$$

$$\frac{v_o}{R_C} + \frac{v_o - v_E}{r_o} + \beta\Delta i_B = 0$$

$$\Delta i_B = \frac{v_i - v_E}{r_\pi} \quad \text{(Controlled source aux. Eq.)}$$



Substituting for Δi_B in the node equations and noting $1 + \beta \approx \beta$, we get :

$$\frac{v_E}{R_E} + \beta\frac{v_E - v_i}{r_\pi} + \frac{v_E - v_o}{r_o} = 0$$

$$\frac{v_o}{R_C} + \frac{v_o - v_E}{r_o} - \beta\frac{v_E - v_i}{r_\pi} = 0$$

Above are two equations in two unknowns (v_E and v_o). Adding the two equation together we get $v_E = -(R_E/R_C)v_o$ and substituting that in either equations we can find v_o. Using $r_\pi/\beta = r_e$, we get:

$$A_v = \frac{v_o}{v_i} = \frac{R_C}{r_e(1 + R_C/r_o) + R_E(1 + r_e/r_o)} \approx \frac{R_C}{r_e(1 + R_C/r_o) + R_E}$$

where we have simplified the equation noting $r_e \ll r_o$. For most circuits, $R_C \ll r_o$ and $r_e \ll R_E$. In this case, the voltage gain is simply $A_v = -R_C/R_E$.

The input resistance of the circuit can be found from (prove it!)

$$R_i = R_B \parallel \frac{v_i}{\Delta i_B}$$

Noting that $\Delta i_B = (v_i - v_E)/r_\pi$ and $v_E = -(R_E/R_C)v_o = -(R_E/R_C)A_v v_i$, we get:

$$R_i = R_B \parallel \frac{r_\pi}{1 + A_v R_C/R_E}$$

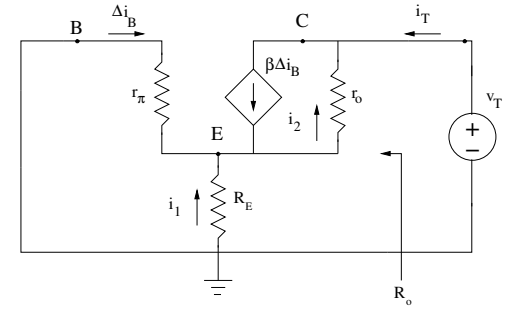
Substituting for A_v from above (complete expression for A_v with $r_e/r_o \ll 1$), we get:

$$R_i = R_B \parallel \left[\beta\left(\frac{R_E}{1 + R_C/r_o} + r_e\right)\right]$$

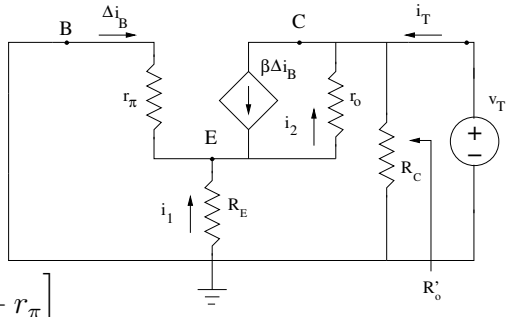
For most circuits, $R_C \ll r_o$ and $r_e \ll R_E$. In this case, the input resistance is simply $R_i = R_B \parallel (\beta R_E)$.

As before the minus sign in A_v indicates a 180° phase shift between input and output signals. Note the impact of negative feedback introduced by the emitter resistance: The voltage gain is independent of BJT parameters and is set by R_C and R_E (recall OpAmp inverting amplifier!). The input resistance is also increased dramatically.

As with the emitter follower circuit, the load can be configured in two ways: 1) R_C is the load. 2) Load is placed in parallel to R_C. The output resistance can be found by killing the source (short v_i) and finding the Thevenin resistance of the two-terminal network (by attaching a test voltage source to the circuit).



Resistor R_B drops out of the circuit because it is shorted out. Resistors r_π and R_E are in parallel. Therefore, $i_1 = (r_\pi/R_E)\Delta i_B$ and by KCL, $i_2 = (\beta + 1 + r_\pi/R_E)\Delta i_B$. Then:



$$i_T = -\Delta i_B - i_1 = -\Delta i_B\left(1 + \frac{r_\pi}{R_E}\right)$$

$$v_T = -\Delta i_B r_\pi - i_2 r_o = -\Delta i_B\left[r_o\left(\beta + 1 + \frac{r_\pi}{R_E}\right) + r_\pi\right]$$

Then:

$$R_o = \frac{v_T}{i_T} = r_o + R_E \times \frac{1 + r_o/r_e}{1 + R_E/r_\pi}$$

where we have used $r_\pi/\beta = r_e$. Generally $r_o \gg r_e$ (first approximation below) and for most circuit, $R_E \ll r_\pi$ (second approximation) leading to

$$R_o \approx r_o + r_o \times \frac{R_E/r_e}{1 + R_E/r_\pi} \approx r_o + \frac{R_E r_o}{r_e} = r_o \left(\frac{R_E}{r_e} + 1 \right)$$

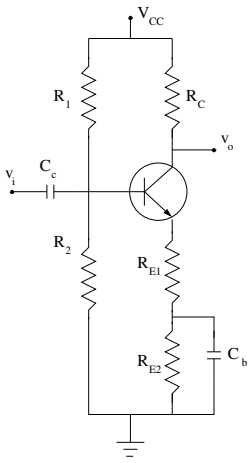
Value of R'_o can be found by a similar procedure. Alternatively, examination of the circuit shows that

$$R'_o = R_C \parallel R_o \approx R_C$$

Lower cut-off frequency: The coupling capacitor together with the input resistance of the amplifier lead to a lower cut-off frequency for this amplifier (similar to emitter follower). The lower cut-off frequency is given by:

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c}$$

A Possible Biasing Problem: The gain of the common emitter amplifier with the emitter resistance is approximately R_C/R_E. For cases when a high gain (gains larger than 5-10) is needed, R_E may be become so small that the necessary good biasing condition, $V_E = R_E I_E > 1$ V cannot be fulfilled. The solution is to use a by-pass capacitor as is shown. The AC signal sees an emitter resistance of R_{E1} while for DC signal the emitter resistance is the larger value of $R_E = R_{E1} + R_{E2}$. Obviously formulas for common emitter amplifier with emitter resistance can be applied here by replacing R_E with R_{E1} as in deriving the amplifier gain, and input and output impedances, we "short" the bypass capacitor so R_{E2} is effectively removed from the circuit.



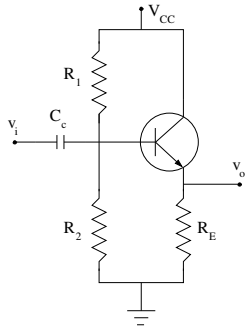
The addition of by-pass capacitor, however, modifies the lower cut-off frequency of the circuit. Similar to a regular common emitter amplifier with no emitter resistance, both the coupling and bypass capacitors contribute to setting the lower cut-off frequency for this amplifier. Similarly we find that an approximate formula for the cut-off frequency (accurate within a factor of two and exact at the limits) is:

$$\omega_l = 2\pi f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

$$\text{where} \quad R'_E \equiv R_{E2} \parallel (R_{E1} + r_e)$$

Summary of BJT Amplifiers*

Common Collector (Emitter Follower):



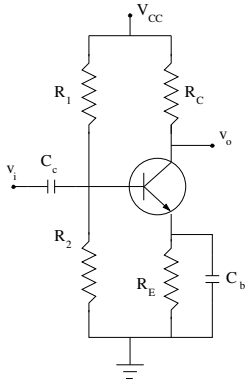
$$A_v = \frac{(R_E \parallel r_o)(1+\beta)}{r_\pi + (R_E \parallel r_o)(1+\beta)} \approx 1$$

$$R_i = R_B \parallel [r_\pi + (R_E \parallel r_o)(1+\beta)] \approx R_B$$

$$R_o = \frac{(r_o)\, r_\pi}{(1+\beta)(r_o) + r_\pi} \approx \frac{r_\pi}{\beta} = r_e \qquad 2\pi\, f_l = \frac{1}{R_i C_c}$$

$$R_o' = \frac{(r_o')\, r_\pi}{(1+\beta)(r_o') + r_\pi} \approx \frac{r_\pi}{\beta} \qquad \text{where} \quad r_o = r_o \parallel R_C$$

Common Emitter:



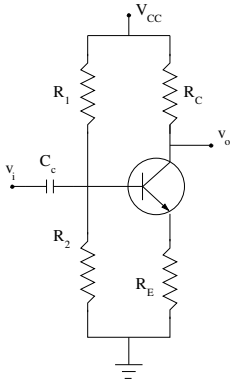
$$A_v = -\frac{\beta}{r_\pi}(R_C \parallel r_o) \approx -\frac{\beta}{r_\pi} R_C = -\frac{R_C}{r_e}$$

$$R_i = R_B \parallel r_\pi$$

$$R_o = r_o \qquad R_o' = R_C \parallel r_o \approx R_C$$

$$2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R_E' C_b} \qquad \text{where} \quad R_E' \equiv R_E \parallel r_e$$

Common Emitter with Emitter Resistance:



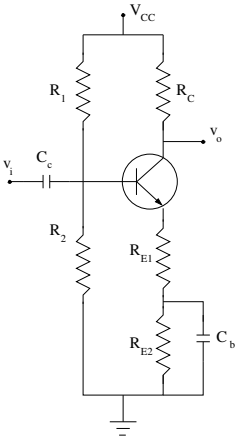
$$A_v = -\frac{R_C}{r_e(1 + R_C/r_o) + R_E} \approx -\frac{R_C}{r_e + R_E} \approx -\frac{R_C}{R_E}$$

$$R_i = R_B \parallel \left[\beta\left(\frac{R_E}{1 + R_C/r_o} + r_e\right)\right] \approx R_B \parallel \beta R_E \approx R_B$$

$$R_o \approx r_o + r_o \times \frac{R_E/r_e}{1 + R_E/r_\pi} \approx r_o\left(\frac{R_E}{r_e} + 1\right)$$

$$R_o' = R_C \parallel R_o \approx R_C \qquad \text{and} \quad 2\pi\, f_l = \frac{1}{R_i C_c}$$

Replace R_E with R_{E1} in the above formulas except



$$2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R_E' C_b}$$

where $\quad R_E' \equiv R_{E2} \parallel (R_{E1} + r_e)$

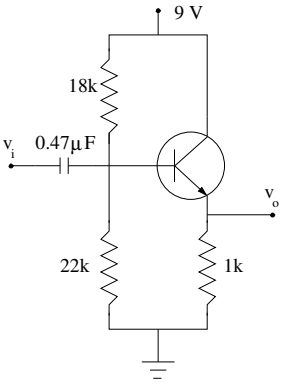
*If bias resistors are not present (*e.g.,* bias with current mirror), let $R_B \to \infty$ in the "full" expression for R_i.

Examples of Analysis and Design of BJT Amplifiers

Example 1: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $h_{fe} = 200$, $h_{ie} = 5$ kΩ, $h_{oe} = 10$ μS).

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad \beta = h_{fe} = 200 \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$

DC analysis:



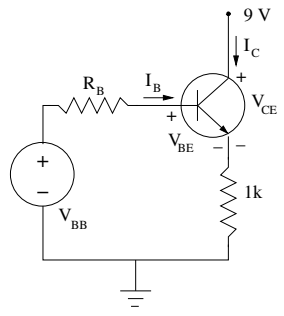
Replace R_1 and R_2 with their Thevenin equivalent and proceed with DC analysis (all DC current and voltages are denoted by capital letters):

$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega$$

$$V_{BB} = \frac{22}{18+22} 9 = 4.95 \text{ V}$$

KVL: $V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$4.95 - 0.7 = I_E \left(\frac{9.9 \times 10^3}{201} + 10^3 \right)$$



$$I_E = 4 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 20 \ \mu\text{A}$$

KVL: $V_{CC} = V_{CE} + 10^3 I_E$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$

DC Bias summary: $I_E \approx I_C = 4$ mA, $\quad I_B = 20$ μA, $\quad V_{CE} = 5$ V

AC analysis: The circuit is a common collector amplifier. Using the formulas in page 134,

$$A_v \approx 1$$

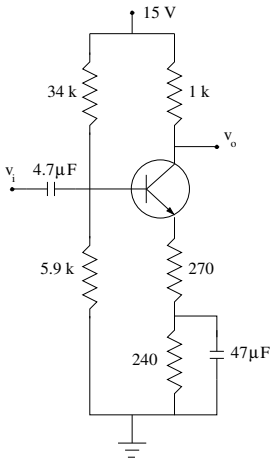
$$R_i \approx R_B = 9.9 \ k\Omega$$

$$R_o \approx r_e = 25 \ \Omega$$

$$f_l = \frac{\omega_l}{2\pi} = \frac{1}{2\pi R_B C_c} = \frac{1}{2\pi \times 9.9 \times 10^3 \times 0.47 \times 10^{-6}} = 36 \text{ Hz}$$

Example 2: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $h_{fe} = 200$, $h_{ie} = 5$ kΩ, $h_{oe} = 10$ μS).

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad \beta = h_{fe} = 200 \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$



DC analysis: Replace R_1 and R_2 with their Thevenin equivalent and proceed with DC analysis (all DC current and voltages are denoted by capital letters). Since all capacitors are replaced with open circuit, the emitter resistance for DC analysis is 270+240 = 510 Ω.

$$R_B = 5.9 \text{ k} \parallel 34 \text{ k} = 5.0 \text{ k}\Omega$$

$$V_{BB} = \frac{5.9}{5.9 + 34} 15 = 2.22 \text{ V}$$

KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

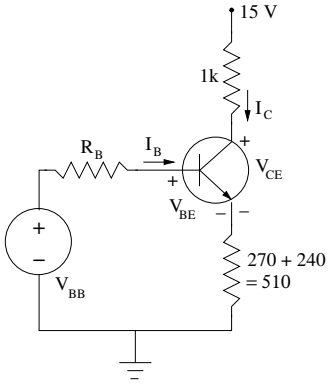
$$2.22 - 0.7 = I_E \left(\frac{5.0 \times 10^3}{201} + 510 \right)$$

$$I_E = 3 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 15 \ \mu\text{A}$$

KVL: $V_{CC} = 1000 I_C + V_{CE} + 510 I_E$

$$V_{CE} = 15 - 1,510 \times 3 \times 10^{-3} = 10.5 \text{ V}$$

DC Bias: $I_E \approx I_C = 3$ mA, $\quad I_B = 15$ μA, $\quad V_{CE} = 10.5$ V



AC analysis: The circuit is a common collector amplifier with an emitter resistance. Note that the 240 Ω resistor is shorted out with the by-pass capacitor. It only enters the formula for the lower cut-off frequency. Using the formulas in page 134 (with $R_{E1} = 270$ Ω):

$$A_v = \frac{R_C}{R_{E1}} = \frac{1,000}{270} = 3.70$$

$$R_i \approx R_B \parallel \beta R_{E1} \approx R_B = 5.0 \text{ k}\Omega \qquad R_o \approx r_e \left(\frac{R_{E1}}{r_e} + 1 \right) = 1.2 \text{ M } \Omega$$

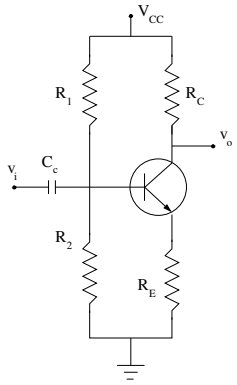
$$R'_E = R_{E2} \parallel (R_{E1} + r_e) = 240 \parallel (270 + 25) = 132 \ \Omega$$

$$f_l = \frac{\omega_l}{2\pi} = \frac{1}{2\pi R_i C_c} + \frac{1}{2\pi R'_E C_b} =$$

$$\frac{1}{2\pi \times 5,000 \times 4.7 \times 10^{-6}} + \frac{1}{2\pi \times 132 \times 47 \times 10^{-6}} = 31.5 \text{ Hz}$$

Example 3: Design a BJT amplifier with a gain of 4 and a lower cut-off frequency of 100 Hz. The Q point parameters should be $I_C = 3$ mA and $V_{CE} = 7.5$ V. (Manufacturers' spec sheets give: $\beta_{min} = 100$, $\beta = 200$, $h_{ie} = 5$ kΩ, $h_{oe} = 10$ μS).

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$

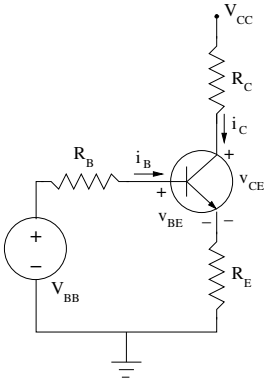


The prototype of this circuit is a common emitter amplifier with an emitter resistance. Using formulas of page 134

$$|A_v| \approx \frac{R_C}{R_E} = 4$$

The lower cut-off frequency will set the value of C_c.

We start with the DC bias: As V_{CC} is not given, we need to choose it. To set the Q-point in the middle of load line, set $V_{CC} = 2V_{CE} = 15$ V. Then, noting $I_C \approx I_E$,:



$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$
$$15 - 7.5 = 3 \times 10^{-3}(R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.5 \text{ k}\Omega$$

Values of R_C and R_E can be found from the above equation together with the AC gain of the amplifier, $A_V = 4$. Ignoring r_e compared to R_E (usually a good approximation), we get:

$$\frac{R_C}{R_E} = 4 \quad \rightarrow \quad 4R_E + R_E = 2.5 \text{ k}\Omega \quad \rightarrow \quad R_E = 500 \ \Omega, R_C = 2. \text{ k}\Omega$$

Commercial values are $R_E = 510$ Ω and $R_C = 2$ kΩ. Use these commercial values for the rest of analysis.

We need to check if $V_E > 1$ V, the condition for good biasing. $V_E = R_E I_E = 510 \times 3 \times 10^{-3} = 1.5 > 1$, it is OK (See next example for the case when V_E is smaller than 1 V).

We now proceed to find R_B and V_{BB}. R_B is found from good bias condition and V_{BB} from a KVL in BE loop:

$$R_B \ll (\beta + 1)R_E \quad \rightarrow \quad R_B = 0.1(\beta_{min} + 1)R_E = 0.1 \times 101 \times 510 = 5.1 \text{ k}\Omega$$
KVL: $\quad V_{BB} = R_B I_B + V_{BE} + R_E I_E$
$$V_{BB} = 5.1 \times 10^3 \frac{3 \times 10^{-3}}{201} + 0.7 + 510 \times 3 \times 10^{-3} = 2.28 \text{ V}$$

Bias resistors R_1 and R_2 are now found from R_B and V_{BB}:

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 5 \text{ k}\Omega$$
$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{2.28}{15} = 0.152$$

R_1 can be found by dividing the two equations: $R_1 = 33$ kΩ. R_2 is found from the equation for V_{BB} to be $R_2 = 5.9$ kΩ. Commercial values are $R_1 = 33$ kΩ and $R_2 = 6.2$ kΩ.

Lastly, we have to find the value of the coupling capacitor:

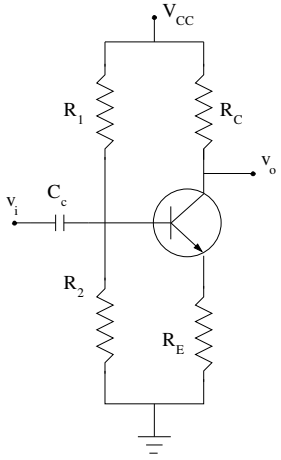
$$\omega_l = \frac{1}{R_i C_c} = 2\pi \times 100$$

Using $R_i \approx R_B = 5.1$ kΩ, we find $C_c = 3 \times 10^{-7}$ F or a commercial values of $C_c = 300$ nF.

So, are design values are: $R_1 = 33$ kΩ, $R_2 = 6.2$ kΩ, $R_E = 510$ Ω, $R_C = 2$ kΩ. and $C_c = 300$ nF.

Example 4: Design a BJT amplifier with a gain of 10 and a lower cut-off frequency of 100 Hz. The Q point parameters should be $I_C = 3$ mA and $V_{CE} = 7.5$ V. A power supply of 15 V is available. Manufacturers' spec sheets give: $\beta_{min} = 100$, $h_{fe} = 200$, $r_\pi = 5$ kΩ, $h_{oe} = 10$ μS.

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$



The prototype of this circuit is a common emitter amplifier with an emitter resistance. Using formulas of page 134:

$$|A_v| \approx \frac{R_C}{R_E} = 10$$

The lower cut-off frequency will set the value of C_c.

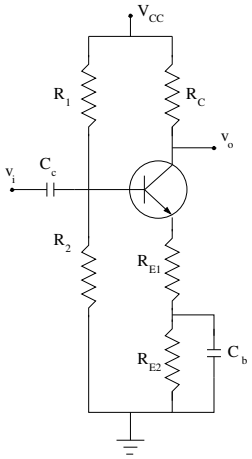
We start with the DC bias: As the power supply voltage is given, we set $V_{CC} = 15$ V. Then, noting $I_C \approx I_E$,:

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$
$$15 - 7.5 = 3 \times 10^{-3}(R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.5 \text{ k}\Omega$$

Values of R_C and R_E can be found from the above equation together with the AC gain of the amplifier $A_V = 10$. Ignoring r_e compared to R_E (usually a good approximation), we get:

$$\frac{R_C}{R_E} = 10 \quad \rightarrow \quad 10R_E + R_E = 2.5 \text{ k}\Omega \quad \rightarrow \quad R_E = 227\ \Omega, R_C = 2.27 \text{ k}\Omega$$

We need to check if $V_E > 1$ V which is the condition for good biasing: $V_E = R_E I_E = 227 \times 3 \times 10^{-3} = 0.69 < 1$. Therefore, we need to use a bypass capacitor and modify our circuits as is shown.

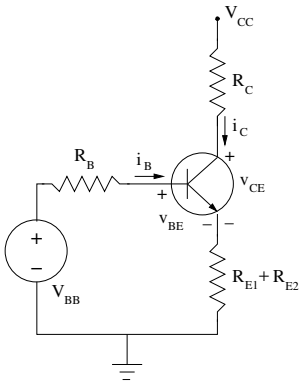


For DC analysis, the emitter resistance is $R_{E1} + R_{E2}$ while for AC analysis, the emitter resistance will be R_{E1}. Therefore:

$$\text{DC Bias:} \quad R_C + R_{E1} + R_{E2} = 2.5 \text{ k}\Omega$$

$$\text{AC gain:} \quad A_v = \frac{R_C}{R_{E1}} = 10$$

Above are two equations in three unknowns. A third equation is derived by setting $V_E = 1$ V to minimize the value of $R_{E1} + R_{E2}$.



$$V_E = (R_{E1} + R_{E2}) I_E$$

$$R_{E1} + R_{E2} = \frac{1}{3 \times 10^{-3}} = 333$$

Now, solving for R_C, R_{E1}, and R_{E2}, we find $R_C = 2.2$ kΩ, $R_{E1} = 220\ \Omega$, and $R_{E2} = 110\ \Omega$ (All commercial values).

We can now proceed to find R_B and V_{BB}:

$$R_B \ll (\beta + 1)(R_{E1} + R_{E2})$$

$$R_B = 0.1(\beta_{min} + 1)(R_{E1} + R_{E2}) = 0.1 \times 101 \times 330 = 3.3 \text{ k}\Omega$$

$$\text{KVL:} \quad V_{BB} = R_B I_B + V_{BE} + R_E I_E$$

$$V_{BB} = 3.3 \times 10^3 \frac{3 \times 10^{-3}}{201} + 0.7 + 330 \times 3 \times 10^{-3} = 1.7 \text{ V}$$

Bias resistors R_1 and R_2 are now found from R_B and $V_B B$:

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 3.3 \text{ k}\Omega$$

$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{1}{15} = 0.066$$

R_1 can be found by dividing the two equations: $R_1 = 50$ kΩ and R_2 is found from the equation for V_{BB} to be $R_2 = 3.6$k Ω. Commercial values are $R_1 = 51$ kΩ and $R_2 = 3.6$k Ω

Lastly, we have to find the value of the coupling and bypass capacitors:

$$R'_E = R_{E2} \parallel (R_{E1} + r_e) = 110 \parallel (220 + 25) = 76\ \Omega$$
$$R_i \approx R_B = 3.3\ \text{k}\Omega$$
$$\omega_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b} = 2\pi \times 100$$

This is one equation in two unknown (C_c and C_B) so one can be chosen freely. Typically $C_b \gg C_c$ as $R_i \approx R_B \gg R_E \gg R'_E$. This means that unless we choose C_c to be very small, the cut-off frequency is set by the bypass capacitor. The usual approach is the choose C_b based on the cut-off frequency of the amplifier and choose C_c such that cut-off frequency of the $R_i C_c$ filter is at least a factor of ten lower than that of the bypass capacitor. Note that in this case, our formula for the cut-off frequency is quite accurate (see discussion in page 129) and is

$$\omega_l \approx \frac{1}{R'_E C_b} = 2\pi \times 100$$

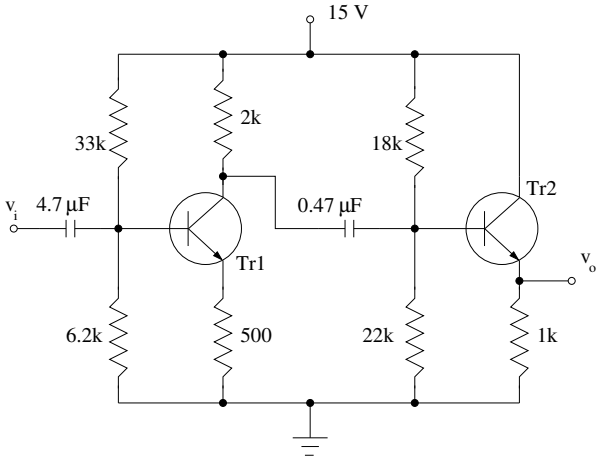
This gives $C_b = 20\ \mu$F. Then, setting

$$\frac{1}{R_i C_c} \ll \frac{1}{R'_E C_b}$$
$$\frac{1}{R_i C_c} = 0.1\,\frac{1}{R'_E C_b}$$
$$R_i C_c = 10 R'_E C_b \quad \rightarrow \quad C_c = 4.7 \times 10^{-6} = 4.7\ \mu\text{F}$$

So, are design values are: $R_1 = 50$ kΩ, $R_2 = 3.6$ kΩ, $R_{E1} = 220\ \Omega$, $R_{E2} = 110\ \Omega$, $R_C = 2.2$ kΩ, $C_b = 20\ \mu$F, and $C_c = 4.7\ \mu$F.

An alternative approach is to choose C_b (or C_c) and compute the value of the other from the formula for the cut-off frequency. For example, if we choose $C_b = 47\ \mu$F, we find $C_c = 0.86\ \mu$F.

Example 5: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $\beta = 200$, $r_\pi = 5$ kΩ, $r_o = 100$ kΩ).



This is a two-stage amplifier. The first stage (Tr1) is a common emitter amplifier and the second stage (Tr2) is an emitter follower. The two stages are coupled by a coupling capacitor (0.47 μF).

DC analysis:

When we replace the coupling capacitors with open circuits, we see the that bias circuits for the two transistors are independent of each other. Each bias circuit can be solved independently.

For Tr1, we replace the bias resistors (6.2k and 33k) with their Thevenin equivalent and proceed with DC analysis:

$$R_{B1} = 6.2 \text{ k} \parallel 33 \text{ k} = 5.22 \text{ k}\Omega \qquad \text{and} \qquad V_{BB1} = \frac{6.2}{6.2+33}\,15 = 2.37 \text{ V}$$

BE-KVL: $V_{BB1} = R_{B1}I_{B1} + V_{BE1} + 10^3 I_{E1} \qquad I_{B1} = \dfrac{I_{E1}}{1+\beta} = \dfrac{I_{E1}}{201}$

$$2.37 - 0.7 = I_{E1}\left(\frac{5.22\times 10^3}{201} + 500\right)$$

$$I_{E1} = 3.17 \text{ mA} \approx I_{C1}, \qquad I_{B1} = \frac{I_{C1}}{\beta} = 16\ \mu\text{A}$$

CE-KVL: $V_{CC} = 2\times 10^3 I_{C1} + V_{CE1} + 500 I_{E1}$

$$V_{CE1} = 15 - 2.5\times 10^3 \times 3.17 \times 10^{-3} = 7.1 \text{ V}$$

DC Bias summary for Tr1: $I_{E1} \approx I_{C1} = 3.17$ mA, $I_{B1} = 16\ \mu$A, $V_{CE1} = 7.1$ V

Following similar procedure for Tr2, we get:

$$R_{B2} = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega \qquad \text{and} \qquad V_{BB2} = \frac{22}{18+22}\,15 = 8.25 \text{ V}$$

BE-KVL: $V_{BB2} = R_{B2}I_{B2} + V_{BE2} + 10^3 I_{E2} \qquad I_{B2} = \dfrac{I_{E2}}{1+\beta} = \dfrac{I_{E2}}{201}$

$$8.25 - 0.7 = I_{E2}\left(\frac{9.9\times 10^3}{201} + 10^3\right)$$

$I_{E2} = 7.2$ mA $\approx I_{C2}$, $\quad I_{B2} = \dfrac{I_{C2}}{\beta} = 36\ \mu$A

CE-KVL: $\quad V_{CC} = V_{CE2} + 10^3 I_{E2}$

$\quad V_{CE2} = 15 - 10^3 \times 7.2 \times 10^{-3} = 7.8$ V

DC Bias summary for TR2: $\quad I_{E2} \approx I_{C2} = 7.2$ mA, $\quad I_{B2} = 36\ \mu$A, $\quad V_{CE2} = 7.8$ V

AC analysis:

We start with the emitter follower circuit (Tr2) as the input resistance of this circuit will appear as the load for the common emitter amplifier (Tr1). Using the formulas in page 134:

$$A_{v2} \approx 1$$

$$R_{i2} \approx R_{B2} = 9.9\ k\Omega$$

$$f_{l2} = \frac{\omega_{l2}}{2\pi} = \frac{1}{2\pi R_{B2} C_{c2}} = \frac{1}{2\pi \times 9.9 \times 10^3 \times 0.47 \times 10^{-6}} = 34 \text{ Hz}$$

Since $R_{i2} = 9.9$ kΩ is NOT much larger than the collector resistor of common emitter amplifier (Tr1), it will affect the first circuit. Following discussion in pages 125 and 128, the effect of this load can be taken into by replacing R_C in common emitter amplifiers formulas with $R'_C = R_C \parallel R_L = R_{C1} \parallel R_{i2} = 2$ k $\parallel 9.9$ k$\Omega = 1.66$ kΩ.

$$|A_{v1}| \approx \frac{R'_C}{R_E} = \frac{1.66\text{k}}{500} = 3.3$$

$$R_{i1} \approx R_{B1} = 5.22\ k\Omega$$

$$f_{l1} = \frac{\omega_{l1}}{2\pi} = \frac{1}{2\pi R_{B1} C_{c1}} = \frac{1}{2\pi \times 5.22 \times 10^3 \times 4.7 \times 10^{-6}} = 6.5 \text{ Hz}$$

The overall gain of the two-stage amplifier is then $A_v = A_{v1} \times A_{v2} = 3.3$. The input resistance of the two-stage amplifier is the input resistance of the first-stage (Tr1), $R_i = 9.9$ kΩ. To find the lower cut-off frequency of the two-stage amplifier, we note that:

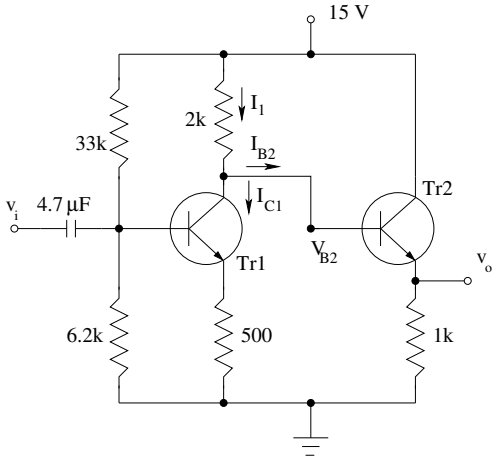
$$A_{v1}(j\omega) = \frac{A_{v1}}{1 - j\omega_{l1}/\omega} \qquad \text{and} \qquad A_{v2}(j\omega) = \frac{A_{v2}}{1 - j\omega_{l2}/\omega}$$

$$A_v(j\omega) = A_{v1}(j\omega) \times A_{v2}(j\omega) = \frac{A_{v1}A_{v2}}{(1 - j\omega_{l1}/\omega)(1 - j\omega_{l2}/\omega)}$$

From above, it is clear that the maximum value of $A_v(j\omega)$ is $A_{v1}A_{v2}$ and the cut-off frequency, ω_l can be found from $|A_v(j\omega = \omega_l)| = A_{v1}A_{v2}/\sqrt{2}$ (similar to procedure we used for filters). For the circuit above, since $\omega_{l2} \gg \omega_{l1}$ the lower cut-off frequency would be very close to ω_{l2}. So, the lower-cut-off frequency of this amplifier is 34 Hz.

Example 6: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $\beta = 200$, $r_\pi = 5$ kΩ, $r_o = 100$ kΩ).

This is a two-stage amplifier. The first stage (Tr1) is a common emitter amplifier and the second stage (Tr2) is an emitter follower. The circuit is similar to the two-stage amplifier of Example 5. The only difference is that Tr2 is directly biased from Tr1 and there is no coupling capacitor between the two stages. This approach has its own advantages and disadvantages that are discussed at the end of this example.



DC analysis:

Since the base current in BJTs are typically much smaller that the collector current, we start by assuming $I_{C1} \gg I_{B2}$. In this case, $I_1 = I_{C1} + I_{B2} \approx I_{C1} \approx I_{E1}$ (the bias current I_{B2} has no effect on bias parameters of Tr1). This assumption simplifies the analysis considerably and we will check the validity of this assumption later.

For Tr1, we replace the bias resistors (6.2k and 33k) with their Thevenin equivalent and proceed with DC analysis:

$$R_{B1} = 6.2 \text{ k} \parallel 33 \text{ k} = 5.22 \text{ k}\Omega \qquad \text{and} \qquad V_{BB1} = \frac{6.2}{6.2+33}\,15 = 2.37 \text{ V}$$

$$\text{BE-KVL:} \quad V_{BB1} = R_{B1}I_{B1} + V_{BE1} + 10^3 I_{E1} \qquad I_{B1} = \frac{I_{E1}}{1+\beta} = \frac{I_{E1}}{201}$$

$$2.37 - 0.7 = I_{E1}\left(\frac{5.22\times 10^3}{201} + 500\right)$$

$$I_{E1} = 3.17 \text{ mA} \approx I_{C1}, \qquad I_{B1} = \frac{I_{C1}}{\beta} = 16\ \mu\text{A}$$

$$\text{CE-KVL:} \quad V_{CC} = 2\times 10^3 I_{C1} + V_{CE1} + 500 I_{E1}$$

$$V_{CE1} = 15 - 2.5\times 10^3 \times 3.17\times 10^{-3} = 7.1 \text{ V}$$

DC Bias summary for Tr1: $I_{E1} \approx I_{C1} = 3.17$ mA, $I_{B1} = 16\ \mu$A, $V_{CE1} = 7.1$ V

To find the bias point of TR2, we note:

$$V_{B2} = V_{CE1} + 500 \times I_{E1} = 7.1 + 500 \times 3.17 \times 10^{-3} = 8.68 \text{ V}$$

BE-KVL: $V_{B2} = V_{BE2} + 10^3 I_{E2}$

$8.68 - 0.7 = 10^3 I_{E2}$

$I_{E2} = 8.0 \text{ mA} \approx I_{C2}, \qquad I_{B2} = \frac{I_{C2}}{\beta} = 40 \ \mu\text{A}$

KVL: $V_{CC} = V_{CE2} + 10^3 I_{E2}$

$V_{CE2} = 15 - 10^3 \times 8.0 \times 10^{-3} = 7.0 \text{ V}$

DC Bias summary for TR2: $I_{E2} \approx I_{C2} = 8.0$ mA, $I_{B2} = 40 \ \mu$A, $V_{CE2} = 7.0$ V

We now check our assumption of $I_{C1} \gg I_{B2}$. We find $I_{C1} = 3.17$ mA$\gg I_{B2} = 41 \ \mu$A. So, our assumption was justified.

It should be noted that this bias arrangement is also stable to variation in transistor β. The bias resistors in the first stage will ensure that I_{C1} ($\approx I_{E1}$) and V_{CE1} is stable to variation of TR1 β. Since $V_{B2} = V_{CE1} + R_{E1} \times I_{E1}$, V_{B2} will also be stable to variation in transistor β. Finally, $V_{B2} = V_{BE2} + R_{E2} I_{E2}$. Thus, I_{C2} ($\approx I_{E2}$) will also be stable (and V_{CE2} because of CE-KVL).

AC analysis:

As in Example 5, we start with the emitter follower circuit (Tr2) as the input resistance of this circuit will appear as the load for the common emitter amplifier (Tr1). Using the formulas in page 134 and noting that this amplifier does not have bias resistors ($R_{B1} \to \infty$):

$A_{v2} \approx 1$

$R_{i2} = r_\pi + (R_E \parallel r_o)(1 + \beta) = 5 \times 10^3 + 201 \times 10^3 = 201 \text{ k}\Omega$

Note that because of the absence of the bias resistors, the input resistance of the circuit is very large, and because of the absence of the coupling capacitors, there is no lower cut-off frequency for this stage.

Since $R_{i2} = 201$ kΩ is much larger than the collector resistor of common emitter amplifier (Tr1), it will NOT affect the first circuit. The parameters of the first-stage common emitter amplifier can be found using formulas of page 134.

$|A_{v1}| \approx \frac{R_C}{R_E} = \frac{2,000}{500} = 4$

$R_{i1} \approx R_{B1} = 5.22 \ k\Omega$

$f_{l1} = \frac{\omega_{l1}}{2\pi} = \frac{1}{2\pi R_{B1} C_{c1}} = \frac{1}{2\pi \times 5.22 \times 10^3 \times 4.7 \times 10^{-6}} = 6.5 \text{ Hz}$

The overall gain of the two-stage amplifier is then $A_v = A_{v1} \times A_{v2} = 4$. The input resistance of the two-stage amplifier is the input resistance of the first-stage (Tr1), $R_i = 9.9$ kΩ. The find the lower cut-off frequency of the two-stage amplifier is 6.5 Hz.

The two-stage amplifier of Example 6 has many advantages over that of Example 5. It has three less elements. Because of the absence of bias resistors, the second-stage does not load the first stage and the overall gain is higher. Also because of the absence of a coupling capacitor between the two-stages, the overall cut-off frequency of the circuit is lower. Some of these issues can be resolved by design, *e.g.,* use a large capacitor for coupling the two stages, use a large R_{E2}, *etc.*. The drawback of the Example 6 circuit is that the bias circuit is more complicated and harder to design.