Outline

- Introduction
- Grading Policy
- Objective
- Altera DE2 Board
- ARM7-TDMI
- NXP LPC2378 Board
- Laboratory in a Glance
Microprocessor Systems' Lab (25-723)

Dr. M. Hashemi

Lab Hours: Sundays 16:30 –19:30

Course Webpage:

http://microlab.ee.sharif.ir

Including:

4 Labs conducted on Altera DE2 Boards
Note that we have no policy for pre-reports late submission, so lately submitted pre-reports won’t take into account.

<table>
<thead>
<tr>
<th></th>
<th>Introduction</th>
<th>Lab1</th>
<th>Lab2</th>
<th>Lab3</th>
<th>Lab4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5%</td>
<td>5%</td>
<td>10%</td>
<td>15%</td>
<td>65%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Pre-report</th>
<th>Lab Progress</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>30%</td>
<td>70%</td>
</tr>
</tbody>
</table>
Objectives

- Getting to know NIOS II and ARM processor families and gathering some practical experience on both hardware and software of these processors.
- Learning about JTAG interface for Debugging and programming.
- Learning about Soft-Processors and the principles of Reconfigurable Computing.
- Familiarizing the students with different memories and different applications for them.
Altera DE2 Board

- Cyclone II FPGA Chip with 35000 LEs
- USB Blaster & JTAG
- 50-MHz and 27-MHz Clock Sources
- Many peripherals like:
  - Line In/Out, Microphone In (24-bit Audio CODEC)
  - 128 MB SDRAM, 2 MB SRAM, 8 MB Flash
  - PS/2 mouse or keyboard port
  - Video Out (VGA 8-bit DAC)
  - 16 x 2 LCD display
NIOS II

- The Most Popular Soft-Core
- The world's most versatile processor
- Available for Standard-Cell ASICs through Synopsys.
- Support of hundreds of peripheral IP Cores.
- Perfect for Prototyping
- Available in 3 flavors:
  - Fast
  - Economy
  - Standard
Softwares

NIOS 2

Quartus 9.0 or Higher

SoPC Builder

NIOS2 Software

Altera Monitor Program
1. **NIOS II Intro.**
   - Learning about NIOS assembly
   - Implementation of a costume hardware
   - Debugging process

2. **Character LCD**
   - Coding in C for NIOS
   - Using interrupts
   - Usage of predefined IP cores

3. **VGA Demonstration**
   - Implementation of some graphical algorithm

4. **Speech Recognition**
   - Starting with calculating correlation
   - Coding in C for ARM/NIOS II
Warning

- The debugging process in this lab is highly time-consuming and the only possible way in which you will see the results, is if you have studied the related documentations before the lab.