Mohammad Sharifkhani, Ph.D.,

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Education

Ph.D., Electrical and Computer Engineering   2002-2006
University of Waterloo, Waterloo, Ontario, Canada

Thesis: "Design and Analysis of Low-power SRAMs"
Under the supervision of Prof. Manoj Sachdev

M.Sc., Electrical and Computer Engineering   1998-2000
University of Tehran, Tehran, Iran

Thesis: "A Monolithic CMOS Line-driver for ADSL Modem Applications"
- A high-speed line driver is implemented in 0.6um CMOS technology which is driven by a single 5V power supply voltage.

B.Sc., Electrical and Computer Engineering   1994-1998
University of Tehran, Tehran, Iran

Project: "Implementation of a data acquisition board"
- Design, Fabricate and Test of an RS-422 based data acquisition system.

Research Area

Embedded SRAM Circuits and Architecture for VLSI Circuits, Digital and Mixed Signal VLSI, Analog Built-in Self Test Circuits, Wireless Communication Circuits and Systems.

Administrative Management

Chair   2010-Now
Communication and Public Affairs Office
Sharif University of Technology, Tehran, Iran

Professional and Research Experience

Assistant Professor   2008-Now
Sharif University of Technology, Tehran, Iran
- Instructor of several graduate and undergrad courses in the broad area of analog and digital integrated circuit design.
- Head of the Semiconductor Digital and Memory Circuit Design Research Group
- One of the three founders of the Advanced IC Design Lab at Sharif Univ. of Tech.
- Supervised or co-supervised 15 grad students

VoD Set-top-box Program Director   2011-Now
Sharif University of Technology, Tehran, Iran
- 600 K$ project funded by Setad-micro.

DVB-T Receiver Program Director   2009-2011
Sharif University of Technology, Tehran, Iran
- 1.4 M$ project funded by IRIB.
- More than 25 engineers/grad students involved.
- Including tree technical divisions of Silicon Tuner design team, DVB-T Demod. design team, and Set-top-box design team.
- The tuner was awarded in the National Khwarizmi scientific contest.

Senior Research Associate   2007-2008
Micro Electronics Research and Development
Center of Iran (MERDCI)
- Member of SmartCard v2.5 IC design group
- Design of a compact DES/TDES coprocessor
- Design of a compact multi-standard ECC/RSA/AES Cryptoprocessor

Post-Doctoral Research Fellow   2006-2007
University of Waterloo, Waterloo, Canada
- Member of CMOS Design and Reliability Group
- Compact High-reliability SRAM design
- Analog built-in self test structures for high frequency analog circuits.

Research Assistant   2004-2006
University of Waterloo, Waterloo, Canada
- Member of CMOS Design and Reliability Group
- Low-power SRAM design and Integrated analog testing

Research Assistant   2002-2004
University of Waterloo, Waterloo, Canada
- Working on phase/frequency digitizers
- A team work on the test setup and troubleshooting of the Dual PLL project is delivered this led to the following papers:

  M. Izadi, B. Leung, "PLL-based frequency discriminator using the loop filter as an estimator", IEEE Transactions on Circuit and Systems (TCAS-II), Nov 2002.

  Z. Shu, K. Lee, B. Leung, "A 2.4GHz Ring Oscillator Based CMOS Frequency Synthesizer with a Fractional Divider Dual PLL Architecture", IEEE Journal of Solid State Circuits.

- The time-domain phase noise simulation of the ring oscillator is developed

IC Design Eng. of a Low Voltage / Low Power A/D   2002
Valence Semiconductor, Dubai, UAE
- A delta-sigma modulator based A/D plus its decimation filters is developed in a CMOS 0.18um technology.
- The power consumption of 200 micro watts is achieved at 100 Sample/Sec.

IC Design Eng. of a Low Voltage Highly Integrated CODEC+SLIC for VoIP applications   2001-2002
Valence Semiconductor, Dubai, UAE
- System level design of call processing required blocks based on analog processing methods
- Analog circuit design of the blocks on TSMC 3.3V CMOS 0.35um technology

IC Design Eng. of a Quad Voice CODEC DSP for VoDSL applications   2000-2001
Valence Semiconductor, Dubai, UAE
- Standard compliant system level design of audio path signal processing units
- Hardware implementation of a low-power DSP for the required signal processing operation in a Mixed-Signal environment
- Mapping the design on TSMC CMOS 0.35um technology for an integrated solution

Research Assistant   1998-2000
IC-Design Center, University of Tehran, Tehran, Iran
- Member of ADSL system & circuit research team at the

University of Tehran.

- Development of an ADSL simulator

Skills

- Analog and mixed signal integrated circuit design
- System level design of oversampling data converters
- Digital VLSI design (Verilog)
- Experienced in using Cadence (IC, SoC Encounter), Mentor (ModelSim, Calibre), Synopsys (Design Compiler), Matlab
- Computer programming C++

Awards

- 3rd ranked Laureate in the National Khwarizmi contest.
- IEEE CICC/AMD Student Paper Award, IEEE Solid-State Circuit Sciety, 2007
- International Doctoral Scholarship University of Waterloo, 2004-2006
- International Student Scholarship, University of Waterloo, 2002-2003
- Rank 110 out of 300'000 in National University Entrance Exam 1994
- Rank 33 out of 10'000 in National University Graduate Program Entrance Exam 1998
- Rank 5 out of 10'000 in National Scholarship Program in 2001
- Rank 2 out of 150 in Univ. of Tehran PhD Entrance Exam 2000

Activities

Univ. of Tehran IEEE Student Branch Executive Committee   1998

IEEE Member   1998-present

Teaching Experience

Lecturer

- Several Graduate and Under Graduate level courses have been taught by the referee at Electrical Engineering Dept. at Sharif University of Technology since 2007. Namely, the following courses have been taught by him:

  - Circuit Theory (UG)
  - VLIS Systems (G)

- Advanced Digital Integrated Circuits (G)
- Analog Circuits (UG)
- Research methodology and presentation (Seminar) (G)

Adjunct Lecturer

- Electronics II, Ferdowsi University of Mashad, Fall'07.

Teaching Assistantships

- Circuit analysis and design (ECE 241), University of Waterloo, Fall'05.

- Microelectronic circuits (ECE 332), University of Waterloo, Summer'05.

- Analog integrated circuits (ECE 439), University of Waterloo, Winter'04.

- Circuit analysis and design (ECE 241), University of Waterloo, Fall'03.

- Microelectronic circuits (ECE 332), University of Waterloo, Summer'03.

- Analog integrated circuits (ECE 439), University of Waterloo, Winter'03.

- Electronic II Lab, University of Tehran, Tehran, Iran.

- Digital Electronics, University of Tehran, Tehran, Iran.

Journal Publications

Mohammad Chahardori, Mojtaba Atarodi, Mohammad Sharifkhani, "A Sub 1 Volt High PSRR CMOS Bandgap voltage reference", Accepted with modifications, Integration on VLSI, Elsevier, 2011.

M. Sharifkhani, E. Rahiminejad, S. Jahinuzzaman, M. Sachdev, "A Compact Hybrid Current/Voltage Sense Amplifier With Offset Cancellation for High-speed SRAMs", IEEE Transactions on VLSI (IEEE T-VLSI) Systems, Vol 19, No. 5, pp.883-894, May 2011.

S. M. Jahinuzzaman, M. Sachdev, and M. Sharifkhani, "An analytical model for soft error critical charge of nanometric SRAMs," IEEE Transactions on VLSI (IEEE T-VLSI) Systems, Vol 15, pp.196-205, March 2009.

M. Sharifkhani, M. Sachdev, "SRAM Cell Data Stability: A Dynamic Perspective", IEEE Journal of Solid State Circuits (IEEE JSSC), Vol. 44, No. 2, pp. 609-619, Feb. 2009

M. Sharifkhani, M. Sachdev, "An Energy Efficient 40Kb SRAM Module With Extended Read/Write Noise Margin in 0.13um CMOS", IEEE Journal of Solid State Circuits (IEEE JSSC), Vol. 44, No. 2, pp. 620-630, Feb. 2009

M. Sharifkhani, M. Sachdev, "Segmented Virtual Ground Architecture for Low-power Embedded SRAM", IEEE Transactions on VLSI (IEEE T-VLSI) Systems, Vol 15, pp.196-205, Feb. 2007.

Conference Publications

R. Saeidi, M. Sharifkhani, K. Hajsadeghi, "A Subthreshold Dynamic Read SRAM (DRSRAM) Based on Dynamic Stability Criteria," Proceedings of 2011 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 61-65, 2011.

M. Gholami, M. Sharifkhani, " Novel Parallel Architecture for Low Voltage-Low Power DLL-Based Frequency Multiplier ," Proceeding of IEEE DTIS, 2011.

M. Gholami, M. Sharifkhani, " Low Voltage and Low Power DLL-Based Frequency Synthesizer for Covering VHF Frequency Band ," Proceeding of IEEE DTIS, 2011.

M. Gholami, M. Sharifkhani, M. Hashemi, "Covering VHF frequency band with novel DLL-based frequency synthesizer," Proceeding of IEEE International Conference on Communications and Signal Processing (ICCSP), pp.297-299, 2011.

M. Gholami, M. Sharifkhani, S. Saeedi, "Modeling of DLL-based frequency multiplier in time and frequency domain with Matlab Simulink," Proceedings on IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pp. 1051-1054, 2010.

M. Gholami, M. Sharifkhani, A. Ebrahimi, S. Saeedi, M. Atarodi, M., "Systematic modeling and simulation of DLL-based frequency multiplier," Proceedings of IEEE Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), pp. 1-5, 2010.

Bahadori, M.; Mali, M.R.; Sarbishei, O.; Atarodi, M.; Sharifkhani, M.;, "A novel approach for secure and fast generation of RSA public and private keys on SmartCard," Proceedings of IEEE International NEWCAS Conference (NEWCAS), pp. 265 – 268, 2010.

M. Gholami, M. Sharifkhani, S. Saeedi, M. Atarodi, "A DLL-based frequency synthesizer for VHF DVB-H/T receivers," Proceedings of IEEE Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), pp. 1-5, 2010.

F. Haghighizadeh, H. Attarzadeh, M. Sharifkhani, "A Compact 8-Bit AES Crypto-processor," Proceedings of International Conference on Computer and Network Technology (ICCNT), pp. 71-75, 2010.

Attarzadeh, H.; SharifKhani, M.; Jahinuzzaman, S.M.;, "A scalable offset-cancelled current/voltage sense amplifier", Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 3853-3856, 2010.

S.M. Jahinuzzaman, M. Sharifkhani, M. Sachdev, "Investigation of Process Impact on Soft Error Susceptibility of Nanometric SRAMs Using a Compact Critical Charge Model," Proceeding of the International Symposium on Quality Electronic Design(IEEE ISQED), pp. 201-212, 2008.

M. Sharifkhani, S. M. Jahinuzzaman, M. Sachdev, "Dynamic Data Stability in Low-power SRAM Design", Proceedings of IEEE Custom Integrated Circuit Conference, September 2007. Awarded IEEE CICC/AMD Student Paper.

M. Sharifkhani, M. Sachdev, "A Phase-Domain Continuous-Time 2nd-Order ΔΣ-Frequency Digitizer", Proceedings of IEEE Custom Integrated Circuit Conference (IEEE CICC'06), pp. 205-208, September 2006.

M. Sharifkhani, M. Sachdev, "A Low Power SRAM Architecture Based on Segmented Virtual Grounding", IEEE Symposium on International Symposium on Low Power Electronics and Design (IEEE ISLPED'06), pp.256-261, October 2006.

M. Sharifkhani, S. M. Jahinnuzaman, M. Sachdev, "Dynamic Data Stability in SRAM Cells and its Implications on Data Stability Tests", Proceedings of IEEE International Workshop on Memory Technology, Design, and Testing (IEEE MTDT'06), pp. 55-61, 2006.

M. Sharifkhani, M. Sachdev, "A Phase-Domain Continuous-Time 2nd-Order ΔΣ- Modulator for Frequency Digitization", Presented at IEEE Symposium on Circuits and Systems (IEEE ISCAS'06), pp. 3434-3438, May 2006.

A. Amirabadi, M.M Tabrizi, M. Sharifkhani, O. Shoaei, "A 10 b, 40 Msample/s, 25 mW Pipeline Analog to Digital Converter", Proceedings of IEEE Canadian Conference on Electrical and Computer Engineering (IEEE CCECE), pp. 1989-1993, May, 2004.

M.M Tabrizi, A. Amirabadi, M. Sharifkhani, O. Shoaei, "A CMOS Elliptic Low-Pass Switched Capacitor Ladder Filter for Video Communication Using Bilinear Implementation", Proceedings of IEEE Canadian Conference on Electrical and Computer Engineering (IEEE CCECE), pp. 1723-1727, May, 2004.

A.H. Ismail, M. Sharikhani, M.I. Elmasry, "On the Design of Low Power MCML Based Ring Oscillators", Proceedings of IEEE Canadian Conference on Electrical and Computer Engineering May (IEEE CCECE), pp. 2383 - 2386 ,May, 2004.

M. Sharifkhani, "A Frequency Digitizer Based on Phase Domain Continuous Time Noise Shaping", Proceedings of IEEE International Symposium on Circuit and System, pp.1060-3, May, 2004.

M. Sharifkhani, I. Golampoor, O. Shoaei, "A Compact DSP for Audio Codecs Applications with Multi-rate Programmable Filtering Enhancement", Proceedings of IEEE International Conference on Communications Circuits and Systems, pp. 1515 - 1520, July 2002.

"Kalman-Filtering timing recovery scheme for OFDM systems", Proceedings of IEEE International Conference on Acoustic Speech and Signal Processing (IEEE ICASSP), pp. 2681 - 2684, June, 2000.

"System level design of an ANSI T1.413 based ADSL Modem", Proceedings of IEEE Iranian Conference on Electrical and Electronics (ICEE) '00, May, 2000. (In farsi)

Patents

"An asymmetric four transistor SRAM cell", US Patent (US), pending approval.

"Low-power SRAM Design based on Segmented Virtual Grounding Scheme"
US Patent (US60/729,936).