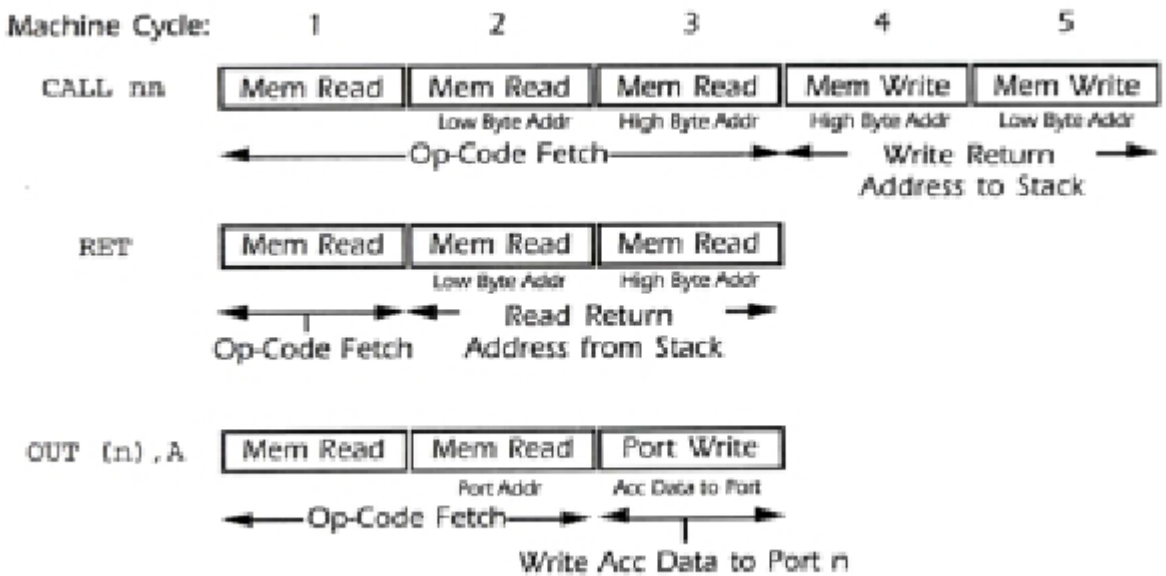
Memory Interfacing

Instruction Cycles and Machine Cycles

- Instruction cycle is the time taken to complete the execution of an instruction ⇒ 1-6 machine operation cycles
- Machine cycle is defined as the time required to complete one operation of accessing memory, accessing IO, etc.



T-States

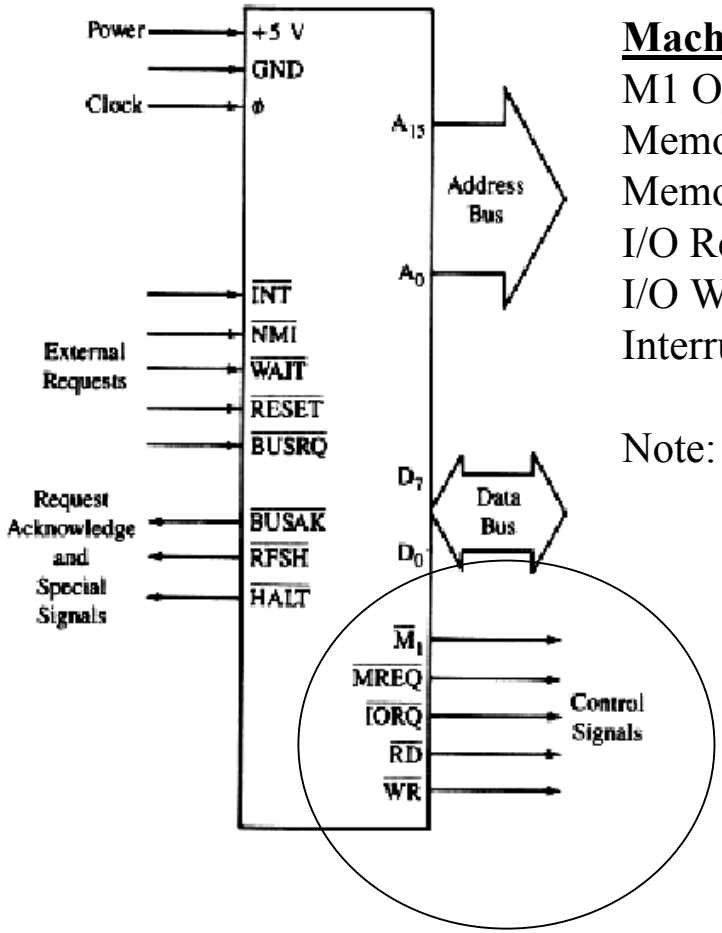
- Machines cycles are divided up into system clock cycles called T-states (1T = 1C cycle)
- T-state = 1T = $1/f_{Z80}$ = 1.75 us for 4MHz
- Example: LD A, 09H

  - It is a 2-byte instruction with 2 machine cycles.

  (2 operations = M1 Opcode Fetch + Memory read(Operand))

  - The execution time = 4T + 3T = 7T.

The Z80 Machine Cycles and Control Signals



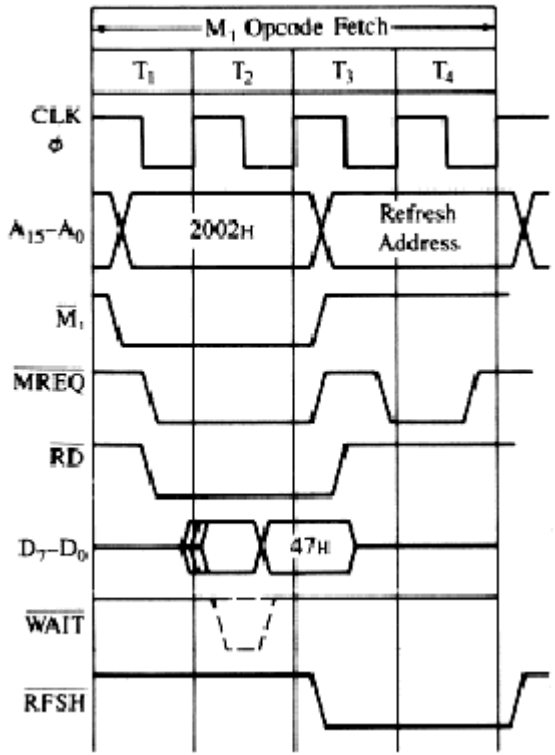
Machine Cycle	M1	MREQ	IORQ	RD	WR
M1 Opcode Fetch	0	0	1	0	1
Memory Read	1	0	1	0	1
Memory Write	1	0	1	1	0
I/O Read	1	1	0	0	1
I/O Write	1	1	0	1	0
Interrupt Ack	0	1	0	0	0

Note: Logic 0 = Active, Logic 1 = Inactive

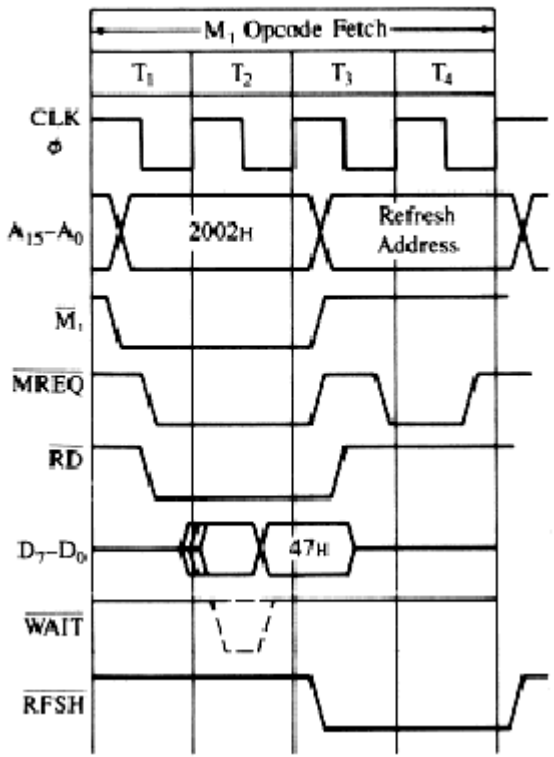
M1 Opcode Fetch Cycle

- Used to differentiate with Memory Read(Operand) and used for Int Ack cycle
- Sequence of events(Initial condition PC=2002H)

  - M1 goes low at the beginning of T1.
  - Z80 places PC on address bus and increments PC by 1
  - After T1 falling edge, MREQ and RD are asserted.
  - External memory circuits decodes the address and 2002H is identified.
  - Data bus which was high impedance state is activated after leading edge of T2.
  - Memory places 47H on the data bus after falling edge of T2.
  - Data is read at the leading edge of T3 and signals become inactive
  - Between T3 and T4 the instruction decoder in the μP decodes and executes the opcode.



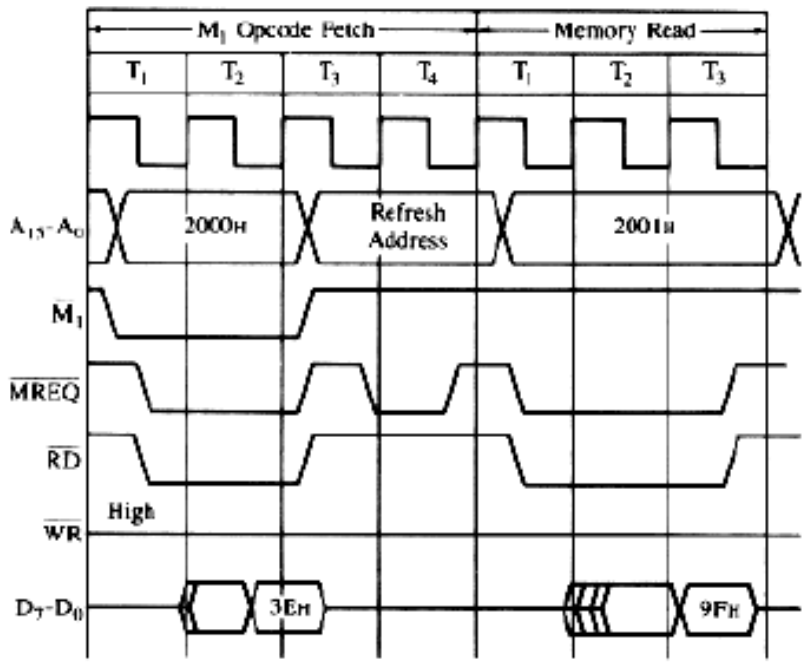
M1 Refresh Cycle and Wait Signal



- Dynamic memory consists of MOS transistors, which store information as capacitive charges; each cell needs to be periodically refreshed.
- Wait signal : the Z80 samples the wait signal during T2 if low then Z80 adds wait states to extend the machine cycle - used to interface memories with slow response time.

Memory Read Cycle

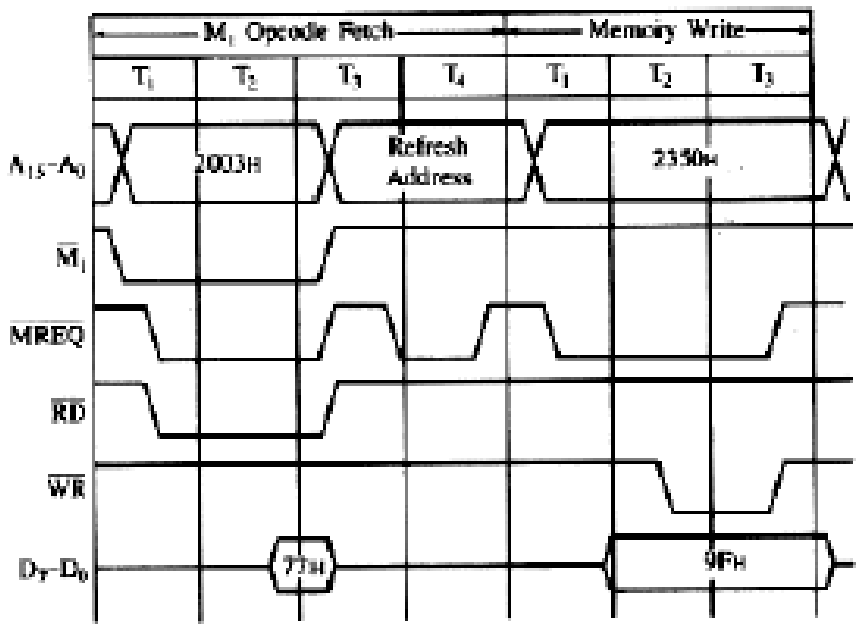
Address	Opcode	Instruction
2000	3E	LD A, 9FH
2001	9F	



Memory Write Cycle

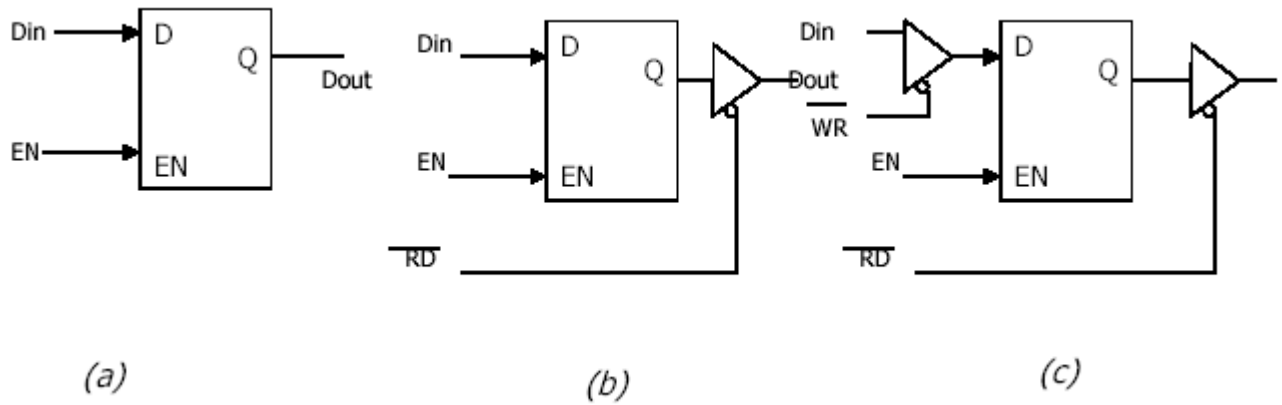
Address	Opcode	Instruction
2003	77	LD (HL),A

(Assume HL = 2350H , A = 9FH)



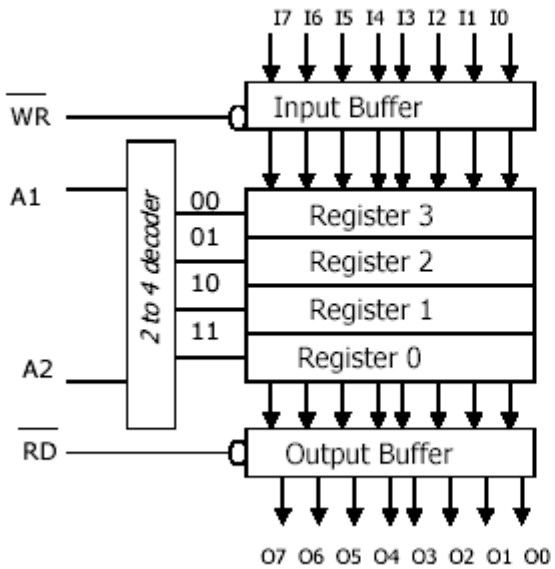
Memories

- Memory cell : A latch that can store one binary bit
- Registers are made up of multiple memory cells.
- A simple latch with an input and enable bit(Figure a) : Stored bit is always available at output.
- Using tri-state buffer to the output of the the latch (Figure b) : Stored bit can be read only when buffer is enabled.
- Using a tri-state buffer on the input too (Figure c) : Write into it by enabling the input buffer and read from it by enabling the output buffer.

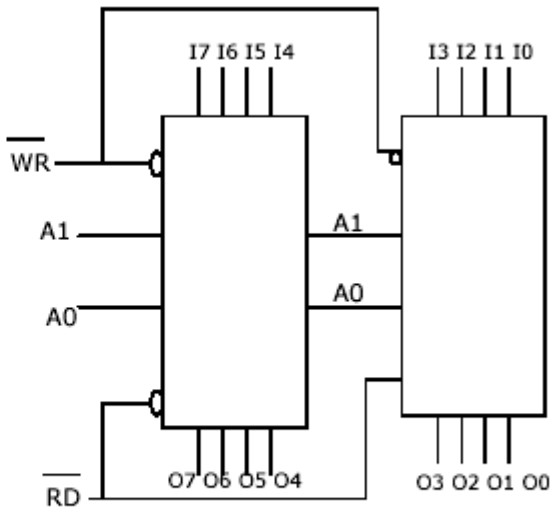


Memories Continued

- Figure (a) shows a 4×8 bit memory(register).
- To write into or read from any one of the registers, a specific register should be identified. This is a simple decoding function; 2-to-4 decoder can perform that function.
- In this case two more input lines A1 and A0 called address lines are required by the decoder.
- Each combination (00, 01, 10, 11) can identify or enable one of the registers (R0-R3).
- If we have only 4 bit memory chips, we can combine two chips in parallel to make an 8-bit memory word as shown in Figure (b).

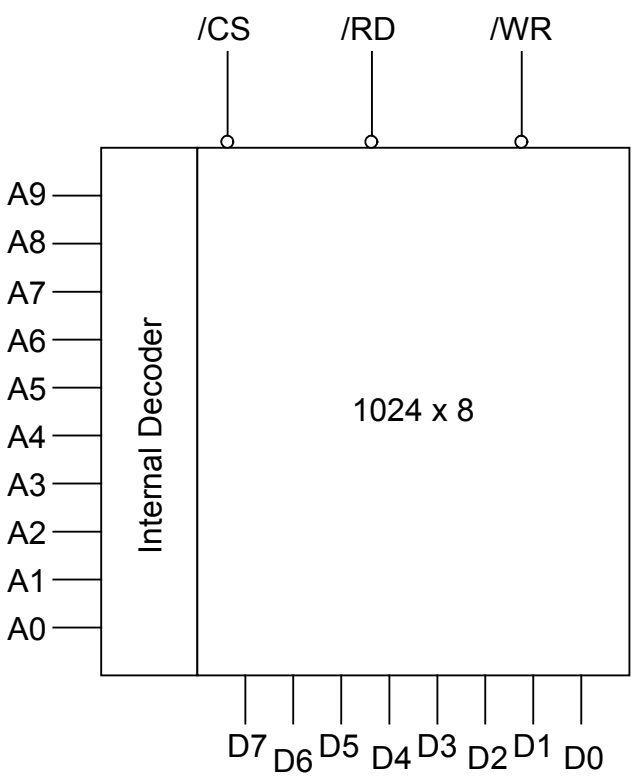


(a)



(b)

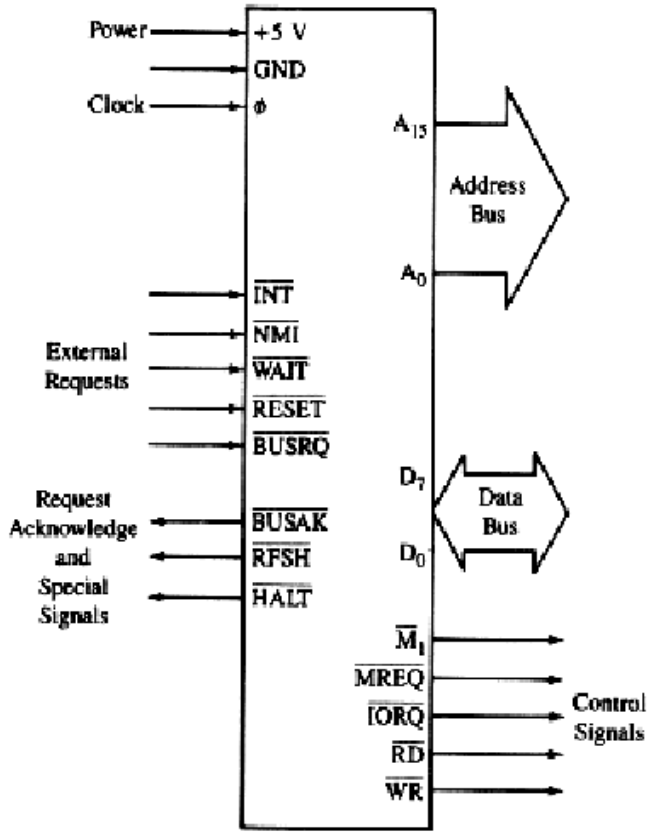
Memory Chips



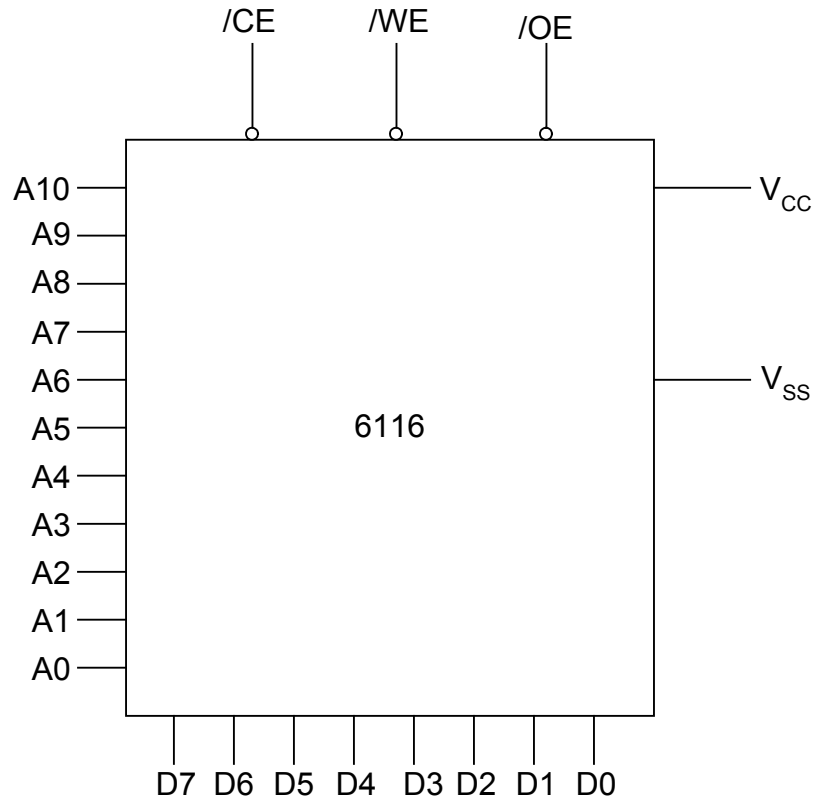
A typical 1K memory chip

- A0-A9 = Address lines to identify memory register, /CS (Chip Select) = signal to enable chip, /RD and /WR control signals to read from and write into memory.
- Number of address line is related to number of registers (2^n = number of registers, n is the number of address lines).
- /RD enables the output buffer. Data from the selected register are made available on the output lines.
- /WR enables the input buffer. Data on the input lines are written into memory cells.

Interfacing the Z80 with 6116 Memory Chip(2K x 8)

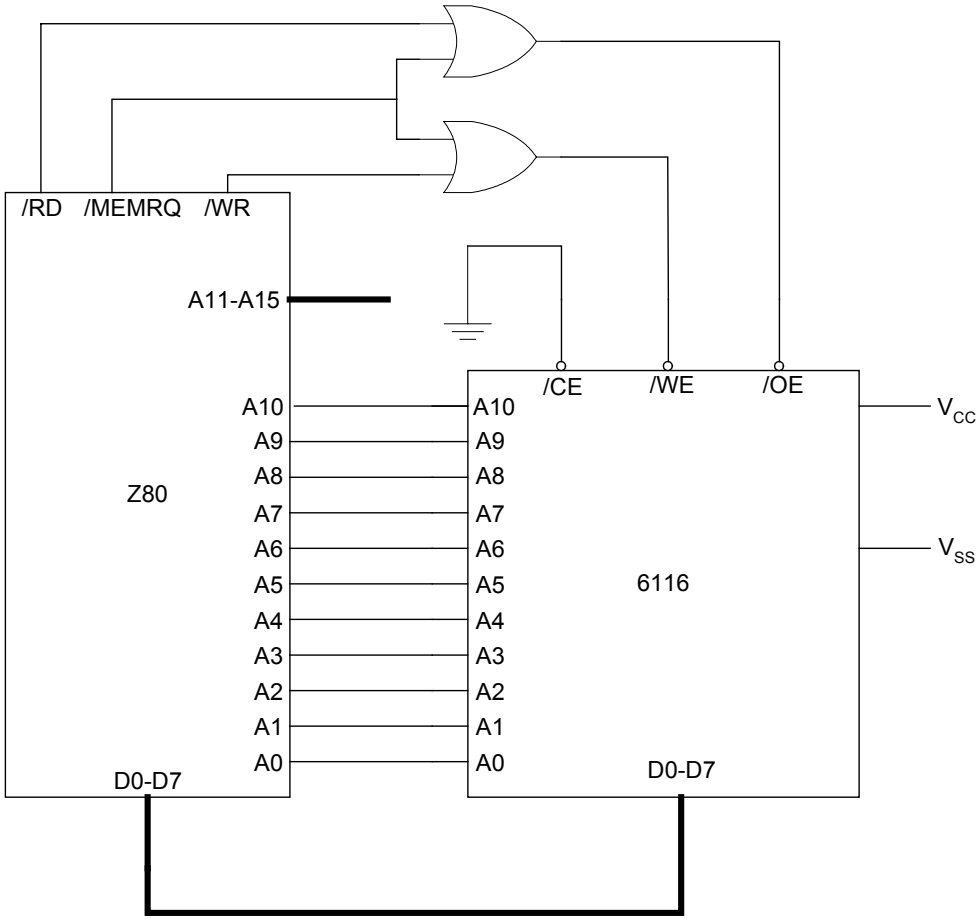


Z80



/CE = Chip Enable
/WE = Write Enable
/OE = Output Enable
VCC = Power(+5 Volts)
VSS = Ground

6116 Interfacing Circuit



A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
X	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1

Address 0000H-07FFH =

Address 0800H-0FFFH =

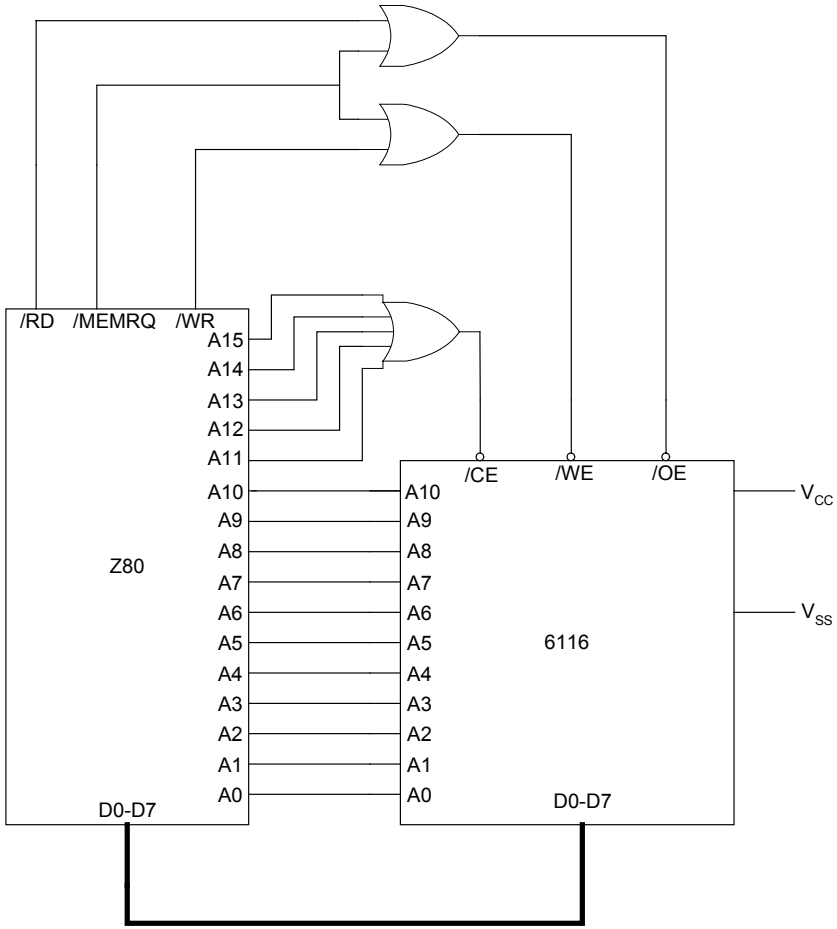
Address 1000H-17FFH =

Address 1800H-1FFFH = … =

Address 0F800H-0FFFFH

- Address 0000H is the same address on the 6116 chip as address 0800H,1000H,1800H,…,0F800H.

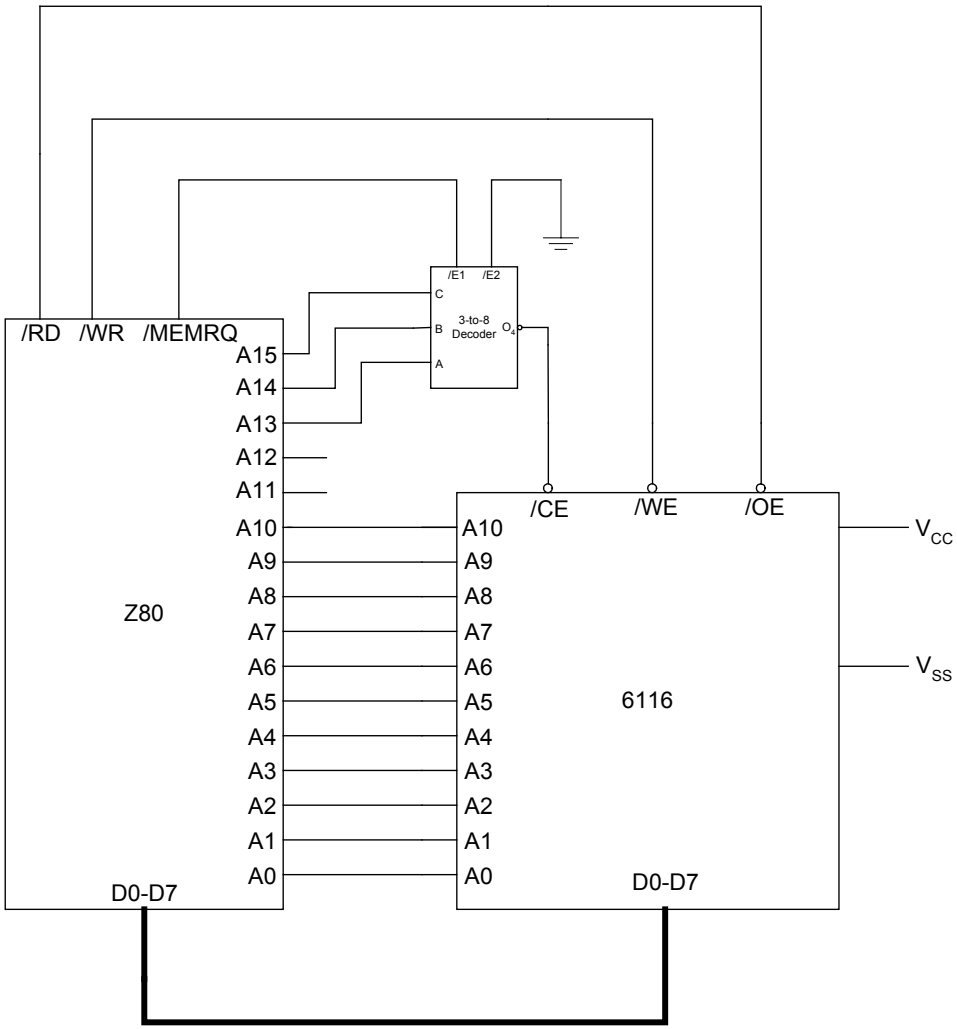
6116 Interfacing Circuit Continued



A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

- The memory range of the 6116 chip is 0000H-07FFH.

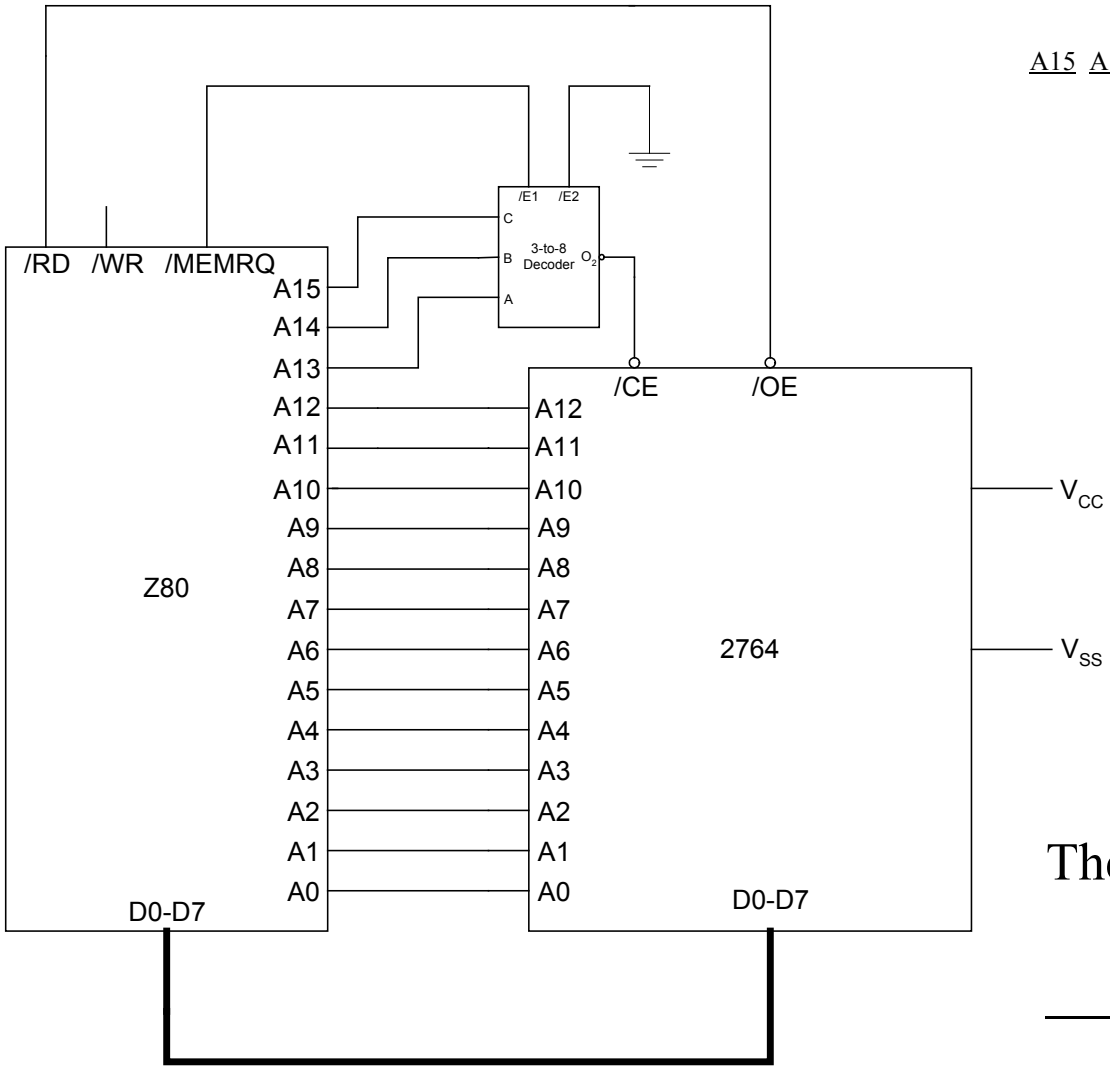
6116 Interfacing Circuit Continued



A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The memory range of the 6116 chip is _____ .

Interfacing the Z80 with 2764 EPROM(8K x 8)



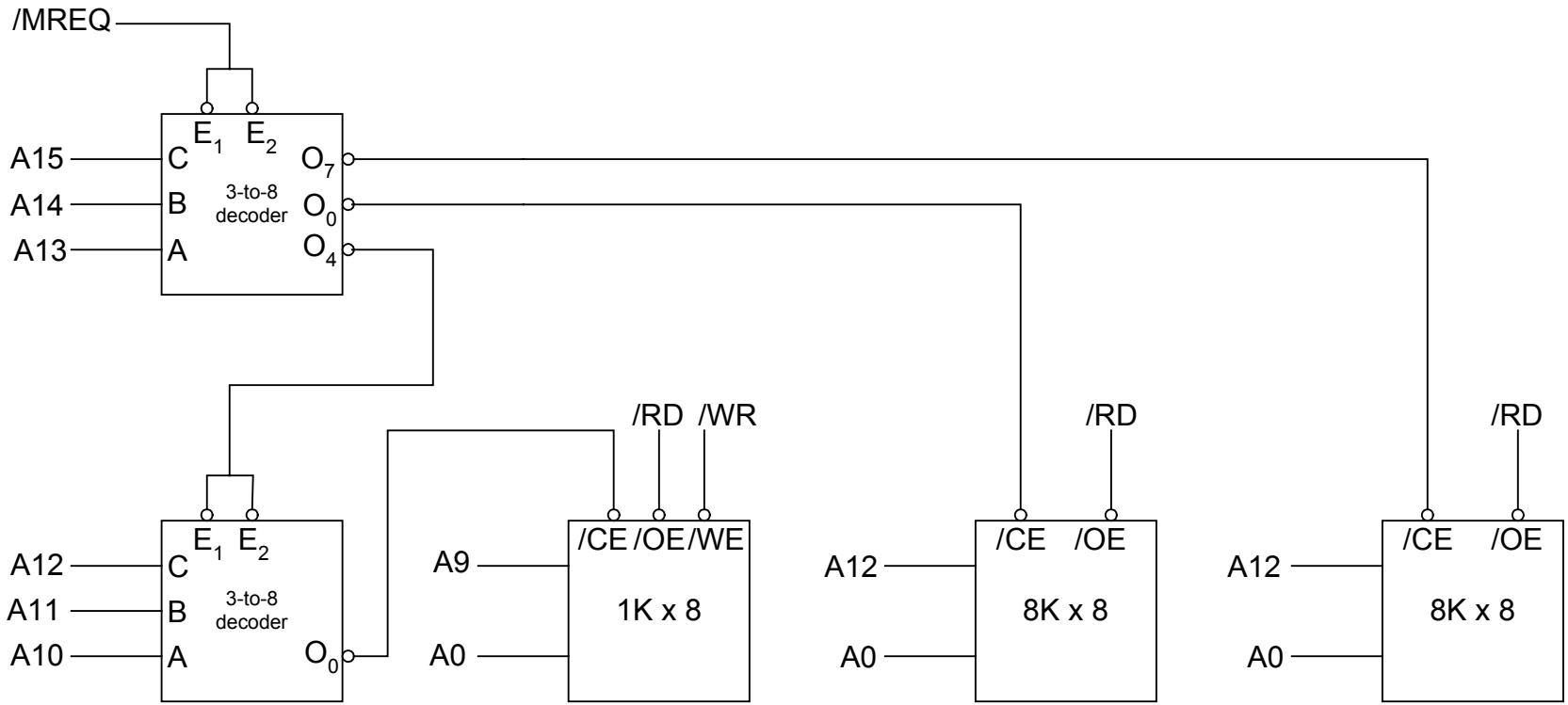
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

The memory range of the 2764 chip is

_____ .

Memory Map

- The Z80 has a 16-bit address bus which can access $2^{16} = 2^6.2^{10} =$ 65,536(64K) memory locations.
- Memory map(0000 to 0FFFFH) is a pictorial representation in which memory chips are located in the entire range of addresses.



Memory Map Continued