Session 9: Solid State Physics

MOS Cap
Outline

- A
  - B
  - C
  - D
  - E
- F
  - G
- H
- I
- J
MOS!

Metal: \( Al, \ldots, \text{Poly Si (n++, p++)} \), \( \rho_{poly} = 0.1 \, m\Omega \text{cm} \)

Oxide: SiO\(_2\) (reason why Si beat GaAs)

Semi Conductor: Si

CMOS is the dominant technology in integrated circuits

Heart of a MOSFET is MOS-cap

\[ \epsilon_{Si} = 11.9 \quad \text{and} \quad (3 \times)\epsilon_{SiO_2} = 3.9 \]
Bulk Semiconductor Potential, $\phi_F$

**Definition:**

$$q\phi_F \equiv E_i - E_F = E_i(\text{bulk}) - E_F$$

\[
\begin{align*}
E_{cp} & \quad E_{cn} \\
E_{fp} & \quad E_{fn} \\
E_{vp} & \quad E_{vn}
\end{align*}
\]

\[p\text{-type}\]

$$\phi_F = \frac{kT}{q} \ln \left(\frac{N_A}{n_i}\right) > 0$$

\[n\text{-type}\]

$$\phi_F = -\frac{kT}{q} \ln \left(\frac{N_D}{n_i}\right) < 0$$
Special case: $\varphi_m = \varphi_s$

$E_0$
$q\chi_i$
$q\varphi_m$
$q\varphi_s$
$q\chi$
$E_C$
$E_G$
$E_{FS}$
$E_{VC}$
$E_Fm$
$E_V$

metal
SiO2
Si, p-type
MOS – Special Case

Special case: \( \varphi_m = \varphi_s \)

- **SiO2 (oxide) → High k**
- **p-type Si (bulk)**
- **Gate**
- **A**
- **Al (metal)**
- **A’**
- **\( t_{ox} \sim 0.1 \mu m \)**
- **\( t_{ox} \sim 5 \text{nm} \)**

Diagram:
- **E\(_V\)**
- **E\(_F_S\)**
- **E\(_C\)**
- **E\(_0\)**
- **q\( \varphi_m \)**
- **q\( \varphi_s \)**
- **q\( \chi \)**
- **q\( \chi_i \)**

Materials:
- **Metal**
- **SiO2**
- **Si, p-type**
M (Al), O (SiO2), S (Si)

$E_0$

$q \varphi_{m_{Al}} = 4.1$

$E_{Fm}$

$E_G = 9 eV$

$E_C$

$q \varphi_s = 4.9 eV$

$q \chi = 4.05 eV$

$E_{F_S}$

$E_V$

metal

SiO2

Si, p-type
Flat Band Voltage

\[ E_0 \]

\[ q\varphi_m = 4.1 \]

\[ qV_G = q\varphi_m - q\varphi_s \]

\[ V_{FB} \equiv \varphi_m - \varphi_s = \varphi_{ms} \]

\[ V_{FB} = -0.8 \, V \]

metal

Si, p-type

\[ q\varphi_s = 4.9eV \]

\[ q\chi = 4.05eV \]
Voltage Barrier

$q\varphi_{m_{\text{Al}}} = 4.1$

$E_0$

$E_m$

$qV_G$

$V_G = V_{FB} = -0.8\ V$

No way electrons might pass the voltage barrier!
No Gate Voltage

$V_G = 0 \text{ V}$

$q\varphi_{mAl} = 4.1eV$

$q\varphi_s = 4.9eV$

$q\chi = 4.05eV$

$E_Fm$

$E_Fs$

$E_C$

$E_V$

metal

Si, p-type

$E_0$

$0.8\text{ V}$

$0.95$

$3.15eV$

$3.1eV$
Boundary Condition

\[ D_{2n} - D_{1n} = \rho_{surface} \]

\[ \rho_{surface} = 0 \]

\[ \varepsilon_1 \varepsilon_1 = \varepsilon_2 \varepsilon_2 \]

\[ \varepsilon_0 \frac{dE_{Ox}}{dx} \bigg|_{int} = \varepsilon_{Si} \frac{dE_{Si}}{dx} \bigg|_{int} \]

\[ \frac{dE_{Ox}}{dx} \bigg|_{int} \approx 3 \frac{dE_{Si}}{dx} \bigg|_{int} \]
M (PolyGate), O (SiO2), S (Si)

\[ q\chi = 4.05\text{eV} \]

\[ q\phi_s = 4.9\text{eV} \]

\[ V_{FB} = \phi_m - \phi_s = -0.85\text{V} \]
No Gate Voltage – Poly Gate

$V_G = 0 \text{ V}$

metal

Si, p-type

$q\chi = 4.05eV$

$q\phi_s = 4.9eV$

$E_C$

$E_Fm$

$E_V$

$E_0$

$E_C$

$E_{Fs}$

$E_V$

$0.95$

$3.1eV$

$3.1eV$

$q\chi = 4.05eV$
No Gate Voltage

\[ V_G = 0 \, V \]

metal

Si, p-type
No Gate Voltage

As important as KVL

\[ V_G - V_{FB} = V_{Oxide} + V_{Si} = V_{Ox} + \varphi_s \]
Flat Band

\[ V_G = V_{FB} \]
Accumulation

$V_G < V_{FB}$

$E_F$  

$qV_{FB}$

$E_C$

$E_F$

$E_V$

$\rho$

$+Q$

$\mathcal{E}$

$-Q$

$x$

$x$
Flat Band

\[ V_G = V_{FB} \]
Depletion (Weak Inversion)

\[ V_T > V_G > V_{FB} \]
(Strong) Inversion

\[ V_G > V_T \]
Depletion (Weak Inversion)

\[ V_T > V_G > V_{FB} \]

\[ \frac{d\varepsilon}{dx} = \frac{\rho}{\varepsilon_{Si}} = -\frac{qN_A}{\varepsilon_{Si}} = \frac{d^2\varphi}{dx^2} \]

\[ \varphi_s = \frac{qN_A x^2}{2\varepsilon_{Si}} \]

\[ W_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A \varphi_s}} \]

\[ Q_{dep} = -qN_A W_d = \sqrt{2qN_A\varepsilon_{Si} \varphi_s} \]

\[ \varepsilon_{Ox} = \frac{-Q_{dep}}{\varepsilon_{Ox}} \quad \Rightarrow \quad V_{Ox} = \frac{-t_{ox} Q_{dep}}{\varepsilon_{Ox}} = -\frac{Q_{dep}}{C_{Ox}} \quad \text{[C/cm}^2\text{]} \]

\[ V_G = V_{FB} + V_{Ox} + \varphi_s \quad \Rightarrow \quad V_G = V_{FB} + \varphi_s + \frac{1}{C_{Ox}} \sqrt{2qN_A\varepsilon_{Si} \varphi_s} \quad \text{p-type Si (nMOS)} \quad \text{In Depl} \]

\[ \varphi_s < 0 \]

\[ V_G = V_{FB} + \varphi_s - \frac{1}{C_{Ox}} \sqrt{2qN_A\varepsilon_{Si} |\varphi_s|} \quad \text{n-type Si (pMOS)} \quad \text{In Depl} \]
Threshold Voltage – Definition!

\[ V_G = 0 \]
\[ V_G > 0 \]
\[ V_G = V_T \]
Threshold Voltage

\[ V_G = V_T \]

Definition of Threshold voltage:

\[ V_T = V_G \bigg|_{\varphi_s = 2\varphi_F} \]

\[ p_{\text{bulk}} = N_A \hspace{1cm} n_{\text{surface}} = N_A \]

\[ W_{\text{max}} = W_{\text{depl}} \bigg|_{\varphi_s = 2\varphi_F} = \sqrt{\frac{2\varepsilon_S}{qN_A}(2\varphi_F)} \]

p-type

\[ V_T = V_G \bigg|_{\varphi_s = 2\varphi_F} = V_{\text{FB}} + 2\varphi_F + \frac{1}{C_{\text{Ox}}} \sqrt{2qN_A\varepsilon_S(2\varphi_F)} \]

n-type

\[ V_G = V_{\text{FB}} + 2\varphi_F - \frac{1}{C_{\text{Ox}}} \sqrt{2qN_A\varepsilon_S|2\varphi_F|} \]

\[ q\varphi_F = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) > 0 \]

\[ q\varphi_F = -\frac{kT}{q} \ln \left( \frac{N_D}{n_i} \right) < 0 \]
Threshold Voltage vs. Bulk Doping

$p$-type

$n$-type

$V_T$ vs. $\ln N_A$

$V_T$ vs. $\ln N_D$
MOS Band Diagram (n-type Bulk)

Decrease $V_G$ (toward more negative values)
→ move the gate energy-bands up, relative to the Si

• Accumulation
  – $V_G > V_{FB}$
  – Electrons accumulate at surface

• Depletion
  – $V_G < V_{FB}$
  – Electrons repelled from surface

• Inversion
  – $V_G < V_T$
  – Surface becomes p-type
Accumulation, Poly Gate

$V_G < V_{FB}$

Mobile carriers (holes) accumulate at Si surface
Accumulation, Layer Charge Density

\[ V_G < V_{FB} \]

\[ V_{Ox} \approx V_G - V_{FB} \]

From Gauss’ Law:

\[ \varepsilon_{Ox} = -\frac{Q_{acc}}{\varepsilon_{SiO_2}} \]

\[ V_{Ox} = t_{Ox} \varepsilon_{Ox} = -\frac{Q_{acc}}{C_{Ox}} \]

where \( C_{Ox} \equiv \frac{\varepsilon_{SiO_2}}{t_{Ox}} \) \([F/cm^2]\)

\[ Q_{acc} = -C_{Ox} (V_G - V_{FB}) > 0 \]
Depletion, Poly Gate

\[ V_G < V_{FB} \]

Si surface is depleted of mobile carriers (holes)
=> Surface charge is due to ionized dopants (acceptors)
Depletion (Weak Inversion)

\[ V_T > V_G > V_{FB} \]

\[ d\varepsilon \quad d\xi = \frac{-qN_A}{\varepsilon_{Si}} = \frac{d^2\varphi}{dx^2} \quad \rightarrow \quad \varphi_s = \frac{qN_Ax^2}{2\varepsilon_{Si}} \]

\[ \rightarrow W_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}} \varphi_s \quad \quad V_{Ox} = \frac{-Q_{dep}}{C_{Ox}} \]

\[ V_G = V_{FB} + V_{Ox} + \varphi_s \quad \rightarrow \quad V_G = V_{FB} + \varphi_s + \frac{1}{C_{Ox}} \sqrt{2qN_A\varepsilon_{Si}\varphi_s} \]

Solving for \( \varphi_s \):

\[ \varphi_s = \frac{qN_A\varepsilon_{Si}}{2C_{Ox}^2} \left[ \sqrt{1 + \frac{2C_{Ox}^2}{qN_A\varepsilon_{Si}}(V_G - V_{FB}) - 1} \right]^2 \]

\[ Q_{dep} = -qN_AW_d = -\sqrt{2qN_A\varepsilon_{Si}\varphi_s} \]
**Strong Inversion**

As $V_G$ is increased above $V_T$, the negative charge in the Si is increased by adding mobile electrons (rather than by depleting the Si more deeply), so the depletion width remains $\sim$ constant at $W = W_T$

$$\phi_s \approx 2\phi_F \quad \rightarrow \quad W \approx W_T = \frac{2\epsilon_{Si}}{qN_A} (2\phi_F)$$

$$V_G = V_{FB} + \phi_s + V_{Ox}$$

$$= V_{FB} + 2\phi_F - \frac{Q_{dep} + Q_{inv}}{C_{Ox}}$$

$$= V_{FB} + 2\phi_F - \frac{\sqrt{2q\epsilon_{Si}N_A(2\phi_F)}}{C_{Ox}} - \frac{Q_{inv}}{C_{Ox}}$$

$$V_G = V_T - \frac{Q_{inv}}{C_{Ox}}$$

$\therefore \quad Q_{inv} = -C_{Ox}(V_G - V_T)$
$\varphi_s$ and $W$ vs. $V_G$

$\varphi_s$:

$\varphi_s = \frac{qN_A\varepsilon_{Si}}{2C_{\partial x}^2} \left[ \sqrt{1 + \frac{2C_{\partial x}^2}{qN_A\varepsilon_{Si}} (V_G - V_{FB})} - 1 \right]^2$  

$(V_{FB} < V_G < V_T)$

$W$:

$W = \frac{\varepsilon_{Si}}{C_{ox}} \left[ \sqrt{1 + \frac{2C_{\partial x}^2}{qN_A\varepsilon_{Si}} (V_G - V_{FB})} - 1 \right]$  

$(V_{FB} < V_G < V_T)$
Total Charge Density in Si, $Q_S$

$Q_{acc}$:

$Q_{acc} = -C_{ox}(V_G - V_{FB})$

$Q_{dep}$:

$Q_{dep} = -qN_AW$

$Q_{inv}$:

$Q_{inv} = -C_{ox}(V_G - V_T)$

$Q_S = Q_{acc} + Q_{dep} + Q_{inv}$

$Q_S$:

Slope = $-C_{ox}$
MOS C-V Characteristics

\[ Q_S: \]
\[ V_{FB} \quad \text{accumulation} \quad V_T \quad \text{depletion} \quad V_G \quad \text{inversion} \]
\[ \text{Slope} = -C_{ox} \]

\[ C = \left| \frac{dQ_{gate}}{dV_G} \right| = \left| \frac{dQ_S}{dV_G} \right| \]

\[ \begin{align*}
\text{accumulation} & \quad \text{depletion} & \quad \text{inversion} \\
V_{FB} & \quad V_T & \quad V_G
\end{align*} \]
Debye Length

- As the gate voltage is varied, incremental charge is added/subtracted to/from the gate and substrate.
- The incremental charges are separated by the gate oxide.

\[
\frac{d^2 \varphi}{dx^2} = -\frac{\rho}{\varepsilon} = \frac{q}{\varepsilon} (N_D - N_A + p - n)
\]

n-type bulk:

\[
\frac{d^2 \varphi}{dx^2} = \frac{q}{\varepsilon} (N_D - n) e^{-\varphi/\varphi_{th}}
\]

\[
= \frac{q}{\varepsilon} N_D \left(1 - e^{\varphi/\varphi_{th}}\right)
\]

implies

\[
\frac{q}{\varepsilon} N_D \frac{\varphi}{\varphi_{th}} = \frac{\varphi}{L_D^2}
\]

\[
L_D = \sqrt{\frac{\varepsilon kT}{q^2 N_D}}
\]
Flat-Band Capacitance

\[ C_{FB} = \frac{C_{Ox} C_D}{C_{Ox} + C_D} \]

\[ \frac{1}{C_{FB}} = \frac{t_{Ox}}{\varepsilon_{Ox}} + \frac{L_D}{\varepsilon_{Si}} \]

\[ \frac{1}{C} = \frac{t_{Ox}}{\varepsilon_{Ox}} + \frac{W_{dep}}{\varepsilon_{Si}} \]
Capacitance in Inversion

CASE 1: Inversion-layer charge can be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at the surface of the substrate.

Time required to build inversion-layer charge = \(2N_A\tau_0/n_i\), where \(\tau_0\) = minority-carrier lifetime at the surface

\[
C = \left| \frac{dQ_{inv}}{dV_G} \right| = C_{Ox}
\]
**Capacitance in Inversion**

**CASE 2:** Inversion-layer charge *can not* be supplied/removed quickly enough to respond to changes in the gate voltage.

Incremental charge is effectively added/subtracted at depth $W_T$ in the substrate.

\[
\frac{1}{C} = \frac{1}{C_{Ox}} + \frac{1}{C_{dep}} \\
= \frac{1}{C_{Ox}} + \frac{W_T}{\varepsilon_{Si}} \\
= \frac{1}{C_{Ox}} + \sqrt{\frac{2(2\varphi_F)}{qN_A\varepsilon_{Si}}} \equiv \frac{1}{C_{min}}
\]
Supply of Inversion Charge

Accumulation:

Depletion:

Inversion:

Case 1

Case 2
Boundary Condition

1. MOS transistor at any f,
2. MOS capacitor at low f, or quasi-static C-V
3. MOS capacitor at high f

\[ C(V_G) \]

- Accumulation: \[ V_{FB} \]
- Depletion: \[ C_{min} \]
- Inversion: \[ V_T \]
Deep Depletion

If $V_G$ is scanned quickly, $Q_{\text{inv}}$ cannot respond to the change in $V_G$. The increase in substrate charge density $Q_s$ must then come from an increase in depletion charge density $Q_{\text{dep}}$

$\Rightarrow$ depletion depth $W$ increases as $V_G$ increases

$\Rightarrow C$ decreases as $V_G$ increases
## Boundary Condition

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Oxide Charges

In real MOS devices, there is always some charge in the oxide and at the Si/oxide interface.

In the oxide:

1. Trapped charge $Q_{ox}$
   High-energy electrons and/or holes injected into oxide

2. Mobile charge $Q_M$
   Alkali-metal ions, which have sufficient mobility to drift in oxide under an applied electric field

At the interface:

1. Fixed charge $Q_F$
   Excess Si (+)

2. Trapped charge $Q_{IT}$
   Dangling bonds
Effect of Oxide Charges

In general, charges in the oxide cause a shift in the gate voltage required to reach the threshold condition:

$$
\Delta V_T = - \frac{1}{\varepsilon_{SiO_2}} \int_0^{t_{Ox}} x \rho_{0x}(x) dx
$$

(x defined to be 0 at metal-oxide interface)

In addition, they may alter the field-effect mobility of mobile carriers (in a MOSFET) due to Coulombic scattering.
Fixed Oxide Charges $Q_F$

$V_{FB} = \varphi_{ms} - \frac{Q_F}{C_{Ox}}$

$E_C \quad E_F$

$E_V \quad |qV_{FB}|$

$4.8eV$

$3.1eV$

$qQ_F/C_{Ox}$
Parameter Extraction from C-V

From a single C-V measurement, we can extract much information about the MOS device.

Suppose we know that the gate-electrode material is heavily doped n-type poly-Si ($\varphi_M = 4.05\text{eV}$), and that the gate dielectric is SiO2 ($\varepsilon_r = 3.9$):

- From $C_{\text{max}} = C_{Ox}$ we determine the oxide thickness $x_0$
- From $C_{\text{min}}$ and $C_{Ox}$ we determine substrate doping (by iteration)
- From substrate doping and $C_{Ox}$ we calculate the flat-band capacitance $C_{FB}$
- From the C-V curve, we can find
- From $\varphi_M, \varphi_S, C_{Ox}$, and $V_{FB}$ we can determine $Q_F$
Determination of $\varphi_M$ and $Q_F$

Measure C-V characteristics of capacitors with different oxide thicknesses.
Plot $V_{FB}$ as a function of $x_0$:

$$V_{FB} = \varphi_{ms} - \frac{Q_F}{\varepsilon_{SiO_2}} t_{ox}$$
Odd shifts in C-V characteristics were once a mystery:

Source of problem: Mobile charge moving to/away from interface, changing charge centroid

\[ \Delta V_{FB} = -\frac{Q_M}{C_{OX}} \]
Interface Traps

Traps cause “sloppy” C-V and also greatly degrade mobility in channel

\[ \Delta V_G = - \frac{Q_{IT}(\varphi_s)}{C_{Ox}} \]
A heavily doped film of polycrystalline silicon (poly-Si) is typically employed as the gate-electrode material in modern MOS devices.

There are practical limits to the electrically active dopant concentration (usually less than $1 \times 10^{20} \text{ cm}^{-3}$).

⇒ The gate must be considered as a semiconductor, rather than a metal.
Si biased to inversion:

$V_G > V_T$

$V_G$ is effectively reduced:

$$Q_{inv} = C_{ox} (V_G - V_{poly} - V_T)$$

$$W_{poly} = \sqrt{\frac{2\epsilon_{Si} V_{poly}}{qN_{poly}}}$$

How can gate depletion be minimized?
Gate Depletion Effect

Gauss’s Law dictates:

\[ W_{\text{poly}} = \frac{\varepsilon_{\text{ox}} \varepsilon_{\text{ox}}}{q N_{\text{poly}}} \]

\( t_{\text{ox}} \) is effectively increased:

\[ C = \left( \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{poly}}} \right)^{-1} = \left( \frac{t_{\text{ox}}}{\varepsilon_{\text{SiO}_2}} + \frac{W_{\text{poly}}}{\varepsilon_{\text{Si}}} \right)^{-1} \]

\[ = \frac{\varepsilon_{\text{SiO}_2}}{t_{\text{ox}} + \frac{1}{3} W_{\text{poly}}} \]

\[ Q_{\text{inv}} = C_{\text{ox}}(V_G - V_{\text{poly}} - V_T) \]

\[ Q_{\text{inv}} = \frac{\varepsilon_{\text{SiO}_2}}{t_{\text{ox}} + \frac{1}{3} W_{\text{poly}}} (V_G - V_T) \]
Inversion Layer Thickness $T_{\text{inv}}$

The average inversion-layer location below the Si/SiO$_2$ interface is called the inversion-layer thickness, $T_{\text{inv}}$. $V_G > V_T$
Effective Oxide Thickness, $T_{Oxe}$

\[ T_{Oxe} = t_{Ox} + \frac{1}{3}W_{poly} + \frac{1}{3}T_{inv} \]

@ $V_G = V_{DD}$

$(V_G + V_T)/T_{Ox}$ can be shown to be the average electric field in the inversion layer. $T_{inv}$ of holes is larger than that of electrons because of the difference in effective masses.
Effective Oxide Capacitance, $C_{Oxe}$

\[ Q_{\text{inv}} = C_{Oxe}(V_G - V_T) \]

\[ T_{Oxe} = t_{Ox} + \frac{1}{3}W_{\text{poly}} + \frac{1}{3}T_{\text{inv}} \]
MOS Cap: Equivalent Circuit in Depletion & Inversion

General case for both depletion and inversion regions.

In the depletion regions

\[ V_G \approx V_T \]

Strong inversion
In modern IC fabrication processes, the threshold voltages of MOS transistors are adjusted by ion implantation:

- A relatively small dose $N_I$ (units: ions/cm$^2$) of dopant atoms is implanted into the near-surface region of the semiconductor.
- When the MOS device is biased in depletion or inversion, the implanted dopants add to the dopant-ion charge near the oxide-semiconductor interface.

$$\Delta V_T = -\frac{qN_I}{C_{Ox}}$$

- $N_I > 0$ for donor atoms
- $N_I < 0$ for acceptor atoms
Dynamic \( V_T \) Adjustment Bulk Voltage

\[ V_T = V_{FB} + 2\varphi_F + \frac{Q_{depl}}{C_{Ox}} \]

1. 
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\[ V_T = V_{FB} + V_C + 2\varphi_F + \frac{Q_{depl}}{C_{Ox}} \]

\[ Q_{depl} = \sqrt{2qN_A\varepsilon_{Ox}(V_{BC} + 2\varphi_F)} \]
CCD Imager and CMOS Imager

Deep depletion, $Q_{inv} = 0$ 
Exposed to light