VLSI Interconnect – HW01 – due 21 Farvardin

The goal is this HW is to get familiar with the trend of VLSI technology. Use latest ITRS2015 reports available at http://www.itrs2.net/itrs-reports.html or https://www.semiconductors.org/main/2015_international_technology_roadmap_for_semiconductors_itrs/, to answer the following questions. Use older versions of ITRS for the items not showed in ITRS2015.

1. Descriptions:

- Describe following terms briefly:
  "Ideal MOS Transistor" , "2.5Dvs. 3D Integration", "beyond CMOS options",
- Draw three different structures of TSVs: First, Middle, and Last.

2. Minimum Feature Size

- What is the difference between "Flash 1/2 pitch", "DRAM 1/2 pitch", "MPU 1/2 pitch", "Printed Gate Length", and "Physical Gate Length"?
- Make a plot comparing these parameters as a function of year.

3. Oxide Thickness

- Make a plot of T_{OX} "transistor oxide thickness" and "gate leakage per unit micron" as a function of year.

4. Supply Voltage (V_{DD})

- Make a plot of "V_{DD} projections" and the ratio of the threshold voltage (V_T) to the supply voltage (V_{DD}) for different processors as a function of year.

5. Drive Current (I_{ON}) vs. Off Current (I_{OFF})

- Make a plot of the I_{ON} current (in mA/µm) as a function of year.
- Make a plot of the I_{OFF} current (in mA/µm) as a function of year.
- Make a plot of the I_{ON}/I_{OFF} as a function of year.

6. CV/I Metric, Clock Frequency

- Make a plot of the "$t = CV/I$ metric" and "$T = 1/f$"as a function of year. ($t = CV/I$ is called the intrinsic delay and f is the on-chip local clock)

7. Chip Size, Power Dissipation

- Make a plot of the P "power dissipation" projected for the next generations. Given that you know the supply voltage projections, find the "I_{avg} =average current per gate" for different generations. Knowing that "I_G =current per logic gate" is k times "average current per gate". Plot I_G as a function of year for $k = 10$.
- Make a plot of the "A=chip size" at production as a function of year. Knowing the number of transistors (N_T) for each generation and assuming that (by average) each gate consists of 6 transistors, relate "G_P=gate pitch" to A and N_T. Plot G_P=gate pitch" as a function of year.

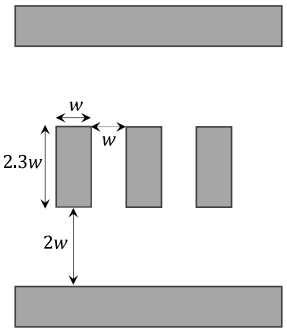

Figure 1

- Estimate the ratio of the power dissipation in the wires to the power dissipation in the gates (P_w/P_G). You may use the total wire length given in the ITRS and assume the total wire length given in the ITRS and assume that the wiring structure is as shown in Figure 1.
- **(Extra credit)** Having an estimation about wire length distribution, Assume the same chip being manufactured in 3D technology with 4 active layers of devices with total chip footprint reduced to ¼ . Assume clock frequency and all other factors are kept the same. Talk about the change in the total chip power dissipation and chip temperature.

8. Wire Delay

- Wire RC delay is defined as $t_w = RC$, where R and C are resistance and capacitance of the wire. Consider structure as shown in Figure 1. Assume length of the wire is $L = 100\mu m$ and W is the minimum wire size for each technology generation. Plot t_w/t as a function of year.
- L^* is defined as the length of the wire at which t_w is equal to $t = CV/I$ for that technology generation. Plot L^* vs. year. Assume repeater insertion and recalculate L^* and plot it on the previous curve. (use data in ITRS to extract R_0 and C_0 for the repeater) (*Hand in the repeater part later!*)

(Extra credit) 9. Read "Executive Summary of the ITRS 2013 and list all difficult challenges related to "interconnect." Specifically, highlight those related to the "modeling."

(Extra credit) 10. Think of a method to plot as much important information as possible on a single plot (one possible idea could be: plotting all important variables vs. year, normalized to their value in the starting generation). Make such a plot based on the variables that you think contain the most important date for each technology generation.

(Extra credit) 11. Find a distributed circuit model which result in the following PDE. (you are not allowed to use dependent source but you may consider position-dependent elements!)

$$\frac{\partial^2 V}{\partial x^2} + \alpha \frac{\partial V}{\partial x} = \beta \frac{\partial V}{\partial t}$$