

Prediction of Net-Length Distribution for Global Interconnects in a Heterogeneous System-on-a-Chip

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Abstract—A system-on-a-chip (SoC) contains several pre-designed heterogeneous megacells that have been designed and routed optimally. In this paper a new stochastic net-length distribution for global interconnects in a nonhomogeneous SoC is derived using novel models for netlist, placement, and routing information. The netlist information is rigorously derived based on heterogeneous Rent's rule, the placement information is modeled by assuming a random placement of terminals for a given net in a bounding area, and the routing information is constructed based on a new model for minimum rectilinear Steiner tree construction (MRST). The combination of the three models gives a priori estimation of global net-length distribution in a heterogeneous SoC. Unlike previous models that empirically relate the average length of the global wires to the chip area, the new distribution provides a complete and accurate distribution of net-length for global interconnects. Through comparison with actual product data, it is shown that the new stochastic model successfully predicts the global net-length distribution of a heterogeneous system.

Index Terms—Global interconnect, heterogeneous Rent's rule, netlist model, placement model, routing model, Slip99: system level interconnect, system-on-a-chip.

I. INTRODUCTION

SYSTEM level integration is evolving as a new paradigm, allowing an entire system to be built on a single chip, using pre-designed functional blocks called megacells. The performance of a system-on-a-chip (SoC) is often determined by interconnect wiring requirements of the system. Moreover, *system level wire-length distribution* is a key factor in timing analysis, designing, floorplanning, routing of a SoC, and studying of the wiring resource limit at the global level. The prediction of wire-length distribution at the early stage of the chip design (*a priori* estimation) can help the designer to: 1) optimize the interconnect structure to meet the minimum chip size with the maximum clock frequency [1] and 2) improve the results derived from CAD tools for layout by providing information such as minimum number of metal levels for wireability [2]. Although *a priori* estimation doesn't offer the accuracy of CAD tools, it provides the above information before the layout design with almost no cost.

For the first time, a real breakthrough in the estimate of a wire length distribution was reported by Donath [3] in 1981. In his paper, Donath discussed, using a hierarchical method, that the wire length distribution should follow a power law function for most of the wires until it drops rapidly to zero for long wires. The

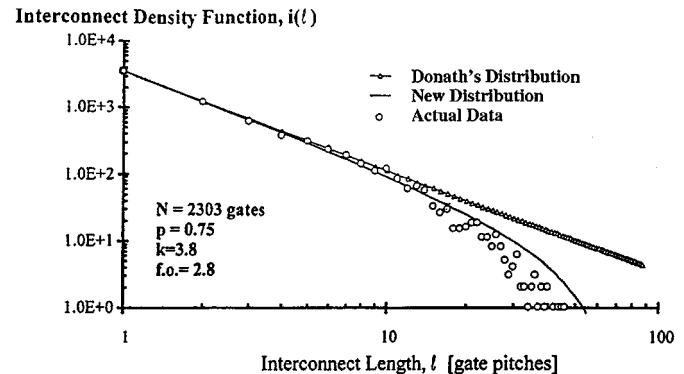


Fig. 1. Comparison of Davis' stochastic wiring model [5] to actual data and Donath's model.

underlying assumption of his model is based on a well-established empirical relationship commonly known as Rent's rule [4]. A more accurate wire-length distribution, compared to the previous model, has been derived recently by Davis *et al.* [5]. In the new method, the gates are grouped into three distinct but adjacent blocks. By applying the principle of conservation of I/O's to the three-block system and using Rent's rule, a complete wire length distribution is determined. Fig. 1 illustrates the accuracy of the new model compared to the previous distribution. The primary assumption of the Davis *et al.* wire-length distribution model is that each block consists of a uniform and homogeneous collection of gates and therefore this model is suitable only for prediction of wire-length distribution *within* the homogeneous blocks in a system. The new model derived in this paper is not subject to this restriction and applies to a heterogeneous set of megacells.

The prediction of global wiring demand in a nonhomogeneous system requires more information about the system such as netlist, placement, and routing. Karp *et al.* [6] demonstrate a wiring model for global interconnects under netlist assumptions. They show that a simple model can relate the average global wire length to a fraction of chip size. Sorkin [7] presents a stochastic global wiring model, which has the disadvantage of requiring even more assumptions about the chip. His conclusion, though, gives a similar relationship for the average wire length, which is roughly one-third of the semi-perimeter of the chip.

It has been previously observed that the overall wire-length distribution, at the system level, has a bimodal behavior [8], as shown in Fig. 2. The distribution has two peaks—the first peak representing internal megacell interconnects, and the second representing global interconnects that provide communication between megacells. The reason for the bimodal behavior in wire length distribution is that the placement and routing of

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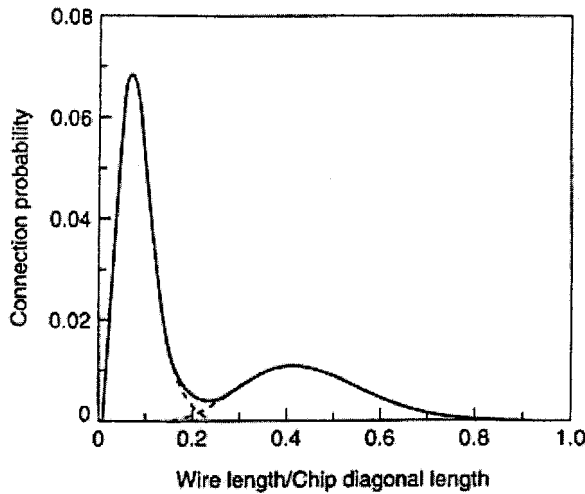


Fig. 2. Typical distribution of wire lengths in an integrated system.

the lower levels (*within* the megacells) are done independently of the higher level (*between* the megacells) in SoC designs. However, the models derived in this paper apply to both single mode and bimodal distributions.

Since global net-lengths are usually longer than local nets within megacells, the overall performance of a chip is often limited by its global wiring network [9], [10]. It is, therefore, imperative to gain thorough understanding of the global wiring requirements for present and projected SoC designs. To enhance this understanding, for the first time a stochastic net-length distribution for global interconnects is derived in this paper. Unlike previous models [6], [7] that empirically relate the average length of the global wires to the chip size, the new distribution provides a complete and accurate global net-length distribution at the very early stage of the design since it utilizes the models for netlist, placement, and routing at the same time. The complete system level wire-length distribution for a heterogeneous SoC can be obtained by combining the new global wiring distribution with the internal wiring distributions of all megacells, as presented in [5].

Fig. 3 represents three novel stochastic models for netlist, placement, and routing information that are used to derive the global net-length distribution [11]. The netlist information is derived based on heterogeneous Rent's rule [12], as shown in Section II. Since the stochastic variations are fairly significant at the global level, a probabilistic method is utilized for the placement and routing models. Section III introduces the placement information by assuming a random placement of terminals for a given net. Section IV describes the routing information based on a new model for minimum rectilinear Steiner tree (MRST) construction. The combination of the three models gives the global net-length distribution, as shown in Section V.

II. STOCHASTIC NETLIST INFORMATION

The netlist information defines the connectivity between megacells or fan-out distribution of the SoC (i.e., the number of nets versus fan-out [13]). To predict the number of nets between megacells, a well-established empirical relationship known as Rent's rule is used. This relationship correlates the number of

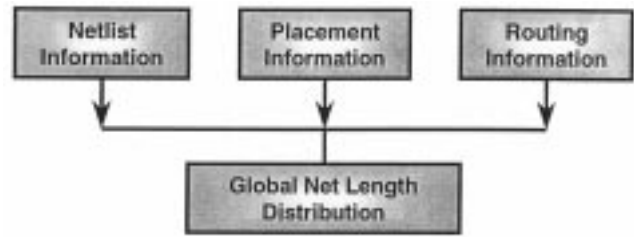


Fig. 3. Global net-length model structure.

I/O terminals T to the number of gates N in a homogeneous logic network. This correlation is given by a simple power-law expression as

$$T = kN^p \quad (1)$$

where k and p are the Rent's coefficient and exponent, respectively. Since a SoC is a heterogeneous network containing different varieties of megacells, a new definition of Rent's rule for such heterogeneous systems is required. The new heterogeneous Rent's rule [12] is rigorously derived in this section. It is shown that the same power-law expression as (1) is also valid for heterogeneous networks with equivalent k and p parameters

$$\begin{cases} k_{\text{eq}} = N_{G_{\text{eq}}} \sqrt[n]{\left(\prod_{i=1}^n k_i^{N_{G_i}} \right)} \\ p_{\text{eq}} = \frac{\sum_{i=1}^n p_i N_{G_i}}{N_{G_{\text{eq}}}} \end{cases} \quad (2)$$

where k_i and p_i are the usual Rent's rule parameters, N_{G_i} is the equivalent number of gates in the i th megacell and $N_{G_{\text{eq}}} = \sum_{i=1}^n N_{G_i}$.

A. Heterogeneous Rent's Rule

Rent's rule is a simple power-law relationship between the number of I/O terminals of a logic block T and the number of gates contained in that block N . Specifically, [4]

$$T = kN^p \quad (3)$$

where k is the average number of terminals per gate and p reflects the connectivity of the gates in a homogeneous megacell. A homogeneous megacell, by definition, is a large block of identical gates, which is designed to fulfill a specific purpose. For instance, in a heterogeneous SoC, there are several blocks of memory, data path, control unit, etc. Each block is considered as a megacell. Going further into the hierarchy of the design, a megacell may consist of several macrocells. The macrocells have different size (in terms of number of gates inside) and they can be repeatedly used in the design. The smallest macrocell is a single gate. The connectivity between the macrocells defines the complexity of the megacells, which is represented by the Rent's rule parameters k and p .

Early compelling evidence of Rent's rule was presented in a study by Landman and Russo [4], who partitioned various computer logic systems. Fig. 4 is a plot of the average number of pins versus the average number of gates per macrocell for a particular logic design [4]. Besides Rent's rule, there is another important relationship between the average number of macrocells and the average number of gates per macrocell. To illustrate this

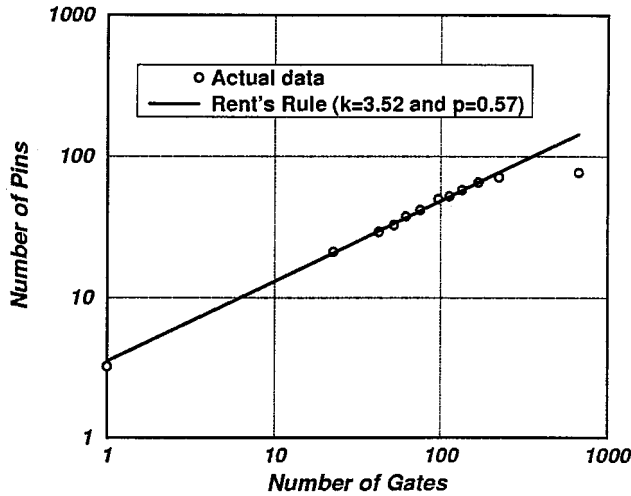


Fig. 4. Average number of pins versus average number of gates per macrocell, after [4].

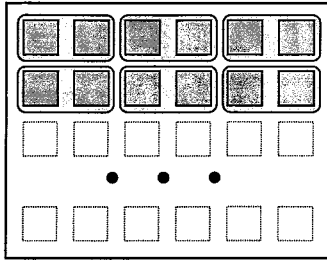


Fig. 5. Partitioning gates to make macrocells.

relationship, consider a rectangular array of N_G gates as seen in Fig. 5.

Suppose, for example, the gates in Fig. 5 are grouped into macrocells containing two gates each. The number of macrocells in this case is $N_G/2$. In general, if N gates are grouped into a macrocell, then the number of macrocells is N_G/N . Thus, the average number of macrocells (M) or population function is

$$M = \frac{N_G}{N}. \quad (4)$$

Now consider a simple 2-block heterogeneous system, as shown in Fig. 6. Megacell#1 and megacell#2 are homogeneous sub-systems with N_{G1} and N_{G2} total gates, and $k_1, p_1, k_2,$ and p_2 , as Rent's parameters, respectively. In order to find k_{eq}, p_{eq} and N_{Geq} , that describe this system as a collective, we use both relationships (3) and (4). The first one is Rent's rule

$$\begin{cases} \text{Megacell\#1 } T_1 = k_1 N^{p_1} \\ \text{Megacell\#2 } T_2 = k_2 N^{p_2}. \end{cases} \quad (5)$$

The second relationship is a population function that describes the number of macrocells

$$\begin{cases} \text{Megacell\#1 } M_1 = N_{G1}/N \\ \text{Megacell\#2 } M_2 = N_{G2}/N. \end{cases} \quad (6)$$

For this heterogeneous system, the overall number of macrocells with N gates is simply the sum of the number of N -gate macrocells in both megacells. Thus,

$$M_{eq} = M_1 + M_2 = \frac{N_{G1}}{N} + \frac{N_{G2}}{N} = \frac{N_{G1} + N_{G2}}{N}. \quad (7)$$

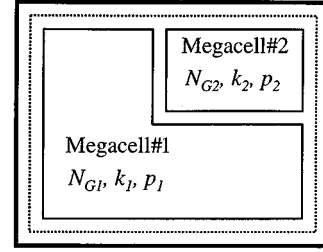


Fig. 6. Simple 2-block heterogeneous system with equivalent N_{Geq}, k_{eq}, p_{eq} .

For the overall system, we can write

$$M_{eq} = \frac{N_{Geq}}{N}. \quad (8)$$

Equations (7) and (8) are validated by the obvious result

$$N_{Geq} = N_{G1} + N_{G2}. \quad (9)$$

Likewise, the average number of terminals of an N -gate macrocell can be computed for the heterogeneous system. In a log-log plot of T versus N , the best fit to a variety of curves (i.e., from a heterogeneous set of blocks) results in a weighted arithmetic average of the logarithm of T for each curve

$$\log T_{eq} = \frac{M_1 \log T_1 + M_2 \log T_2}{M_1 + M_2}. \quad (10)$$

Equation (10) demonstrates the geometric average of the number of terminals. Note that the geometric average is used here because only the geometric average of a set of power law functions is a power law function. From (10)

$$\begin{aligned} T_{eq} &= \left[T_1^{M_1} T_2^{M_2} \right]^{\frac{1}{M_1 + M_2}} \\ &= \left[(k_1 N^{p_1})^{N_{G1}/N} (k_2 N^{p_2})^{N_{G2}/N} \right]^{\frac{1}{(N_{G1}/N) + (N_{G2}/N)}} \\ &= \left[k_1^{N_{G1}} N^{p_1 N_{G1}} k_2^{N_{G2}} N^{p_2 N_{G2}} \right]^{\frac{1}{N_{G1} + N_{G2}}} \\ T_{eq} &= \left(k_1^{N_{G1}} k_2^{N_{G2}} \right)^{\frac{1}{N_{G1} + N_{G2}}} N^{\frac{p_1 N_{G1} + p_2 N_{G2}}{N_{G1} + N_{G2}}}. \end{aligned} \quad (11)$$

This equation shows the overall system also obeys Rent's rule

$$T_{eq} = k_{eq} N^{p_{eq}} \quad (12)$$

with

$$\begin{cases} k_{eq} = \left(k_1^{N_{G1}} k_2^{N_{G2}} \right)^{\frac{1}{N_{G1} + N_{G2}}} \\ p_{eq} = \frac{p_1 N_{G1} + p_2 N_{G2}}{N_{G1} + N_{G2}}. \end{cases} \quad (13)$$

Therefore, the overall heterogeneous system can be described by (12) and (13). Fig. 7 shows the general case, where n different megacells are included in a single chip. Using the same strategy, the equivalent Rent's rule coefficients are calculated as

$$\begin{cases} k_{eq} = N_{Geq} \sqrt[n]{\left(\prod_{i=1}^n k_i^{N_{Gi}} \right)} \\ p_{eq} = \frac{\sum_{i=1}^n p_i N_{Gi}}{N_{Geq}} \end{cases} \quad (14)$$

where

$$N_{Geq} = \sum_{i=1}^n N_{Gi}. \quad (15)$$

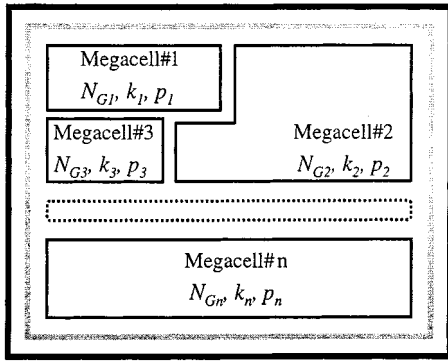


Fig. 7. System-on-a-chip with n different megacells and $N_{G_{cq}}, k_{cq}, p_{cq}$.

Fig. 8 illustrates experimental results of two real chips that mainly consist of two distinct megacells. Megacell#1 is the random logic part of the design and megacell#2 is the memory. The software partitioning program receives the netlist file that contains all connectivity data in a hierarchical form, as input. The macrocells in the netlist file are selected from the blocks that are already defined by the designer. Then a list of macrocells with number of pins and number of gates is constructed. The final data points are generated from the average points of the raw data. In the graphs of Fig. 8, the short dash lines and the long dash lines are the Rent's curves for memory blocks and random logic blocks, respectively. The solid line is the equivalent Rent's rule based on (14) and (15), and circles are real data derived from the netlist files. Design A is a part of an ASIC chip with 37% on-chip SRAM and design B is a color map design with 90% on-chip memory. As shown, the composite Rent's rule successfully describes a heterogeneous collection of megacells.

B. Derivation of Netlist Information

Using the heterogeneous Rent's rule, the number of nets between megacells is computed. For instance, suppose there is a block of two megacells shown in Fig. 9(a), where T_1 and T_2 represent the number of terminals of megacell#1 and megacell#2 respectively. Using the Venn diagram of Fig. 9(b) and de Morgan's law of set theory, it can be proven that

$$T_{\text{Ext}(1,2)} = T_1 + T_2 - T_{\text{Int}(1,2)}. \quad (16)$$

Here, $T_{\text{Int}(1,2)}$ is the number of internal terminals that are shared between the two megacells and $T_{\text{Ext}(1,2)}$ is the number of external terminals of the whole collection of gates, which is calculated by heterogeneous Rent's rule as

$$T_{\text{Ext}(1,2)} = k_{1,2}(N_1 + N_2)^{p_{1,2}} \quad (17)$$

where N_1 and N_2 are the number of gates in megacell#1 and megacell#2, respectively, and $k_{1,2}$ and $p_{1,2}$ are the heterogeneous Rent's parameters given by

$$\begin{cases} k_{1,2} = (k_1^{N_1} \cdot k_2^{N_2})^{\frac{1}{N_1+N_2}} \\ p_{1,2} = \frac{p_1 N_1 + p_2 N_2}{N_1 + N_2}. \end{cases} \quad (18)$$

Equation (16) is illustrated by examining the number of pins of Fig. 9(a). Equations (17) and (18) can also be validated by

considering Rent's rule in a homogeneous system. Substituting Rent's rule in (16) gives

$$k_{1,2}(N_1 + N_2)^{p_{1,2}} = k_1 N_1^{p_1} + k_2 N_2^{p_2} - T_{\text{Int}(1,2)} \quad (19)$$

where k_1, p_1, k_2, p_2 , are the Rent's rule parameter for megacell#1 and megacell#2, respectively, and $k_{1,2}$ and $p_{1,2}$ are the heterogeneous Rent's parameters defined in (18).

Since there are only two megacells in the block, all shared terminals are used for two terminal nets. Note that in this study, a multi-terminal net is defined in the global level where the connections of the terminals inside a megacell are not of concern. Thus, the number of two-terminal nets $N_{\text{net}}(2)$ is given by

$$N_{\text{net}}(2) = \frac{T_{\text{Int}(1,2)}}{2}. \quad (20)$$

Using (20) for all combinations of two megacells in the whole system gives the total number of two-terminal nets (fan-out of 1).

Similarly, in a block of three megacells shown in Fig. 10(a), the number of three-terminal nets can be computed. From the Venn diagram in Fig. 10(b), de Morgan's law gives

$$\begin{aligned} T_{\text{Ext}(1,2,3)} &= T_1 + T_2 + T_3 - T_{\text{Int}(1,2)} - T_{\text{Int}(1,3)} \\ &\quad - T_{\text{Int}(2,3)} + T_{\text{Int}(1,2,3)} \end{aligned} \quad (21)$$

where T_1, T_2 , and T_3 are the number of terminals of each megacell, respectively. $T_{\text{Int}(1,2)}, T_{\text{Int}(1,3)}, T_{\text{Int}(2,3)}$, and $T_{\text{Int}(1,2,3)}$ are the number of terminals that are shared between the associated megacells. $T_{\text{Ext}(1,2,3)}$ is the number of terminals of the whole collection, which is computed by heterogeneous Rent's rule as

$$T_{\text{Ext}(1,2,3)} = k_{1,2,3}(N_1 + N_2 + N_3)^{p_{1,2,3}} \quad (22)$$

where N_1, N_2 , and N_3 are the number of gates in megacell#1, megacell#2, and megacell#3, respectively, and $k_{1,2,3}$ and $p_{1,2,3}$ are the heterogeneous Rent's parameters given by

$$\begin{cases} k_{1,2,3} = (k_1^{N_1} \cdot k_2^{N_2} \cdot k_3^{N_3})^{\frac{1}{N_1+N_2+N_3}} \\ p_{1,2,3} = \frac{p_1 N_1 + p_2 N_2 + p_3 N_3}{N_1 + N_2 + N_3}. \end{cases} \quad (23)$$

Substituting Rent's rule in (21) gives (24), shown at the bottom of the next page, where $T_{\text{Int}(1,2)}, T_{\text{Int}(1,3)}$, and $T_{\text{Int}(2,3)}$ are derived similarly from (19)

$$\begin{cases} T_{\text{Int}(1,2)} = k_1 N_1^{p_1} + k_2 N_2^{p_2} - k_{1,2}(N_1 + N_2)^{p_{1,2}} \\ T_{\text{Int}(1,3)} = k_1 N_1^{p_1} + k_3 N_3^{p_3} - k_{1,3}(N_1 + N_3)^{p_{1,3}} \\ T_{\text{Int}(2,3)} = k_2 N_2^{p_2} + k_3 N_3^{p_3} - k_{2,3}(N_2 + N_3)^{p_{2,3}}. \end{cases} \quad (25)$$

From (24) and (25) the number of three-terminal nets, $N_{\text{net}}(3)$, is given by

$$N_{\text{net}}(3) = \frac{T_{\text{Int}(1,2,3)}}{3}. \quad (26)$$

Using (26) for all combinations of three megacells in the whole system gives the total number of three-terminal nets (fan-out of 2). Equations (26) and (24) show that the number of three-terminal nets is computed recursively from the number of all possible combinations of two-terminal nets. Similarly, in the general case with N_{Meg} megacells, the number of m -terminal nets is computed recursively by examining all possible combinations of $2, 3, \dots, m$ out of N_{Meg} megacells.

Assuming that $N_{\text{Meg}} > 10$, which is satisfied in current and future microprocessor designs [10], then a closed-form expression for the number of m -terminal nets can be derived [13].

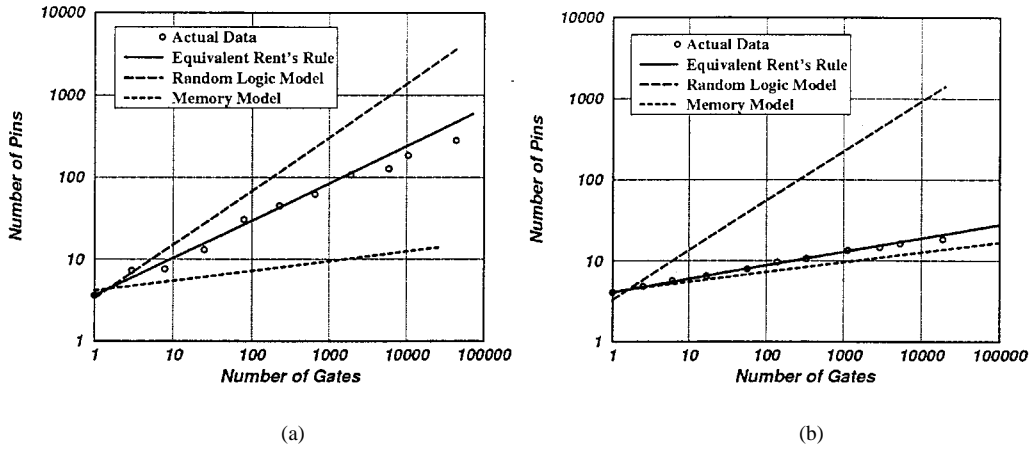


Fig. 8. Experimental results. (a) Data of design A. (b) Data of design B.

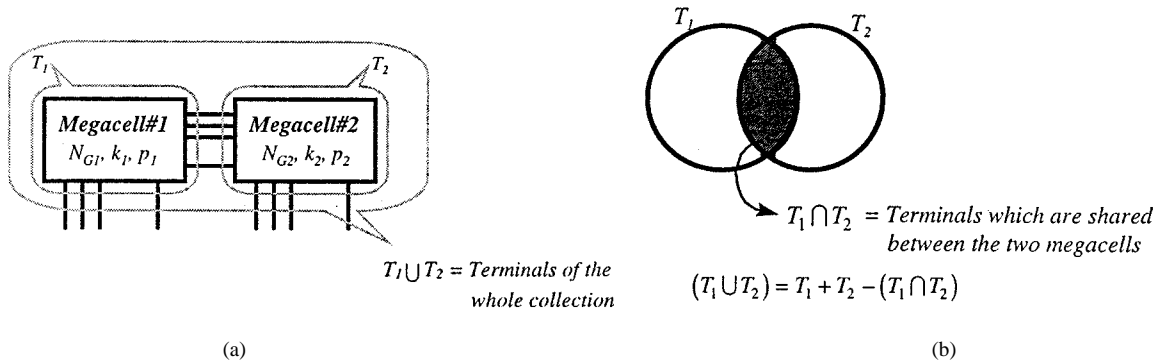


Fig. 9. Example of a collection of two megacells. (a) Block diagram representation. (b) Venn diagram representation.

The approximate expression for the number of m -terminal nets, $N_{\text{net}}(m)$, is

$$N_{\text{net}}(m) \approx \frac{\tilde{K} N_{\text{Meg}} ((m-1)^{\tilde{p}-1} - m^{\tilde{p}-1})}{m} \quad (27)$$

where \tilde{k} and \tilde{p} are the equivalent megacell Rent's rule parameters that are given by

$$\begin{cases} \tilde{k} = N_{\text{Meg}} \sqrt{\left(\prod_{i=1}^{N_{\text{Meg}}} k_i N_i^{p_i} \right)} \\ \tilde{p} = \frac{\sum_{i=1}^{N_{\text{Meg}}} p_i N_i}{N_{\text{Meg}}} \end{cases} \quad (28)$$

Note that the underlying assumption for derivation of (28) is that the heterogeneous Rent's rule is valid throughout the whole design, from the gate level up to the megacell level. However, since the Rent's parameters at the higher level of hierarchy, defined as region II [4], may not be the same as the Rent's parameters at the lower levels, more accurate netlist information results from equating \tilde{k} and \tilde{p} to the Rent's parameters in the region II if they are available. In the absence of the topology of the global Rent's parameters in region II, (28) gives the first order approximation for the Rent's coefficient and exponent of the system.

III. STOCHASTIC PLACEMENT INFORMATION

The placement problem for a SoC is a key factor for achieving designs with minimum global wire length. Therefore, it is important to note that the global wire length depends on the placement tool's efficiency. In this section, a new model is derived for the placement information which defines the bounding area of the nets.

A. Definition of Placement Efficiency

In order to derive the placement model, a new parameter for placement efficiency η_p is defined. For instance, consider the three cases for a placement of four megacells, as shown in Fig. 11(b). In this example, the megacells must be connected by a four-terminal net. Therefore, the best placement ($\eta_p = 100\%$) of the megacells is right next to each other, as shown in Fig. 11(a). The worst case ($\eta_p = 0\%$) is placement of megacells at the corners of the chip area, as shown in Fig. 11(c).

Fig. 12 shows the linear interpolation of block bounding area versus placement efficiency as defined by Fig. 11. In this figure, η_p is the placement efficiency, \bar{A}_{Meg} is the average area of a megacell, m is the number of megacells which are connected by a net, and N_m is the total number of megacells in the design. For

$$\begin{aligned} & k_{1,2,3} (N_1 + N_2 + N_3)^{p_{1,2,3}} \\ & = k_1 N_1^{p_1} + k_2 N_2^{p_2} + k_3 N_3^{p_3} - T_{\text{Int}(1,2)} - T_{\text{Int}(1,3)} - T_{\text{Int}(2,3)} + T_{\text{Int}(1,2,3)} \end{aligned} \quad (24)$$

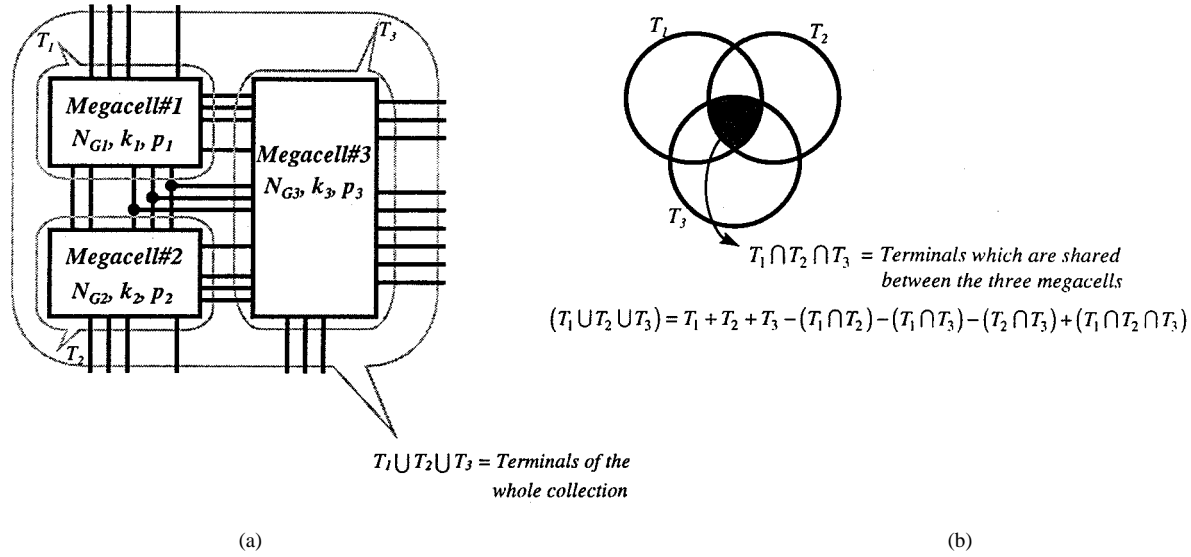


Fig. 10. Example of a collection of three megacells. (a) Block diagram representation. (b) Venn diagram representation.

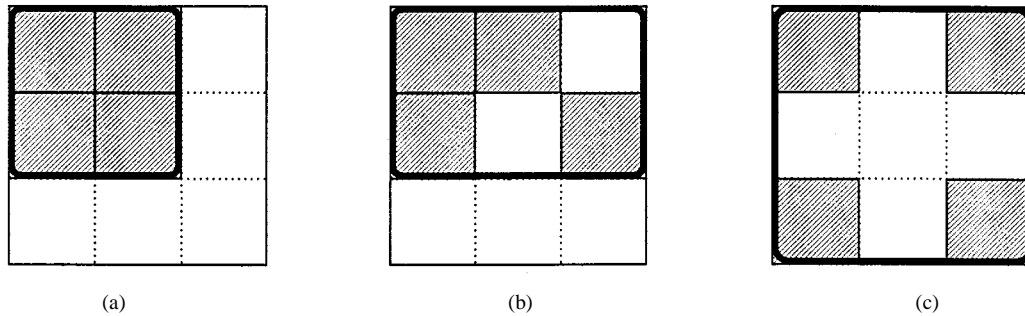


Fig. 11. Placement efficiency model. (a) 100% placement efficiency. (b) 60% placement efficiency. (c) 0% placement efficiency.

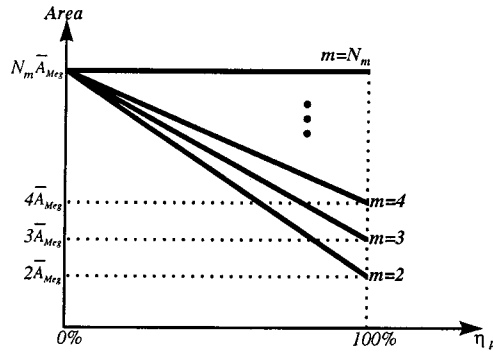


Fig. 12. Linear interpolation of block bounding area versus placement efficiency.

the case of $\eta_p = 100\%$, the bounding area of the blocks is equal to the total area of the megacells in a net which, on average, is $m\bar{A}_{\text{Meg}}$. For the case of $\eta_p = 0\%$, the block bounding area is equal to the chip size ($N_m \cdot \bar{A}_{\text{Meg}}$) regardless of the number of megacells. In the worst case, related blocks can be placed at the corners of chip at the furthest allowable distance. The linear interpolation shown in Fig. 12 can be modeled as

$$\eta_p = \frac{1 - \frac{\text{Block Bounding Area}}{\text{Total Chip Area}}}{1 - \frac{m}{N_m}} \quad (29)$$

where m is the number of megacells which are connected by the net and N_m is the total number of megacells in the design.

Using (29), the placement efficiencies for the three cases, (a), (b), and (c), in Fig. 11 are 100%, 60%, and 0%, respectively.

The placement efficiency depends on CAD tools and it is computed by examining the floor plan results from the auto-placer tool over the entire netlist. Therefore, the average placement efficiency of the entire design is computed by averaging from (29)

$$\bar{\eta}_p = \frac{1}{N_{\text{net}}} \sum_{i \in \text{Entire Netlist}} \frac{1 - \frac{\text{Block Bounding Area}}{\text{Total Chip Area}}}{1 - \frac{m(i)}{N_m}} \quad (30)$$

where N_{net} is the total number of nets in the design. An example of computing the average placement efficiency is contained in Section III-B.

Also from (29), the expression for computing the block bounding area is

$$\text{Block Bounding Area} = \bar{A}_{\text{Meg}}[m\eta_p + N_m(1 - \eta_p)]. \quad (31)$$

Therefore, the bounding area dimension can be computed as

$$\hat{a} = \hat{b} = \sqrt{\bar{A}_{\text{Meg}}[m\eta_p + N_m(1 - \eta_p)]} \quad (32)$$

where \hat{a} and \hat{b} are the block bounding dimensions of m megacells which are connected by a net. Furthermore, the net bounding area is computed by assuming random placement of the terminals of the net in the block bounding area. Fig. 13 shows an example of a net with nine terminals which are placed randomly (with uniform distribution) all over the block

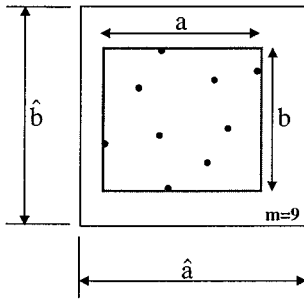


Fig. 13. Block bounding area and net bounding area assuming random placement of terminals.

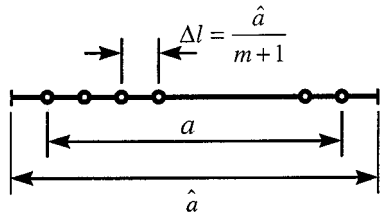


Fig. 14. Distribution of image of terminals in the x axis assuming uniform probability density function.

bounding area \hat{a} and \hat{b} . In this figure, (a) and (b) , which represent the maximum spreading of the terminals, give the net bounding area.

The complete probability density function (pdf) of the net bounding area versus block bounding area has been simulated by using the random walk technique which is described in Section IV. Although there is no analytical closed-form equation for the complete probability density function of net bounding area in general, the average of the pdf can be calculated by a simple closed form-equation.

In order to derive this closed-form equation, first consider the projection of the terminals in Fig. 13 onto the horizontal axis, as shown in Fig. 14. The distance between two adjacent projection points, on average, is given by

$$\Delta l = \frac{\hat{a}}{m+1}. \quad (33)$$

Since there are $m-1$ pieces of Δl , the average net bounding area on the horizontal axis is

$$a = (m-1) \cdot \Delta l = \frac{m-1}{m+1} \cdot \hat{a}. \quad (34)$$

Similarly, on the vertical axis it can be shown that

$$b = \frac{m-1}{m+1} \cdot \hat{b} \quad (35)$$

where a and b are the net bounding area dimensions. Using (32), (34), and (35), the average net bounding area versus the number of terminals of a net(m) is computed.

B. An Example of Placement Efficiency

Placement efficiency is a parameter that defines a CAD tool's capability to place megacells such that it requires the minimum wire-length for the global wiring networks. A perfect placement with 100% placement efficiency means that all connected megacells are placed in the nearest neighborhood of each other. Since the placement efficiency is a criterion to reflect the compactness

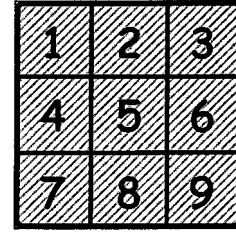


Fig. 15. Example of calculation of placement efficiency.

of a design, it can also be used as a cost function for placement optimization algorithms in CAD tools. Therefore, in this part an example of computing the placement efficiency for a simple case is investigated.

Suppose that there is a chip with nine megacells, as shown in Fig. 15. Each megacell is assumed to occupy one unit area. Hence, the chip area is nine units. For the given netlist shown in Table I, the block bounding area of each combination of connected megacells can be calculated for the case of placement depicted in Fig. 15. Using (29), the placement efficiency of each net is computed. The average placement efficiency of the entire netlist is computed by averaging the placement efficiency from (30), which gives

$$\begin{aligned} \bar{\eta}_p &= \frac{1}{N} \sum_{\substack{\text{net } i \in \text{Entire} \\ \text{Netlist}}} \frac{1 - \frac{\text{Block Bounding Area}}{\text{Total Chip Area}}}{1 - \frac{m(i)}{N_m}} \\ &= \frac{1}{94} \times 59 = 63\%. \end{aligned} \quad (36)$$

Similarly, the average placement efficiency can be computed for a typical design created by any CAD tool under test.

IV. STOCHASTIC ROUTING INFORMATION

It is well-known that the routing problem is an NP-hard problem [14]. This means that, the exact solution for the general case is impossible or hard to achieve. Several methods have been introduced in CAD tools such as the MRST [15], Rip-up and Reroute [16] and Iterative Deletion [17]. In this paper, we use the MRST to derive a model for routing information, since it is the most popular method to achieve minimum wire length for global interconnects. There are several models for MRST net-length estimation such as the work of Chung and Hwang [18], Cheng [19], and Beardwood *et al.* [20]. Although these models give a good estimation for the length of the multi-terminal nets with large number of terminals, they are not accurate enough for two- or three-terminal nets. Since most of the nets in a design are two- or three-terminal nets (refer to netlist information model), an accurate model for a wide range of number of terminals is required in this work.

Fig. 16(a) shows an example of a six-terminal net based on MRST. A rule of thumb to calculate the net-length is known as the half perimeter model [21] that approximates the net length by the half perimeter of the net bounding area. For example, in the net shown in Fig. 16, the length is estimated as

$$L_{HP} = a + b \quad (37)$$

where a and b are the net bounding area dimensions and L_{HP} is the estimated net length using the half perimeter model. It can

TABLE I
AN EXAMPLE OF COMPUTING THE PLACEMENT EFFICIENCY

m	Connected Megacells	Number of nets	Block Bounding Area [Unit area]	$1 - \frac{\text{Block Bounding Area}}{\text{Total Chip Area}}$	$1 - \frac{m}{N_m}$	$\eta_p(i)$
2	1,2	10	2	$1 - 2/9 = 7/9$	$7/9$	100%
2	1,6	14	6	$1 - 6/9 = 1/3$	$7/9$	43%
2	2,5	12	2	$1 - 2/9 = 7/9$	$7/9$	100%
2	4,8	18	4	$1 - 4/9 = 5/9$	$7/9$	71%
2	3,7	9	9	$1 - 9/9 = 0$	$7/9$	0%
3	1,2,5	7	4	$1 - 4/9 = 5/9$	$2/3$	83%
3	2,7,8	5	6	$1 - 6/9 = 1/3$	$2/3$	50%
3	4,5,7	8	4	$1 - 4/9 = 5/9$	$2/3$	83%
4	6,7,8,9	3	6	$1 - 6/9 = 1/3$	$5/9$	60%
4	1,3,5,8	4	9	$1 - 9/9 = 0$	$5/9$	0%
4	5,7,8,9	2	6	$1 - 6/9 = 1/3$	$5/9$	60%
6	1,2,4,5,6,7	1	9	$1 - 9/9 = 0$	$1/3$	0%
8	1,2,3,4,5,6,7,8	1	9	$1 - 9/9 = 0$	$1/9$	0%

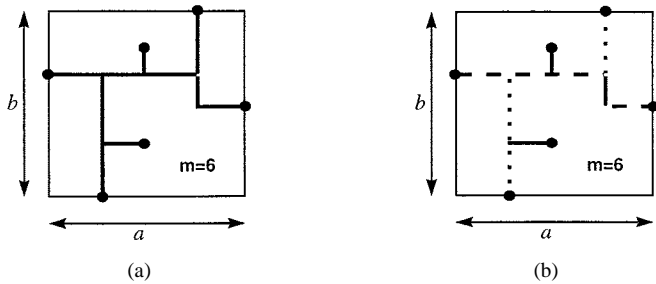


Fig. 16. Example of a six-terminal net, based on MRST. (a) The complete net structure using MRST. (b) The segments representing the net bounding area dimensions.

be easily shown that the half perimeter model always underestimates the net length for m -terminal nets when $m > 3$. Suppose the net in Fig. 16(a) is divided into segments as shown in Fig. 16(b). The total sum of the length of dashed line and dotted line segments in the net bounding area is equal to the length of a and b , respectively. Therefore, the actual wire length of the MRST net is the half perimeter length $(a + b)$ plus the solid line segments

$$L_{\text{MRST}} = \delta L + (a + b) \quad (38)$$

where δL represents the length of the additional segments which is a function of the number of terminals and the bounding area dimensions. Also δL depends on the placement of the terminals.

Here we assume the terminals are placed randomly with uniform probability density function over the entire bounding area. Then, the probability density function of net length can be computed by the random walk technique. An example of the net-length pdf for the case of a 30-terminal net over the block bounding area of $10 \times 20 \text{ mm}^2$ is shown in Fig. 17. As shown, the net-length pdf has an average of 61.1 mm and a standard deviation of 3.98 mm.

The random walk simulation has been performed for various numbers of terminals over different bounding area dimensions in order to find a simple and closed-form equation for the average net length of an MRST net. In the simulation the MRST is constructed using a heuristic algorithm shown in [22]. Fig. 18

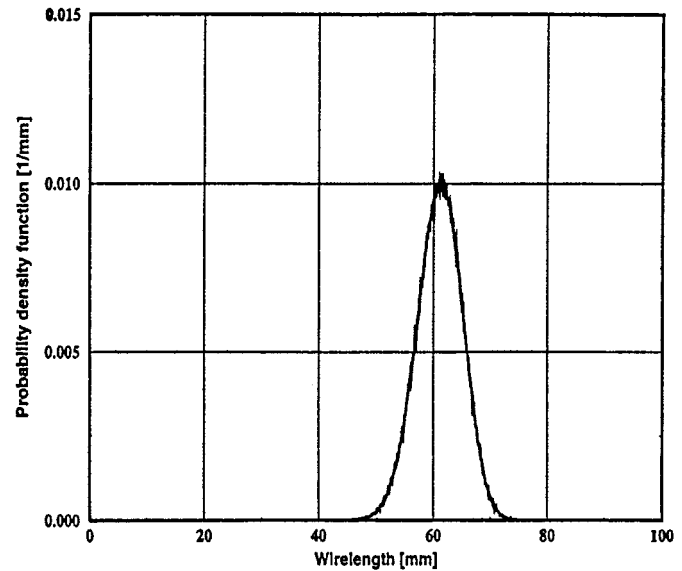


Fig. 17. Example of net-length probability density function.

illustrates the average net length versus the number of terminals of the net for two different bounding area dimensions of $10 \times 10 \text{ mm}^2$ and $10 \times 20 \text{ mm}^2$.

In order to find a closed-form expression for the average MRST net-length, suppose that there is an m -terminal MRST net bounded with a square of size d ($a = b = d$). The net-length is proportional to the d , because scaling the bounding dimension would scale the net-length with the same weight of scaling. Thus the net length can be represented by

$$L_{\text{MRST}} = f(m) \cdot d \quad (39)$$

where f is a function of the number of net terminals, m , and d is the net bounding area dimension, and L_{MRST} is the net-length of the MRST net. Now suppose that the area is divided into four equal pieces with dimensions of $d/2$ by $d/2$, as shown in Fig. 19. Assuming uniform distribution of terminals, there are $m/4$ terminals in each piece, which means that the length of the net in each piece is $L'_{\text{MRST}} = f(m/4) \cdot (d/2)$. For a very large value of m , the length of broken segments, due to

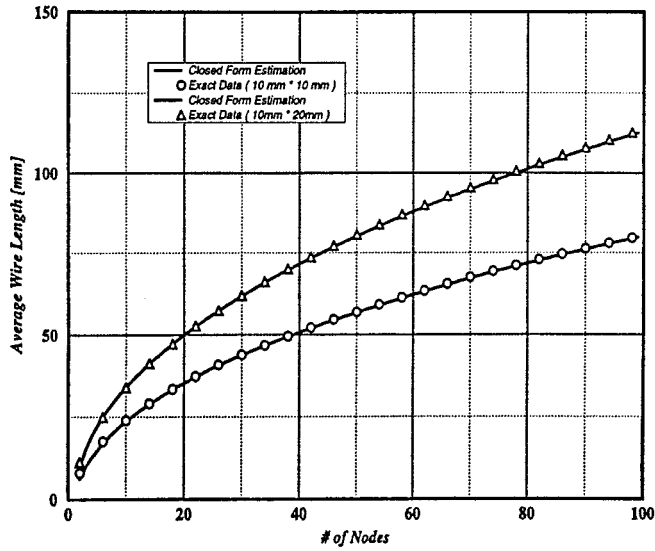


Fig. 18. Average net length versus the number of terminals from (42) compared to exact data from computer simulations.

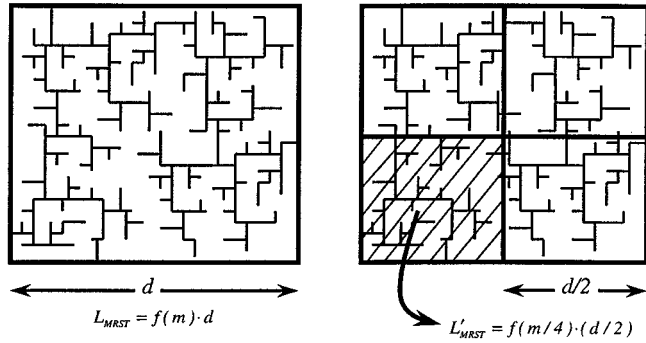


Fig. 19. Derivation of the form of MRST net-length function based on net partitioning.

this dividing, can be ignored compare to the total net length. Therefore, $L_{MRST} = 4L'_{MRST}$, which gives

$$\begin{aligned} f(m) \cdot d &= 4 \cdot f(m/4) \cdot (d/2) \\ f(m)/2 &= f(m/4). \end{aligned} \quad (40)$$

The only solution of (40) is $f(m) = \alpha \cdot m^\gamma$, where $\gamma = 0.5$ precisely, and α can be any number. In the general case when m is small, by considering the length of broken segments, the general solution of the same equation as described above is

$$f(m) = \alpha \cdot m^\gamma - \beta \quad (41)$$

where α, β , and γ are computed by curve fitting.

For the case of a rectangular (nonsquare) bounding area, the simulation results shows that for the case of $a \ll b$, the value of δL in (38) is proportional to a . Similarly for the case of $a \gg b$, the value of δL is proportional to b . The only symmetric function that gives the best fit to the simulations data is $ab/(a+b)$. Therefore, the form of the equation for the average net-length of an MRST net is given by

$$L_{av} \approx (\alpha \cdot m^\gamma - \beta) \frac{a \cdot b}{a + b} + (a + b) \quad (42)$$

where α, β , and γ are the fitting parameters which have been computed as $\alpha \approx 1.1, \beta \approx 2.0$, and $\gamma \approx 0.5$, the first term, $(\alpha \cdot m^\gamma - \beta)(a \cdot b / (a + b))$, is a representation of δL in (38), m is the number of terminals of the net, and a and b are the net bounding area dimensions.

V. COMPLETE STOCHASTIC GLOBAL NET-LENGTH DISTRIBUTION

The complete global net-length distribution is derived by combining all three distinct information bases: netlist, placement, and routing.

The netlist information calculates the number of nets for each fan-out by using heterogeneous Rent's rule. The placement information gives the pdf of the net bounding area dimensions that are computed by the random walk technique. Using the routing information, the net bounding area dimensions are translated to the net length, assuming MRST construction for the net.

The complete global net-length distribution is the summation of net-length pdf multiplied by the corresponding number of nets for all fan-outs. Equations (32), (34), (35), and (42) can be used to compute the average of the net-length pdf for each fan-out.

A real RISC microprocessor [23] has been modeled as an example to verify the new model derived here. The chip size is $16.6 \times 17.8 \text{ mm}^2$ with 20 different megacells. Table II shows the Rent's parameters and the number of gates in the megacells. The Rent's parameters are computed based on some extracted data from actual designs, as shown in [12]. Moreover, the tabulated Rent's parameters for different structures such as random logic, memory, data path, are found in [24]. Based on the type of the megacells in Table II, Rent's rule parameters are selected. For instance, the Rent exponents for memory, data path and random logic are 0.2, 0.47, and 0.6, respectively.

Equations (32), (34), (35), and (42) give the average net length for each fan-out which is depicted in Table III, assuming a placement efficiency of 80%. In the absence of detailed placement data to compute the placement efficiency in this example, the value of 80% is selected for the placement efficiency because it gives the best fit to the data. Note that for the other circuits that are laid out with the same placement program the placement efficiency can be approximated with the same value of 80%. However, the value of 80% for placement efficiency is only for this particular placement program and it can be different for other placement tools.

The second column of Table III gives the total number of nets for the fan-out specified in column one. Column three gives the average net bounding area from the placement information equation and the fourth column gives the average net length from the routing information using the average net bounding computed in the second column. The total net length is computed by multiplying the average net length by the number of nets for each fan-out. Table III shows that the total number of global nets is 6381, the average global net length is 9.11 mm, and the total global net length is 58.1 m. Note that, based on [23], the total number of global nets is about 6000, which supports the prediction of the netlist information presented here.

TABLE II
RENT'S PARAMETERS OF MEGACELLS

Megacell's Name	k	N	p	Megacell's Name	k	N	p
Instruction Cache	4.12	380,000	0.20	Instr. Fetch Address	3.20	16,500	0.60
Instruction Cache Tags	3.80	18,000	0.47	Instr. Fetch Data Path	3.20	13,800	0.60
Data Cache	4.12	350,000	0.20	Instr. Fetch Control	3.20	9,500	0.60
Data Cache Tags	3.80	25,500	0.47	Address Queue	3.20	22,000	0.60
TLB	3.80	22,400	0.35	Inst. Decode & Reg. Ren.	3.20	45,300	0.60
Secondary Cache Ctrl.	3.20	15,700	0.60	Integer Data Path	3.20	43,800	0.60
External Interface	3.20	18,400	0.60	Integer Queue	3.20	19,700	0.60
Sys. Interface Buffers	3.20	22,600	0.60	Floating Point Data Path	3.20	32,600	0.60
Free List	3.20	9,800	0.60	Floating Point Queue	3.20	51,000	0.60
Graduation unit	3.20	26,300	0.60	Floating Point Multiplier	3.20	19,300	0.60

TABLE III
NETLIST, PLACEMENT, AND ROUTING INFORMATION

Global Fan out	Netlist Info. Total No. of Nets	Placement Info. Average Net Bounding Area	Routing Info. Average Net Length	Total Net Length
1	3632	3.03×3.03 mm ²	5.173 mm	18788 mm
2	1184	4.86×4.86 mm ²	9.068 mm	10736 mm
3	561	6.18×6.18 mm ²	12.36 mm	6933.9 mm
4	318	7.24×7.24 mm ²	15.33 mm	4874.9 mm
5	200	8.14×8.14 mm ²	18.10 mm	3620.0 mm
6	134	8.93×8.93 mm ²	20.74 mm	2779.1 mm
7	94	9.64×9.64 mm ²	23.27 mm	2187.3 mm
8	68	10.3×10.3 mm ²	25.75 mm	1751.0 mm
9	50	10.9×10.9 mm ²	28.13 mm	1406.5 mm
10	38	11.4×11.4 mm ²	30.30 mm	1151.4 mm
11	28	12.0×12.0 mm ²	32.78 mm	917.96 mm
12	22	12.5×12.5 mm ²	35.03 mm	770.66 mm
13	16	13.0×13.0 mm ²	37.32 mm	597.12 mm
14	12	13.4×13.4 mm ²	39.34 mm	527.15 mm
15	9	13.9×13.9 mm ²	41.70 mm	375.30 mm
16	6	14.3×14.3 mm ²	43.78 mm	262.68 mm
17	4	14.7×14.7 mm ²	45.88 mm	183.52 mm
18	3	15.1×15.1 mm ²	48.00 mm	144.00 mm
19	2	15.5×15.5 mm ²	50.15 mm	100.30 mm
Total	6381	-	-	58106.8 mm

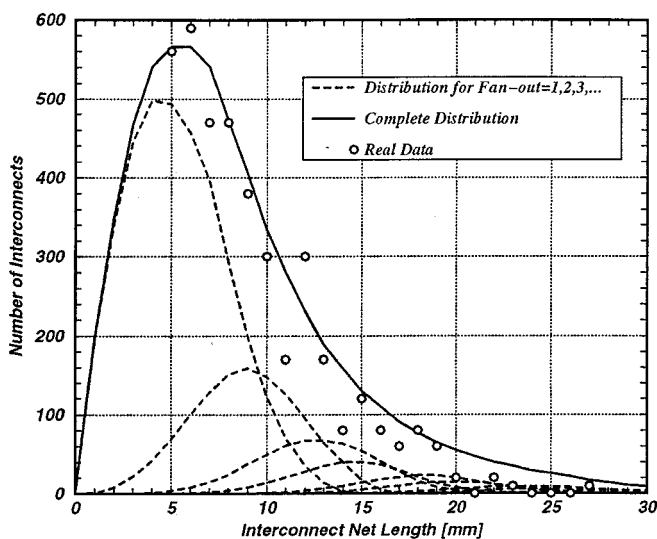


Fig. 20. Complete global net-length distribution compared to real data.

The complete estimation method of global net-length distribution based on the three models of netlist, placement and routing has been implemented in a C program called “GLobal

Interconnect Distribution Estimator” (GLIDE). In this program, the netlist information is computed based on the heterogeneous Rent’s rule. Then, the placement and routing information for every fan-out are obtained from the random walk technique described in Section IV.

The complete model of global net-length distribution used in GLIDE is verified through comparison with actual data. Fig. 20 shows the comparison of the predicted global net-length distribution using GLIDE and very basic parameters of Table II to the actual data taken from [23]. As seen in Fig. 20, the predicted global net-length distribution describes a real wiring histogram with a good accuracy.

VI. CONCLUSION

A priori global net-length distribution for a heterogeneous SoC is derived based on the three stochastic models for *netlist*, *placement*, and *routing* information. The netlist information determines the number of nets for each fan-out by using the heterogeneous Rent’s rule. The placement information gives the probability density function of the net bounding area dimensions that are computed by the random walk technique. Using the routing information, the net bounding area dimensions are translated to the net length, assuming MRST construction for the net. The complete global net-length distribution discussed here has been implemented in a C program called “GLobal Interconnect Distribution Estimator” (GLIDE). The new net-length distribution model used in GLIDE, is verified through comparison with actual data from a commercial RISC microprocessor.

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