IGBT Open-Circuit Fault Diagnosis in a Quasi-Z-Source Inverter

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Abstract—In this paper, a fast and practical method is proposed for open-circuit (OC) fault diagnosis (FD) in a three-phase quasi-Z-source inverter (q-ZSI). Compared to the existing fast OC FD techniques in three-phase voltage-source inverters (VSIs), this method is more cost-effective since no ultra-fast processor or high-speed measurement is required. Additionally, the method is independent of the load condition. The proposed method is only applicable to Z-source family inverters and is based on observing the effect of shoot-through (ST) intervals on the system variables during switching periods. The proposed algorithm includes two consecutive stages: OC detection and fault location identification. When both stages of the OC FD algorithm are done, a redundant leg is activated and utilized instead of the failed leg. The accuracy of the proposed method is confirmed by the experimental results from a low-voltage q-ZSI prototype.

Index Terms—Quasi-Z-Source Inverter, Open-Circuit Fault, Fault Diagnosis Algorithm.

I. INTRODUCTION

To ensure service continuity and increase the reliability of a distributed generation (DG) power system, fault-tolerant (FT) structures have been considered widely in recent literature [1]-[4]. A DG power system includes many parts such as the storage device, the processor unit, the sensors, the input source and the power electronics converter. A failure could occur in any of these parts. According to the study in [5], semiconductor and soldering faults cause approximately 34% of power device failures. However, it is estimated that at least 80% of faults in the converter part are due to semiconductor failures [6].

Power switch faults which are typically caused by high thermal or electrical stress are categorized into two main groups: short-circuit (SC) and open-circuit (OC) faults [7]-[8]. An OC fault (OCF) in a power converter could occur through a switch failure or a driver breakdown. Gate driver breakdown is the main cause of converter failure (53% of the converter faults) and results in permanent IGBT OC [7].

Unlike an SC fault, which usually triggers the SC protection of the system, an OCF can remain undetected for a long time, degrading the power quality in the power system. Problems such as abnormal stress on circuit elements can occur after OCF, causing further damage to the system [7]. As OC faults are prevalent in power device failures, OC FD is a basic step for increasing the reliability of a power system. In non-FT systems, using OC FD techniques prevents extra system damages. In FT systems, it also results in continuous operation after an OC fault. Speed, cost, reliability, and independence of the load condition are the main factors for evaluating an OC FD method. The approaches for OC FD are either current-based or voltage-based [9]-[10] and each type has different strategies. Current-based methods have been considered widely in the literature [11]-[16]. In [10], a thorough review of these methods is presented. In most of these methods, the measured three-phase currents are mathematically analyzed to recognize OCF. Usually, no extra hardware is required in current-based methods, making them cost-effective. Low speed, high complexity, limitation for multiple faults detection and malfunction in small loads are the drawbacks of these approaches [17]. In Table I, some common OC FD methods are compared. Park’s vector approach presented in [18] (with specification as shown in Table I), is a well-known FD method. The main drawback is that the detection algorithm is too complex to fit in a processor designed for power electronics application. The normalized DC current method in [19] is based on Park’s vector approach which is not load-dependent (unlike Park’s vector method). This method is not efficient when closed-loop control is implemented. In the modified normalized DC current method, this problem is nearly solved [19]. The slope calculated from $i_d$ and $i_q$ samples (the current components of Park’s vector), is used for FD in the slope method [20], in which FD is load-dependent and rather slow. In the AC current instantaneous frequency method, OCF is detected from the calculation of the current space vector frequency [20]. The location of the OCF is not recognized by this FD procedure. In [21] another cost-effective and relatively fast current-based alternative is proposed which is also robust to load variation. In this method, the difference between the reference and the output current is calculated. But this approach cannot be used in a system with an open-loop control. A similar technique, using the system mathematical model is proposed in [22] for motor drive application. However, its implementation is rather complex and demands high mathematical calculations. In addition, extra measurement (phase voltage sensing) is needed for the FD procedure. Another model-based method is presented in [23]. Although it is cost-effective as no extra hardware is required, the accuracy of the FD is strongly dependent on the pre-assumed values for the system parameters. In practice, the method is inefficient.
The need for high.

In Table I, the specification of some voltage-based FD methods are also depicted. In “actual and reference quantity comparison” the fault is recognized by comparing the reference and the measured phase voltage values [24]. The method is much faster than current-based methods, but it has a costly implementation. Sensing the lower switch voltage is another fast voltage-based FD strategy [8]. It uses op-amp/flip-flop auxiliary circuits for FD, increasing the complexity of the system. In [7], an OC FD is proposed based on three-phase current, phase voltage, and DC link voltage measurements. The method is fast but the many variables involved in FD could make the method sensitive to noise. An ultra-fast FPGA-based approach is proposed in [25]. It is not possible to implement this technique in a usual DSP/microcontroller processor used in power electronics applications. The need for high-bandwidth voltage measurement is another drawback of this method, leading to a cost increase. In addition, the assumption on delays in the response time of the circuit elements is required. This may affect the accuracy of the FD in practice. In [26] another voltage-based method is proposed. It is based on the comparison of the lower switch voltage and the added photocoupler output. This approach is low-cost and fast, but it is dependent on the characteristics of the devices which can change by thermal conditions or by aging.

In summary, in comparison to current-based FD methods, voltage-based methods are much faster and have higher immunity to false alarms. However, voltage-based methods usually require additional measurement and extra hardware leading to higher cost and complexity [24]-[26].

The three-phase q-ZSI shown in Fig. 1, is a beneficial structure for DG especially in photovoltaic (PV) applications [27]-[29]. In addition to the single-stage buck-boost characteristic, q-ZSI can absorb constant power from the input source. Compared to the traditional Z-source inverter (ZSI) the voltage on capacitor \( C_2 \) (Fig. 1) is much less than that on \( C_1 \) [30], leading to reduced passive component rating and lower manufacturing cost. In [31], modeling and controller design of q-ZSI is discussed. In [31]-[33], q-ZSI with battery storage for hybrid PV application is presented.

To have a reliable PV power system, applying FT strategies to q-ZSI has some advantages compared to the traditional double-stage PV converters. As mentioned, a significant portion of semiconductor failures is due to switch OC faults [7]. To cover OC faults at both AC and DC sides of a double-stage PV converter, two separate FT strategies (for AC and DC stages) are required. FT topologies for DC/DC stage in PV systems are presented in [34]-[35]. Due to a single-stage structure and fewer semiconductor elements in q-ZSI, implementing FT strategies in q-ZSI has lower cost and higher reliability.

FD is the main step in FT systems. In this paper, a novel voltage-based OC FD technique is proposed for three-phase q-ZSI. The proposed method is much faster than most of the approaches shown in Table I. This method is able to recognize OC faults in just a few switching cycles. Despite the fast FD method in [25], no high-speed processor or ultra-fast measurement is required. In comparison to the existing techniques, the proposed method has a simpler implementation. In addition, the CPU of the processor is not involved in the FD procedure during normal work conditions. To implement the proposed method, only a low-cost auxiliary circuit (including a comparator and a resistive divider) is added to the system. Therefore, the cost of the system does not change significantly (unlike most voltage-based approaches [8], [24]-[26]). In addition, this method is independent of the load condition since

### Table I

<table>
<thead>
<tr>
<th>Method</th>
<th>FD Time (msec)</th>
<th>Load Dependency</th>
<th>Implementation complexity</th>
<th>Required variables</th>
<th>Extra Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Park’s Vector Method [18]</td>
<td>20</td>
<td>High</td>
<td>Medium</td>
<td>3-phase currents</td>
<td>No</td>
</tr>
<tr>
<td>Normalized DC Current Method [19]</td>
<td>18.4</td>
<td>High</td>
<td>Low</td>
<td>3-phase currents</td>
<td>No</td>
</tr>
<tr>
<td>Modified Normalized DC Current Method [19]</td>
<td>18.4</td>
<td>Low</td>
<td>Low</td>
<td>3-phase currents</td>
<td>No</td>
</tr>
<tr>
<td>Slope Method [20]</td>
<td>38.3</td>
<td>High</td>
<td>Low</td>
<td>3-phase currents</td>
<td>No</td>
</tr>
<tr>
<td>AC Current Instantaneous Frequency Method [20]</td>
<td>20</td>
<td>Medium</td>
<td>Low</td>
<td>3-phase currents</td>
<td>No</td>
</tr>
<tr>
<td>The Reference Current Errors Method [21]</td>
<td>13</td>
<td>Low</td>
<td>Low</td>
<td>3-phase currents</td>
<td>No</td>
</tr>
<tr>
<td>Observer-Based Method [22]</td>
<td>19</td>
<td>Low</td>
<td>Medium</td>
<td>3-phase currents/voltages</td>
<td>Medium</td>
</tr>
<tr>
<td>Actual and Reference Quantity Comparison [24]</td>
<td>5</td>
<td>Low</td>
<td>High phase, neutral and pole voltages</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>Lower Switches Voltage Observation [8]</td>
<td>2.7</td>
<td>Low</td>
<td>Medium</td>
<td>lower switches voltage</td>
<td>High</td>
</tr>
<tr>
<td>Instant Voltage Error [7]</td>
<td>2.5</td>
<td>Low</td>
<td>Medium</td>
<td>3-phase currents/voltages</td>
<td>Low</td>
</tr>
<tr>
<td>Real-Time FPGA-Based [25]</td>
<td>0.01</td>
<td>Low</td>
<td>High</td>
<td>pole voltages/device delays</td>
<td>High</td>
</tr>
<tr>
<td>Switching Function Model-Based [26]</td>
<td>0.01-10</td>
<td>Low</td>
<td>Medium</td>
<td>lower switches voltage</td>
<td>Medium</td>
</tr>
</tbody>
</table>

![Fig. 1. Three-phase q-ZSI main topology.](image-url)
the detection of OC

\[ D \times T_{SH} \]

\[ D \times T_{SH} = S \)

\[ V_{leg} \]

\[ \theta = \omega m t \]

Fig. 2. The typical waveform across the leg terminals voltage.

Fig. 3. Scalar implementation of SVM method in q-ZSI [37].

It is voltage-based. The FD procedure is based on observing the SH intervals effect on the voltage across the legs (\( v_{leg} \)) in Fig. 1. Therefore, it is not applicable in the traditional VSIs. In the proposed FD algorithm, the detection of OCF and identifying the failed leg are implemented in two consecutive stages. In the first stage, the algorithm confirms an OC

\[ v_{leg} = \begin{cases} 
0 & \text{SH mode} \\
\frac{v_{c1} + v_{c2}}{} & \text{non SH mode} 
\end{cases} \]  

(1)


\[ v_{c1} \] and \( v_{c2} \) are the voltages across \( C_1 \) and \( C_2 \) shown in Fig. 1. As a control strategy in q-ZSI, the peak value of the leg terminals voltage (\( v_{c1} + v_{c2} \)) is regulated through SH duration adjustment, where:

\[ v_{c1} + v_{c2} \approx V_B = V_{in} \times B \]  

(2)

\[ B = \frac{1}{1 - 2D_{sh}} \]  

(3)

B in (2)-(3) denotes the “boost factor” of the q-ZSI and \( D_{sh} \) is the relative SH state duration in a switching period. \( V_B \) denotes the peak value of the \( v_{leg} \). When the source voltage is dropped, \( D_{sh} \) is increased and the leg terminals peak voltage is kept nearly constant [36].

For the scalar implementation of SVM vectors in a q-ZSI, SH duration is divided into six separate intervals which are located between the main SVM vectors [37]. In Fig. 3, the arrangement of SH and the main SVM states are shown for \( A_1 \) sector. In Fig. 4, SVM sectors in \( a\beta \) plane are depicted [37]. \( T_a \) and \( T_b \) in Fig. 3 are the durations of the first and the second active vectors of SVM method respectively. \( T_{sh} \) is SH state length; \( T_0 \) and \( T_7 \) denote the duration of zero state in which the three lower and the three upper switches are turned on. The calculation of the compare signals values in q-ZSI (shown by \( T_{min} \), \( T_{max} \) and \( T_{mid} \) in Fig. 3) is presented in [37]. The filled rectangles in Fig. 3 represent SH states; where \( SH_i (i = a, b, c) \) identifies the short-circuit leg in each SH state. As it is seen, during each SH state only one leg becomes short-circuit. For example, the first SH in Fig. 3 is through leg “a”. The switching states are symmetric to the center of the switching period.

II. AN INTRODUCTION TO QUASI-Z-SOURCE INVERTER

q-ZSI shown in Fig. 1 has two operating modes [36]:

1) Inverter Mode: In this mode, q-ZSI operates similarly to a classic voltage source inverter (VSI). In this mode, the continuous input current flows through the input side diode (\( D \) in Fig. 1).

2) Shoot-through Mode: During this mode, the inverter becomes short-circuit intentionally through any phase legs. The network diode is turned off via the reverse-bias voltage.

III. OPEN-CIRCUIT ANALYSIS IN QUASI-Z-SOURCE INVERTER

In the most probable OC fault case [7], IGBT is only affected and its antiparallel diode is sound. This fault is also called “open-gate fault”. In this case, only one polarity of the output current is conducted by the freewheeling diode or the sound switch of the leg. In Fig. 5(a), the output currents of the inverter are shown when the upper switch of leg “a” (\( S_{alt} \) in Fig. 1) is OC.
It is also possible that the total leg becomes OC. This fault may happen by the intervention of the protection system [6]. In Fig. 5(b), the output currents are shown for the case that both switches of leg “a” are OC.

After an OCF in a switch, low-frequency harmonics appear in the harmonic content of the qZSI state variables (\(v_{C1}, v_{C2}, i_{L1}, \) and \(i_{L2}\)) as well as the output power. The leg voltage peak value is dropped as the SH state is not implemented by the faulty leg (the boost factor is decreased in practice). For the simulated q-ZSI, the normalized value of “\(v_{C1} + v_{C2}\)” is shown in Fig. 6(a)-(b) in the case of OC in a switch and a leg respectively. In both cases, the peak value of the leg terminals is dropped. \(v_{leg}\) during OCF in a switch is shown in Fig. 7. As shown in Fig. 3 and Fig. 7, in normal work condition, six SH intervals are visible on \(v_{leg}\) during each switching period. During OCF (in both leg and switch cases), the number of SH intervals recognizable from \(v_{leg}\) is decreased to four.

IV. OPEN-CIRCUIT FAULT DIAGNOSIS IN QUASI-Z-SOURCE INVERTER

As it is mentioned, all SH states appear as zero-value intervals on \(v_{leg}\). In this paper, “NFE” is defined as the number of falling edges (FE) in \(v_{leg}\) waveform during half of the switching period. It can be said that when all SH states are implemented properly, NFE is three. During OCF, NFE is reduced to two since the SH state is not implemented by one leg.

Assuming normal work condition in an ideal q-ZSI, \(t_{FEi}\) (\(i = 1,2,3\)) is defined as the falling edge (FE) time at the beginning of its SH state in a switching cycle (shown in Fig. 8). \(t_{FEi}\) values are calculated as:

\[
\begin{align*}
 t_{FE1} &= 0.25(T_{sw} - T_a - T_b - T_{sh}) \\
 t_{FE2} &= t_{FE1} + T_{sh}/6 + 0.5T_a \\
 t_{FE3} &= 0.5T_{sw} - t_{FE1} - T_{sh}/6 \\
 T_a/T_{sw} &= M_c \sin \left( n \frac{\pi}{3} - \theta \right) \\
 T_b/T_{sw} &= M_c \sin \left( \theta - (n - 1) \frac{\pi}{3} \right) \\
 M_c &= \sqrt{3}V_{ref}/V_b
\end{align*}
\]

In (5), \(V_{ref}\) and \(\theta\) are the reference vector amplitude and angle in \(a\beta\) plane; “\(n\)” is the sector number.

Each FE in Fig. 8 (FE1, FE2, and FE3) is implemented through a separate leg. Table II shows the short-circuit leg for each FE moment along SVM sectors. For example, the second FE (FE2) during the third sector \((A_3)\) is implemented through leg “c”.

In practice, FE moments in \(v_{leg}\) occur with a little delay comparing to \(t_{FEi}\) values in (4), mainly because of the IGBTs turning-off delay.
The missed FE is identified using Table II. Considering (6), the peak value of \( v_{leg} \) is scaled down to 3\( V \) at the comparator input. \( V_c \) is set at 1.5\( V \), covering nearly half of the IGBT delay during digitalizing \( v_{leg} \). The digital output from the comparator \( (v_{cap}) \) is transferred to the capture unit. The detected FE moments, \( t_{capj} \) \( (j = 1, 2, 3 \text{ in normal condition and } j = 1, 2 \text{ during OCF}) \) are saved to the capture registers \( (\text{CAP}j) \) as shown in Fig. 10. As mentioned, in practice, the detected FE moments \( (t_{capj}) \) are not exactly equal to the calculated times \( (t_{FEi}) \) because of system delays. A delay margin \( (t_d) \) is considered for each \( t_{capj} \) value to be considered as a correct FE detection. \( t_d \) is selected due to the IGBTs typical turning-off time \( (t_{off}) \). In this paper, \( t_d \) is considered 2\( \mu \text{s} \) which is 2.5 times larger than \( t_{off} \) in the used IGBTs. If the difference between \( t_{capj} \) and \( t_{FEi} \) is less than 2\( \mu \text{s} \), FE detection is confirmed. In Fig. 10, the filled rectangles shows the permitted delay margin.

B. Open-Circuit Fault Diagnosis Algorithm

The OC FD algorithm proposed in this paper is based on examining \( v_{leg} \) and its zero-value intervals; the missed zero–value interval in \( v_{leg} \) identifies the OC leg. Comparing to OC
FD algorithms in traditional VSIs, this method has the advantages of being both fast and cost-effective. With this method, it is possible to detect OCF in a few switching cycles without the need to use an ultra-fast processor or high-speed measurement. In addition, the OC FD is independent of the load condition.

In the proposed OC FD algorithm, OCF detection and the failed leg identification are implemented in two consecutive stages. In the first stage, the algorithm confirms an OCF. Then, the CPU starts handling the saved data to identify the failed leg. The NFE is checked for each switching cycle and if it is less than three for a few cycles, an OCF status is announced by the algorithm. To avoid the effect of noise and disturbance, two binary variables are defined for the first stage of the algorithm showing the status of “probable fault” and “definite fault” (PF and DF respectively). By repeating fault detection in three sequential cycles, PF is set. Then, the NFE is checked for the next five cycles and \( t_{C A P1} \) and \( t_{FE1} \) values are saved separately. If the OCF condition is confirmed again (at least in three of the five cycles), DF is set. In fact, the OCF status is announced by setting DF. Then the second stage of the algorithm is started. In Fig. 11 the proposed OC FD algorithm is depicted. The number of cycles for setting DF and PF is selected based on the required speed for FD and the reliability of the algorithm. Increasing the number of investigated cycles results in decreasing the misdetections and also the speed.

As mentioned, \( t_{FE1} \), \( t_{FE2} \), and \( t_{FE3} \) are calculated due to (4)-(5). During OCF only \( t_{CAP1} \) and \( t_{CAP2} \) are retrieved from CAP1 and CAP2 registers. In the second stage of OC FD algorithm, the difference between \( t_{FE1} \) and \( t_{CAPj} \) is calculated as:

\[
\begin{align*}
t_{e1,1} &= |t_{CAP1} - t_{FE1}| \\
t_{e2,1} &= |t_{CAP1} - t_{FE2}| \\
t_{e2,2} &= |t_{CAP2} - t_{FE2}| \\
t_{e3,2} &= |t_{CAP2} - t_{FE3}|
\end{align*}
\]

Using Table III and \( t_{eij} \) values, the missed FE is identified and using Table II, the failed leg is recognized.

After FD, the failed leg is disabled and a redundant leg is added to the inverter circuit through a TRIAC switch as shown in Fig. 12. The proposed algorithm can detect the failed leg (which could have one or two failed switches), but it is not able to determine the exact location of the failed switch. Meaning that by this algorithm it is not possible to recognize that the upper, lower or both switches of the leg are failed. Since replacing the total leg (instead of the failed switch) is introduced as an optimized FT strategy for three-phase inverters [35], this strategy is used in this paper. Therefore, the determination of the failed switch location is not necessary when the total leg is replaced with another one.

V. THE EXPERIMENTAL RESULTS

A low-voltage q-ZSI prototype shown in Fig. 13 is implemented. The switching and line frequencies are 20kHz and 50Hz respectively. The output voltage is 110V and \( V_B \) is 380V. The maximum value of \( D_{sh} \) and the minimum value of the input voltage in the prototype are 0.24 and 200V respectively. A 600V/15A power module (FSBS15CH60) is used in this prototype. Through adjusting SH state duration, the leg voltage peak value (\( v_{c1} + v_{c2} \)) is kept nearly constant (\( \approx V_B = 380V \)) when the input voltage varies. The PV input source is modeled with a DC supply voltage. The prototype provides 1.2kW on the AC side. The digital signal processor, TMS320F2808, provides PWM and the protection commands. The capture unit interface includes a resistive divider, a zener diode (as a voltage limiter) and an inexpensive comparator (LM311). Three TRIAC switches are connected to the middle of the main legs and the redundant leg similar to Fig. 12.

As it is mentioned, \( v_{leg} \) has a pulsating form and its peak value is equal to the sum of the voltages across \( C_1 \) and \( C_2 \). In Fig. 14, \( v_{leg} \) is shown. During SH states, \( v_{leg} \) is nearly equal to

\[
\text{voltage across the leg terminals (} v_{leg} \text{); the SH states are detectable by zero-value intervals; the peak value is nearly 380v.}
\]
In Fig. 15 (a)-(c), the output currents of the q-ZSI in normal conditions and during OCF in a switch/leg are shown. In Fig. 15 (a), the RMS value of the output current is equal to 3.5A per phase. In Fig 15(b), the leg “a” only conducts the current with negative polarity due to the OCF in $S_{aH}$. The output currents during OCF in both switches of a leg are shown in Fig. 15(c). $S_{aH}$ and $S_{aL}$ become OC simultaneously. After the fault, the current of phase “a” is zero.

$v_{leg}$ and $v_{cap}$ (the input of the capture unit) are measured and shown in Fig. 16(a)-(c) for normal conditions and during OCF in a switch/leg. Comparing Fig. 16(a) to Fig. 16(b)-(c) shows that the number of SH states are reduced during OCF. The disturbance originated from the OCF is visible on $v_{leg}$ in Fig. 16(b)-(c). The peak value of $v_{cap}$ is constant and equals $5V$. In Fig. 17(a)-(b), $v_{leg}$ peak value ($v_{c1} + v_{c2}$) is depicted during OCF in a switch/leg. The voltage drop across the capacitors during OCF is due to the reduction of the real SH duration. The line-frequency harmonics are also seen after the OCF in Fig. 17(a)-(b).

In Fig. 18(a)-(b), DF and PF signals before and after OC fault are depicted. The OC instant is highlighted with a dashed line in Fig. 18(a)-(b). After three cycles from the OC instant, PF is set. A few cycles later, DF is also set. Indeed, setting DF is the declaration of definite OC fault by the algorithm. At this point the algorithm enters the second stage. As an example, the data

<table>
<thead>
<tr>
<th>Cycle</th>
<th>CAP1</th>
<th>CAP2</th>
<th>$t_{el}$ [usec]</th>
<th>Sector</th>
</tr>
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<tbody>
<tr>
<td>Cycle 1</td>
<td>2076</td>
<td>2781</td>
<td>[16.50, 0.85, 6.78, 0.97]</td>
<td>1</td>
</tr>
<tr>
<td>Cycle 2</td>
<td>2046</td>
<td>2786</td>
<td>[16.29, 0.85, 7.06, 0.96]</td>
<td>1</td>
</tr>
<tr>
<td>Cycle 3</td>
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<td>2793</td>
<td>[16.08, 0.84, 7.38, 0.98]</td>
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</tr>
<tr>
<td>Cycle 4</td>
<td>1989</td>
<td>2780</td>
<td>[15.90, 0.87, 7.52, 0.84]</td>
<td>1</td>
</tr>
<tr>
<td>Cycle 5</td>
<td>1957</td>
<td>2795</td>
<td>[15.66, 0.85, 7.89, 0.92]</td>
<td>1</td>
</tr>
</tbody>
</table>
used at the second stage of FD algorithm in the OCF case in

Fig. 18(a) are shown in Table IV. $t_{cap_j}$ values are calculated

Fig. 17. The input capacitors voltage ($v_{C1} + v_{C2}$): (a) OCF in $S_{aH}$ (b) OCF in both $S_{aH}$ and $S_{aL}$.

Fig. 18. PF and DF signals after the OCF (a) OCF in $S_{aH}$ (b) OCF in both $S_{aH}$ and $S_{aL}$.

Fig. 19. The output currents in FT q-ZSI; (a) OCF in $S_{aH}$ and replacing the leg “a” in the nominal load; (b) OCF in $S_{aH}$ and $S_{aL}$ and replacing the leg “a” in the nominal load; (c) OCF in $S_{aH}$ and replacing the leg “a” in 30% of the nominal load; (d) OCF in $S_{aH}$ and $S_{aL}$ and replacing the leg “a” in 30% of the nominal load.
from \(CAP_j\) registers as:

\[
t_{capj} = \frac{CAP_j}{2 \times PRD} T_{sw}
\]  

(8)

In (8), PRD is the period of the DSP timer. In Table IV, the difference between the detected FE times and the calculated values in (4) are approximately 1 \(\mu\)sec. Using Table IV and Table III, it is concluded FE1 is not detected. Considering the sector number and Table II, one or both of switches of the leg “a” are failed.

After completing OC FD, the commands of the failed leg are disabled. Then, the redundant leg is activated and added to the inverter circuit through a TRIAC in the FT q-ZSI. In Fig. 19(a)-(d), it is shown how OC is covered by the fault tolerant operation (FTO). The moments of OCF and FTO (activating the redundant leg in the inverter circuit) are determined by the dashed lines in Fig. 19(a)-(d). In Fig. 19(a)-(b), the switch and leg OC occur in the nominal load condition. In Fig 19(c)-(d) the switch/leg OC occur in a light load where the output power is reduced to 30% of the nominal value. In both cases, the OCF is successfully recognized and the redundant leg is used instead of the failed leg.

CONCLUSION

In this paper, a novel, fast and cost-effective OC FD algorithm is presented for FT q-ZSI. The proposed method is independent of the load condition and is based on observing the SH state effect on the leg terminal voltage. No fast measurement or high-speed processor is required and only a low-cost comparator circuit is added to the system. The proposed FD algorithm is only applicable to voltage fed ZSIs.

For higher reliability in a PV system, FT q-ZSI is considered as a beneficial structure. FT q-ZSI has fewer semiconductor elements and a lower probability of facing OCF compared to FT double-stage PV converters. In addition, while in FT double-stage PV converters, two separate FT strategies are needed for each stage (DC/DC and inverter), the FT q-ZSI input side has no switch component. This makes FT q-ZSI more reliable and cost-effective. In this paper, the proposed FD algorithm is applied to an FT q-ZSI with one redundant leg. In less than ten switching cycles, the failed leg is recognized and disabled. The redundant leg is utilized instead of the failed leg.

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