Objective and Outline

**Objective:** Power Components

**Outline:**
1) Acknowledgements
2) ...

Acknowledgement

This lecture note has been obtained from similar courses all over the world. I wish to thank all the professors who created such good works on those lecture notes. Without them, these slides could have not been presented to you.
## CMOS Technology

<table>
<thead>
<tr>
<th>Technology</th>
<th>$V_{DD}$ (V)</th>
<th>$T_{ox}$ (Å)</th>
<th>$V_T$ (V)</th>
<th>$L_{eff}$ (µm)</th>
<th>$I_{off}$ (pA/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 µm</td>
<td>5</td>
<td>200</td>
<td>n/a</td>
<td>0.80</td>
<td>4.1 x 10^-4</td>
</tr>
<tr>
<td>0.8 µm</td>
<td>5</td>
<td>150</td>
<td>0.60</td>
<td>0.55</td>
<td>5.8 x 10^-2</td>
</tr>
<tr>
<td>0.6 µm</td>
<td>3.3</td>
<td>80</td>
<td>0.58</td>
<td>0.35</td>
<td>0.15</td>
</tr>
<tr>
<td>0.35 µm</td>
<td>2.5</td>
<td>60</td>
<td>0.47</td>
<td>0.25</td>
<td>8.9</td>
</tr>
<tr>
<td>0.25 µm</td>
<td>1.8</td>
<td>45</td>
<td>0.43</td>
<td>0.15</td>
<td>24</td>
</tr>
<tr>
<td>0.18 µm</td>
<td>1.6</td>
<td>30</td>
<td>0.40</td>
<td>0.10</td>
<td>86</td>
</tr>
</tbody>
</table>

Technologies:
- HDD: Shallow High-doped drain (no LDD) ← Scaling
- LDD: Lightly Doped Drain ← Reduce hot carrier effects

### Power metrics

- **Peak power**
- **Average power**
- **Energy**

P(t) graph demonstrating peak and average power over time.
Dynamic Power Consumption

- Average power consumption
  - Dynamic power consumption
  - Short-circuit power consumption
  - Leakage power consumption
  - Static power consumption
- Dynamic power dissipation during switching

Power Consumption

- Static Power (no input/output change)
  1. Leakage current.
  2. Sub-threshold conductance.
  3. Pseudo-NMOS has a static current (direct current path between supply and ground) when output is low.
- Dynamic Power (during input/output change)
  1. Capacitive Power due to charging/discharging of capacitive load. Note that sometimes only refer to this component as the dynamic power.
  2. Short-circuit power due to direct path currents when there is a temporary connection between power and ground. Note that sometimes only refer to this component as the short circuit power.
Dynamic Power Dissipation

- Signal properties
  - Signal probability, $P_i$: probability of a signal being logic ONE
  - Signal activity, $a_i$: probability of signal switching (0→1, or 1→0) $P_0\rightarrow_1 & P_1\rightarrow_0$

- Energy dissipated per transition

\[
E_{VDD} = \int_{0}^{\infty} i_{VDD}(t)V_{DD} dt = V_{DD} \int_{0}^{\infty} C_L \frac{dv_{out}}{dt} dt
\]

\[
= C_L V_{DD} \int_{0}^{r_{DD}} dV_{out} = \frac{1}{2} C_L V_{DD}^2
\]

\[
E_C = \int_{0}^{\infty} i_{VDD}(t)V_{out} dt = \int_{0}^{\infty} C_L \frac{dv_{out}}{dt} V_{out} dt = C_L \int_{0}^{r_{DD}} dV_{out} = \frac{1}{2} C_L V_{DD}^2
\]

Energy dissipated for 1→0 or 0→1 transition: $\frac{1}{2} C_L V_{DD}^2$

Dynamic Power Consumption

Energy/transition = $C_L \times V_{DD}^2 \times P_{0\rightarrow 1}$

$P_{dyn} = $ Energy/transition $\times f = C_L \times V_{DD}^2 \times P_{0\rightarrow 1} \times f$

$P_{dyn} = C_{EFF} \times V_{DD}^2 \times f$ where $C_{EFF} = P_{0\rightarrow 1} \times C_L$

Not a function of transistor sizes! Data dependent - a function of switching activity!
**Low-Power Integrated Circuit Design**  

**Section 4: Power Components**

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**Lowering Dynamic Power**

- **Capacitance:** Function of fan-out, wire length, transistor sizes
- **Supply Voltage:** Has been dropping with successive generations

\[
P_{\text{dyn}} = C_L \cdot V_{DD}^2 \cdot P_{0\rightarrow1} f
\]

- **Activity factor:** How often, on average, do wires switch?
- **Clock frequency:** Increasing...

---

**Dissipated Energy**

**Charging:**

\[
E_{\text{dis}0\rightarrow1} = E_{V_{dd}} - E_C = C_L \cdot V_{dd}^2/2
\]

**Discharging:**

\[
E_{\text{dis}1\rightarrow0} = E_C - 0 = C_L \cdot V_{dd}^2/2
\]

⇒ **Total dissipation**

\[
E_{\text{dis}1\rightarrow0} + E_{\text{dis}1\rightarrow0} = C_L \cdot V_{dd}^2
\]
**Dynamic Power Dissipation**

\[ P_{\text{dynamic}} = C_L \cdot V_{DD}^2 \cdot f \]

Assume \( P_{0 \rightarrow 1} \) for all gates 1.

- Example
  - 1.2 \( \mu \)m CMOS chip
  - 100 MHz clock rate
  - Average load capacitance of 30 fF/gate
  - 5V power supply
  - Power consumption/gate = 75 \( \mu \)W
  - Design with 200,000 gates: 15W!
- **Pessimistic evaluation:** not all gates switch at the full rate
  - Reducing \( V_{DD} \) has a quadratic effect on \( P_{\text{dynamic}} \)

---

**Node Transition Activity (Switching Activity Factor)**

- Consider switching a CMOS gate for \( N \) clock cycles

\[ E_N = C_L \cdot V_{dd}^2 \cdot n(N) \]

\( E_N \): the energy consumed for \( N \) clock cycles
\( n(N) \): the number of 0–>1 transition in \( N \) clock cycles

\[ P_{\text{avg}} = \lim_{N \to \infty} \frac{E_N}{N \cdot f_{\text{clk}}} = \left( \lim_{N \to \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{dd}^2 \cdot f_{\text{clk}} \]

\[ \alpha_{0 \rightarrow 1} = \lim_{N \to \infty} \frac{n(N)}{N} \]

\[ P_{\text{avg}} = \alpha_{0 \rightarrow 1} \cdot C_L \cdot V_{dd}^2 \cdot f_{\text{clk}} \]
Principles for Dynamic Power Reduction

- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 ... 0.9 V by 2010!)
- Reduce switching activity
- Reduce physical capacitance

Dynamic Power Consumption is Data Dependent

Switching activity, $P_{0\rightarrow1}$, has two components

- A static component – function of the logic topology
- A dynamic component – function of the timing behavior (glitching)

2 input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Static transition probability

$$P_{0\rightarrow1} = P_{\text{out}=0} \times P_{\text{out}=1}$$

$$= P_0 \times (1-P_0)$$

With input signal probabilities

$$P_{A=1} = 1/2$$

$$P_{B=1} = 1/2$$

NOR static transition probability

$$= 3/4 \times 1/4 = 3/16$$
NOR Gate Transition Probabilities

Switching activity is a strong function of the input signal statistics. \( P_A \) and \( P_B \) are the probabilities that inputs A and B are one.

\[
P_{0 \rightarrow 1} = P_0 \times P_1 = (1 - (1 - P_A)(1 - P_B)) \times (1 - P_A)(1 - P_B)
\]

Transition Probabilities for Some Basic Gates

<table>
<thead>
<tr>
<th>Gate</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOR</td>
<td>( (1 - (1 - P_A)(1 - P_B)) \times (1 - P_A)(1 - P_B) )</td>
</tr>
<tr>
<td>OR</td>
<td>( (1 - P_A)(1 - P_B) \times (1 - (1 - P_A)(1 - P_B)) )</td>
</tr>
<tr>
<td>NAND</td>
<td>( P_A P_B \times (1 - P_A P_B) )</td>
</tr>
<tr>
<td>AND</td>
<td>( (1 - P_A P_B) \times P_A P_B )</td>
</tr>
<tr>
<td>XOR</td>
<td>( (1 - (P_A + P_B - 2P_A P_B)) \times (P_A + P_B - 2P_A P_B) )</td>
</tr>
</tbody>
</table>

\( P_A \) at the inverter input is equal to \( P_1 \) at its output.

For \( X \): \( P_{0 \rightarrow 1} = P_0 \times P_1 = (1 - P_A) P_A = 0.5 \times 0.5 = 0.25 \)

For \( Z \): \( P_{0 \rightarrow 1} = P_0 \times P_1 = (1 - (0.5 \times 0.5)) \times (0.5 \times 0.5) = 3/16 \)
Transition Probabilities as a Function of Input Numbers

\[ P_{0 \rightarrow 1}(\text{NOR, NAND}) = \frac{(2^N - 1)}{2^{2N}} \quad P_{0 \rightarrow 1}(\text{XOR}) = \frac{1}{4} \]

Note: \(\text{XOR}_n(x_1, x_2, ..., x_n) = x_1 \oplus x_2 \oplus ... \oplus x_n\)

Inter-Signal Correlations

\[ P_{0 \rightarrow 1} = 1 - (1 - P_A P_B) P_A P_B \]

\[ P(Z = 1) = p(C = 1 \mid B = 1) \cdot p(B = 1) \]

\[ p_{0 \rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations
- CAD tools required for such analysis
Inter-Signal Correlations

- Determining switching activity is complicated by the fact that signals exhibit correlation in space and time
  - reconvergent fan-out

\[ P(Z=1) = P(B=1) \& P(X=1 \mid B=1) \]

\[ P(Z=1) = 0.5 \times 1 = 0.5 \]

Have to use conditional probabilities

⇒ Become complex and intractable fast!

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Logic Restructuring

- The first step in technology mapping is to decompose each logic function into two-input gates
- The objective of this decomposition is to minimizing the total power dissipation by reducing the total switching activity

---

\[ \alpha = 0.0384 \]

\[ \alpha = 0.0196 \]

\[ \alpha = 0.0099 \]

\[ \alpha = 0.1875 \]

\[ \alpha = 0.0099 \]
Logic Restructuring

- Logic restructuring: changing the topology of a logic network to reduce transitions

\[
P_{0\rightarrow1} = P_0 \times P_1 = (1 - P_A P_B) \times P_A P_B
\]

**Chain**

Chain implementation has a lower overall switching activity than the tree implementation for random inputs

Ignores glitching effects

**Input Re-Ordering**

**Worse**

**Better**

Beneficial to postpone the introduction of signals with a high transition rate (signals with signal probability close to 0.5)
### Input Re-Ordering

\[(1-0.5\times0.2)x(0.5\times0.2)=0.09\]

\[(1-0.2\times0.1)x(0.2\times0.1)=0.0196\]

\[
P_{X}(1) = P_{A}(1).P_{B}(1) = 0.1 \\
P_{X}(0) = 1 - P_{X}(1) = 0.9 \\
P_{X}(0 \rightarrow 1) = 0.0900 \\
P_{F}(1) = P_{X}(1).P_{C}(1) = 0.01 \\
P_{F}(0 \rightarrow 1) = 0.099
\]

<table>
<thead>
<tr>
<th></th>
<th>101</th>
<th>000</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td></td>
<td></td>
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</tbody>
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**Beneficial to postpone the introduction of signals with a high transition rate (signals with signal probability close to 0.5)**

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### Glitching in Static CMOS Networks

Gates have a nonzero propagation delay resulting in spurious transitions or **glitches** (dynamic hazards).

Glitch: node exhibits multiple transitions in a single cycle before settling to the correct logic value.

An example of a glitching node:

\[
\begin{array}{c}
  A \\
  B \\
  C \\
\end{array} \xrightarrow{\text{X}} \begin{array}{c}
  X \\
  Z \\
\end{array}
\]

**Unit Delay**
Glitching in Static CMOS Networks

Gates have a nonzero propagation delay resulting in spurious transitions or glitches (dynamic hazards)

- glitch: node exhibits multiple transitions in a single cycle before settling to the correct logic value

```
A  B  X  C  Z
```

<table>
<thead>
<tr>
<th>ABC</th>
<th>101</th>
<th>000</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td></td>
<td>Glitch</td>
</tr>
</tbody>
</table>

Unit Delay

Spurious Transition at a Node ➔ Glitching Power

Hazardous transition occurs at the output of AND gate due to different delays through two different paths converging at the inputs to the AND gate.

- Assume each gate has unit delay
- Width of the glitch depends on the delays through the logic gates and interconnects.
Example: Glitching in an Ripple Carry Adder (RCA)

- Ripple carry adder generates the carry of each bit based on the sum of the previous bits.

Balanced Delay Paths to Reduce Glitching

- Glitching is due to a mismatch in the path lengths in the logic network; if all input signals of a gate change simultaneously, no glitching occurs

So equalize the lengths of timing paths through logic
Solution: Balanced Delay Paths

- The diagrams only schematically shows the idea behind each type of adder.
- Carry lookahead adder generates the carry of each bit based on the previous bits without waiting for the sum of the previous bits to propagate → Make the delay of all carry almost the same

Factors Affecting Transition Activity: $\alpha_{0 \rightarrow 1}$

- “Static” component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations
  - # of inputs
- “Dynamic” or timing dependent component
  - Circuit Topology (Type and style)
  - Signal Statistics and Correlations
Finite slope of the input signal causes a direct current path between $V_{DD}$ and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

$I_{SC}$ is determined by the two voltages of the n and p transistors:

1) $V_{GS}(t)$ is a function of the input slope. Determines on/off state of the transistors.
2) $V_{DS}(t)$ is a function of the output slope-determined by $C_L$. Determines the region of operation (linear/saturation) of the transistors.

Note: The current used for charging the capacitor is not wasted.

inputs have finite rise and fall times

Direct current path from $V_{DD}$ to GND while PMOS and NMOS are ON simultaneously for a short period

$I_{mean}$ is the average short circuit current for one period that the output make a transition.
Symmetrical Inverter Without Load

\[ I_{mean} = 2 \left[ \frac{1}{T} \int_{t_1}^{t_2} I(t) \, dt + \frac{1}{T} \int_{t_2}^{t_3} I(t) \, dt \right] \]

If \( V_{in} = -V_{in} = V_t \) and \( \beta_n = \beta_p = \beta \) and that the behavior around \( t_2 \) is symmetrical

\[ I_{mean} = 2 \times \frac{2}{T} \int_{t_1}^{t_2} \frac{\beta}{2} (V_{in}(t) - V_t)^2 \, dt \]

with \( V_{in}(t) = \frac{V_{DD}}{t_r} t \)

\[ t_1 = \frac{V_t}{V_{DD}} \cdot t_r \]

\[ t_2 = \frac{t_r}{2} \]

\[ t_r = t_f = t_{rf} \]

Symmetrical Inverter Without Load

\[ I_{mean} = \frac{2 \beta}{T} \int_{t_r V_T/V_{DD}}^{t_r/2} \left( \frac{V_{DD}}{t_{rf}} \cdot t - V_t \right)^2 \, dt \]

\[ = \frac{2 \beta}{T} \left[ \frac{t_{rf}}{3 V_{DD}} \left( \frac{V_{DD}}{t_{rf}} \cdot t - V_t \right)^3 \right]_{t_r V_T/V_{DD}}^{t_r/2} \]

\[ = \frac{2t_{rf}}{3T} \cdot \frac{\beta}{V_{DD}} (V_{DD} - 2V_t)^3 \]

\[ = \frac{t_{rf}}{12T} \cdot \frac{\beta}{V_{DD}} (V_{DD} - 2V_t)^3 \]

\[ P_{sc} = \frac{\beta}{12} (V_{DD} - 2V_t)^3 \cdot \frac{t_{rf}}{T} \]
**Short Circuit Currents**

\[ E_{sc} = t_{sc} \cdot V_{DD} \cdot I_{peak} \cdot P_{0 \rightarrow 1} \]

\[ P_{sc} = t_{sc} \cdot V_{DD} \cdot I_{peak} \cdot f_{0 \rightarrow 1} \]

\[ I_{mean} = I_{peak} \cdot t_{sc} / T \]

- Duration and slope of the input signal determines \( t_{sc} \).
- \( I_{peak} \) determined by
  - the saturation current of the P and N transistors which depend on their sizes, process technology, temperature, etc.
  - strong function of the ratio between input and output slopes
  - a function of \( C_L \)

---

**Output Transitions under Different Loads**

[Diagram showing output voltage over time for different capacitances and input voltages]
Impact of $C_L$ on $P_{sc}$

Large capacitive load

Output fall time significantly larger than input rise time.

$\Rightarrow$ $C_L$ remain short circuit till the end of the input transition. (Bad for cascaded logic)

The current used for discharging the capacitance is not considered as the short circuit current.

Small capacitive load

Output fall time substantially smaller than the input rise time.

$\Rightarrow$ $C_L$ quickly becomes open circuit and the current is determined by the ratio of the two transistors on-resistances. Since this current is not used in charging the capacitor, it is wasted.

$I_{\text{peak}}$ as a Function of $C_L$

When load capacitance is small, $I_{\text{peak}}$ is large.

Short circuit dissipation is minimized by matching the rise/fall times of the input and output signals - slope engineering.
Short-Circuit Current

- Short circuit current goes to zero if $t_{\text{fall( Output)}} >> t_{\text{rise(input)}}$
- But cannot do this for cascaded logic
  - Keep input and output rise/fall times the same
  - Less than 10% of the total consumption

Conclusions:
- If inverter is lightly loaded (small $C_L$, so output $t_r, t_f$ are shorter than input $t_r, t_f$) then $P_{\text{SC}}$ becomes comparable to dynamic dissipation.
- When input and output have equal rise and fall times, $P_{\text{SC}}$ is small $\Rightarrow$ Must make input $t_r, t_f$ equal to output $t_r, t_f$. 
**P_{sc} as a Function of Rise/Fall Times**

When load capacitance is small ($t_{\text{rise}}/t_{\text{fall}} > 2$ for $V_{DD} > 2\text{V}$) the power is dominated by $P_{sc}$.

If $V_{DD} < V_{TN} + |V_{TP}|$ then $P_{sc}$ is eliminated since both devices are never on at the same time.

\[
\frac{W}{L_p} = 1.125 \ \mu\text{m}/0.25 \ \mu\text{m} \\
\frac{W}{L_n} = 0.375 \ \mu\text{m}/0.25 \ \mu\text{m} \\
C_L = 30 \ \text{fF}
\]

**Static Power Consumption**

\[
P_{\text{stat}} = P_{(In=1)} \cdot V_{dd} \cdot I_{\text{stat}}
\]

Wasted energy ...

Should be avoided almost in all cases.
Leakage Components of the Static Power Dissipation

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punch-through
6. Narrow width effect (for trench isolation)
7. Gate oxide tunneling
8. Hot carrier injection

Subthreshold (Weak Inversion)/Reversed Biased PN Junction Currents

\[ I_D = K \cdot e^{(V_{gs} - V_t)q / nkT} (1 - e^{V_{ds}q / kT}) \]

Sub-threshold current

\[ I_O = i_s (e^{Vq / kT} - 1) \]

Diode leakage

db(PMOS) pn junction: \( V_{db} = 0 \)

\[ V_{out} = V_{DD} \]

db(NMOS) pn junction: \( V_{db} = V_{DD} \)

Long channel model if \( V_t \) does not contain DIBL effect.
Reverse Biased pn Junction

- Leakage current through the reverse biased diode junctions.
- For typical devices it is between 10pA – 500pA at room temperature.
- For a die with 1 million devices operated at 5 V, this results in 0.5mW power consumption → not much.
- Junction leakage current is caused by thermally generated carriers → therefore is a strong function of temperature ($JS$ doubles for every 9 deg C!)
- For 0.25 μm CMOS: $JS = 10$-100 pA/μm² at 25 deg C.

\[
I_{DL} = JS \times A
\]

Subthreshold Leakage Component

- Leakage control is critical for low-voltage operation.
  - The sub-threshold leakage is very important when the threshold voltage is close to 0.
  - Sub-threshold current is one of most compelling issues in low-energy circuit design!
Leakage as a Function of $V_T$

- Continued scaling of supply voltage and the subsequent scaling of threshold voltage will make subthreshold conduction a dominate component of power dissipation.

- An 90mV/decade $V_T$ roll-off - so each 255mV increase in $V_T$ gives 3 orders of magnitude reduction in leakage (but adversely affects performance)

Gate Oxide Tunneling

- $I_{GD} \sim e^{-\frac{V_{GD}}{V_{TH}}}$
- $I_{GS} \sim e^{-\frac{V_{GS}}{V_{TH}}}$

- Independent of the subthreshold leakage
- Contributes to the total leakage
- Modeled in BSIM4
- Also in BSIM3v3 but foundries usually do not include it
**Gate Oxide Tunneling**

- High $E_{ox}$ electric field across oxide layer causes:
  - **Direct electron** tunneling through gate
    
    $$I_{ox1} \approx e^{-eT_{ox}} e^{dV_{ox}}$$
  
  - **Fowler-Nordheim** (FN) tunneling through oxide bands (usually only at higher $E_{ox}$ than chips use)
    
    $$I_{ox2} = A E_{ox}^2 e^{-b/E_{ox}}$$

- Currently is a non-issue, expected to become dominant leakage condition as oxides get thinner
Gate-Induced Drain Leakage (GIDL)

- **High field** between gate and drain (small gate and large drain voltages) increases the hole-electron generation injecting holes into substrate and electron into the drain → substrate leakage and drain current increase.

- Some electrons tunnel from gate to drain using surface traps and/or band-to-band tunneling. gate leakage and drain current increase. This component is not considered as GIDL.

- Increasing current for **negative** $V_G$ values

- **Localized** along channel width between gate and drain

- Major problem in $I_{off}$ current:
  - Caused by thinner $t_{ox}$, higher $V_{DD}$, and lightly doped drains.

- Contributes to standby power, so must control this by increasing oxide thickness, increasing drain doping, or eliminating traps.

- For high performance device (low $V_{th}$), is not a major issue.
Drain-Induced Barrier-Lowering (DIBL)

- **Depletion region of drain** interacts with source near channel surface
  - Voltage at the drain lowers the potential barrier at the source
    - Lowers $V_{th}$
    - **Increases subthreshold** current **without any change on $S$**
  - Causes source to inject carriers into channel surface independent of the gate voltage
  - More DIBL at higher $V_D$ and shorter $L_{eff}$
  - Moves curve up, to right, as $V_D$ increases
- **Surface** DIBL happens before **deep bulk** punchthrough
- **Fix DIBL:**
  - Higher surface & channel doping
  - Shallow source/drain junction depths

Punchthrough

- Happens when drain and source depletion regions approach each other and touch.
- Lets **channel current** exist deep in sub-gate region and in the surface
  - **Gate loses control of sub-gate region.**
- Varies **quadratically** with $V_D$ and with $V_S$.
- Viewed as **subsurface (deep in bulk)** version of DIBL
Narrow-Width Effect

- Trench isolation:
  - Dig trench in substrate and fill with SiO$_2$ to isolate $n$ and $p$ MOSFETs
- Non-trench isolated technologies (LOCOS):
  - $V_t$ increases for gate widths of 0.5 μm
- Trench isolated technologies:
  - $V_t$ decreases for effective channel widths $W \leq 0.5$ μm

DIBL, GIDL, Weak Inversion

- DIBL $\Rightarrow$ Moves curve up, to right as $V_D$ increases
  - $V_D$ going from 0.1 to 2.7 V, $I_D$ changed $1.68 \times$ decades
  - 1.55V/decade change of $I_D$

Large $V_G$'s means less GIDL
Leakage Components

Weak inversion + pn junction + DIBL + GIDL
@ $V_D = 3.9 \text{ V}$
- GIDL dominates

Weak inversion + pn junction + DIBL
@ $V_D = 2.7 \text{ V}$
- DIBL dominates

Weak inversion + pn junction
(80 mV/dec & $V_D = 0.1 \text{ V}$)
- Weak inversion dominates

1. No punchthrough
2. No width effect
3. No gate leakage

CMOS Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} P_{0\rightarrow1} + V_{DD} I_{leakage} T_{leakage}$$

$$f_{0\rightarrow1} = P_{0\rightarrow1} \cdot f_{clock}$$

$$P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} f_{0\rightarrow1} + V_{DD} I_{leakage} T_{leakage} / T$$

Dynamic power  Short-circuit power  Leakage power