9.2.7 Increasing the Output Voltage Range: The Wide-Swing Current Mirror

In Section 9.2.2 it was found that while the output voltage of the circuit of Fig. 9.9 can swing to within $2|V_{BE}|$ of $V_{CE}$, the cascode current mirror limits the negative swing to $V_{CE} - V_{BE}$. In other words, the cascode mirror reduces the voltage swing by $V_{BE}$ volts. This point is further illustrated in Fig. 9.12(a), which shows a cascode mirror (with $V_{BE} = 0$, for simplicity) and indicates the voltages that result at the various nodes. Observe that because the voltage at the gate of $Q_2$ is $V_{CE} - V_{BE}$, the minimum voltage permitted at the output (while $Q_1$ remains saturated) is $V_T + 2V_{BE}$, hence the extra $V_T$. Also, observe that $Q_1$ is operating with a drain-to-source voltage $V_{DS}$, which is $V_T$ volts greater than it needs to operate in saturation.

The observations above lead us to the conclusion that to permit the output voltage at the drain of $Q_2$ to swing as low as $2V_{BE}$, we must lower the voltage at the gate of $Q_2$ from $V_{CE} - 2V_{BE}$ to $V_{DS} + 2V_{BE}$. This is exactly what is done in the modified mirror circuit in Fig. 9.12(b). The gate of $Q_2$ is now connected to a bias voltage $V_{BE2} = V_T + 2V_{BE}$. Thus the output voltage can go down to $2V_{BE}$ with $Q_2$ still in saturation. Also, the voltage at the drain of $Q_2$ is now $V_{DS}$ and thus $Q_2$ is operating at the edge of saturation. The same is true of $Q_1$, and thus the current tracking between $Q_1$ and $Q_2$ will be assured. Note, however, that we can no longer connect the gate of $Q_2$ to its drain. Rather, it is connected to the drain of $Q_1$, which establishes a voltage of $V_{DS}$ at the drain of $Q_1$, which is sufficient to operate $Q_1$ in saturation (as long as $V_T$ is greater than $V_{BE}$, which is usually the case). This circuit is known as the wide-swing current mirror. Finally, note that Fig. 9.12(b) does not show the circuit for generating $V_{BE2}$. There are a number of possible circuits to accomplish this task, one of which is explored in Exercise 9.8.

9.3 THE 741 OP-AMP CIRCUIT

Our study of JFET op amps is focused on the 741 op-amp circuit, which is shown in Fig. 9.13. Note that in keeping with the IC design philosophy the circuit uses a large number of transistors, but relatively few resistors, and only one capacitor. This philosophy is dictated by the economics (silicon area, ease of fabrication, quality of realizable components) of the fabrication of active and passive components in IC form (see Section 6.1 and Appendix A).

As in the case with most general-purpose IC op amps, the 741 requires two power supplies, $+V_{CC}$ and $-V_{EE}$. Normally, $V_{CC} = V_{EE} = 15$ V, but the circuit also operates satisfactorily with the power supplies reduced to much lower values (such as ±5 V). It is important to observe that no circuit node is connected to ground, the common terminal of the two supplies. With a relatively large circuit such as that shown in Fig. 9.13, the first step in the analysis is the identification of its recognizable parts and their functions. This can be done as follows.

9.3.1 Bias Circuit

The reference bias current of the 741 circuit, $I_{REF}$, is generated in the branch at the extreme left of Fig. 9.13, consisting of the two diode-connected transistors $Q_1$ and $Q_2$ and the resistance $R_b$. Using a Widlar current source formed by $Q_1$, $Q_{20}$, and $R_b$, bias current for the first stage is generated in the collector of $Q_{20}$. Another current mirror formed by $Q_2$ and $Q_3$ takes part in biasing the first stage.

The reference bias current $I_{REF}$ is used to provide two proportional currents in the collectors of $Q_{20}$. This double-collector lateral pnp transistor can be thought of as two

See Appendix A for a description of lateral pnp transistors. Also, their characteristics were discussed in Section 6.2.
transistors whose base-emitter junctions are connected in parallel. Thus $Q_2$ and $Q_3$ form a two-output current mirror: One output, the collector of $Q_{3,2}$ provides bias current for $Q_{3,1}$, and the other output, the collector of $Q_{3,1}$, provides bias current for the output stage of the op-amp.

Two more transistors, $Q_{3,3}$ and $Q_{3,4}$, take part in the dc bias process. The purpose of $Q_{3,3}$ and $Q_{3,4}$ is to establish two $V_{BE}$ drops between the bases of the output transistors $Q_{3,2}$ and $Q_{3,1}$.

### 9.3.2 Short-Circuit Protection Circuitry

The 741 circuit includes a number of transistors that are normally off and conduct only in the event that one attempts to draw a large current from the op-amp output terminal. This happens, for example, if the output terminal is short-circuited to one of the two supplies. The short-circuit protection network consists of $R_T$, $R_T$, $Q_T$, $Q_T$, $R_T$, and $Q_T$. In the following we shall assume that these transistors are off. Operation of the short-circuit protection network will be explained in Section 9.5.3.

### 9.3.3 The Input Stage

The 741 circuit consists of three stages: an input differential stage, an intermediate single-ended high-gain stage, and an output-buffering stage. The input stage consists of transistors $Q_1$ through $Q_4$, with biasing performed by $Q_9$, $Q_6$, and $Q_7$. Transistors $Q_1$ and $Q_2$ act as emitter followers, causing the input resistance to be high and delivering the differential input signal to the differential common-base amplifier formed by $Q_3$ and $Q_4$. Thus the input stage is the differential version of the common-collector common-base configuration discussed in Section 6.11.3.

Transistors $Q_5$, $Q_6$, and $Q_7$ and resistors $R_5$, $R_6$, and $R_7$ form the load circuit of the input stage. This is an elaborate current-mirror load circuit, which we will analyze in detail in Section 9.5.1. It will be shown that this load circuit not only provides a high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection. The output of the input stage is taken single-ended at the collector of $Q_4$.

As mentioned in Section 7.7.2, every op-amp circuit includes a level shifter whose function is to shift the dc level of the signal so that the signal at the op-amp output can swing positive and negative. In the 741, level shifting is done in the first stage using the lateral pnp transistors $Q_1$ and $Q_2$. Although lateral pnp transistors have poor high-frequency performance, their use in the common-base configuration (which is known to have good high-frequency responses) does not seriously impair the op-amp frequency response.

The use of the lateral pnp transistors $Q_1$ and $Q_2$ in the first stage results in an added advantage: protection of the input-stage transistors $Q_3$ and $Q_4$ against emitter-base junction breakdown. Since the emitter-base junction of an npn transistor breaks down at about 7 V of reverse bias (see Section 5.2.5), regular npn differential stages suffer such a breakdown if, for example, the supply voltage is accidentally connected between the input terminals. Lateral pnp transistors, however, have high emitter-base breakdown voltages (above 30 V) and because they are connected in series with $Q_3$ and $Q_4$, they provide protection of the 741 input transistors, $Q_3$ and $Q_4$.

### 9.3.4 The Second Stage

The second or intermediate stage is composed of $Q_{3,3}$, $Q_{3,4}$, $Q_{3,5}$, and the two resistors $R_T$ and $R_T$. Transistor $Q_{3,3}$ acts as an emitter follower, thus giving the second stage a high input
resistance. This minimizes the loading on the input stage and avoids low of gain. Transistor $Q_1$ acts as a common-emitter amplifier with a 100-k resistor in the emitter. Its load is composed of the high output resistance of the pop-current source $Q_{10}$ in parallel with the input resistance of the output stage (seen looking into the base of $Q_{12}$). Using a transistor current source as a load resistance (active load) enables one to obtain high gain without resorting to the use of large load resistances, which would occupy a large chip area and require large power supply voltages.

The output of the second stage is taken at the collector of $Q_{14}$. Capacitor $C_5$ is connected in the feedback path of the second stage to provide frequency compensation using the Miller compensation technique studied in Section 8.11. It will be shown in Section 9.5 that the relatively small capacitor $C_5$ gives the 741 a dominant pole at about 4 Hz. Furthermore, pole splitting causes other poles to be shifted to much higher frequencies, giving the op amp a uniform –20-dB/decade gain roll-off with a unity-gain bandwidth of about 1 MHz. It should be pointed out that although $C_5$ is small in value, the chip area that it occupies is about 13 times that of a standard npn transistor!

9.3.5 The Output Stage

The purpose of the output stage is to provide the amplifier with a low output resistance. In addition, the output stage should be able to supply relatively large load currents without dissipating an undue large amount of power in the IC. The 741 uses an efficient output circuit known as a class AB output stage.

Output stages are studied in detail in Chapter 14, and the output stage of the 741 will be discussed in some detail in Section 9.6. For the time being we wish to point out the difference between the class AB output stage and the output stage we are familiar with, namely the emitter (or source) follower. Figure 9.14(a) shows an emitter follower biased with a constant-current source $I$. To keep the emitter-follower transistor conducting at all times and thus ensure the low output resistance it provides, the bias current $I$ must be greater than the largest magnitude of load current $I_L$. This is known as class A operation and the emitter (source) follower is a class A output stage. The drawback of class A operation is the large power dissipated in the transistor.

The power dissipated in the output stage can be reduced by arranging for the transistor to turn on only when an input signal is applied. For this to work, however, one needs two transistors, an npn to source output current and a pnp to sink output current. Such an arrangement is shown in Fig. 9.14(b). Observe that both transistors will be cut off when $V_i = 0$. In other words, the transistors are biased at a zero dc current. When $V_i$ goes positive, $Q_2$ conducts while $Q_3$ remains off. When $V_i$ goes negative the transistors reverse roles. This arrangement is known as class B operation and the circuit is a class B output stage.

Although efficient in terms of power dissipation, the class B circuit causes output signal distortion, as illustrated in Fig. 9.14(c). This is a result of the fact that for $|V_i|$ less than about 0.5 V, neither of the transistors conducts and $V_{out} = 0$. This type of distortion is known as crossover distortion.

Crossover distortion can be reduced by biasing the output-stage transistors at a low current. This ensures that the output transistors $Q_2$ and $Q_3$ will remain conducting when $V_i$ is small. As $I_C$ increases, one of the two transistors conducts more, while the other shuts off, in a manner similar to that in the class B stage.

There are a number of ways for biasing the transistors of the class AB stage. Figure 9.14(d) shows one such approach utilizing two short-circuited transistors $Q_4$ and $Q_5$ with junctions.
9.3.6 Device Parameters

In the following sections we shall carry out a detailed analysis of the 741 circuit. For the standard npn and pnp transistors, the following parameters will be used:

npn: \( I_{C} = 10^{-14} \text{A}, \beta = 200, V_C = 125 \text{ V} \)

pnp: \( I_{C} = 10^{-14} \text{A}, \beta = 50, V_C = 50 \text{ V} \)

In the 741 circuit the nonstandard devices are \( Q_{15} \) and \( Q_{16} \), and \( Q_{18} \). Transistor \( Q_{15} \) will be assumed to be equivalent to two transistors, \( Q_{15a} \) and \( Q_{15b} \) with parallel base-emitter junctions and having the following saturation currents:

\( I_{SA} = 0.25 \times 10^{-14} \text{A} \)
\( I_{SB} = 0.75 \times 10^{-14} \text{A} \)

Transistors \( Q_{15} \) and \( Q_{16} \) will be assumed to each have an area three times that of a standard device. Output transistors usually have relatively large areas, to be able to supply large load currents and dissipate relatively large amounts of power with only a moderate increase in device temperature.

9.4 DC ANALYSIS OF THE 741

In this section, we shall carry out a dc analysis of the 741 circuit to determine the bias point of each device. For the dc analysis of an op-amp circuit the input terminals are grounded. Theoretically speaking, this should result in zero dc voltage at the output. However, because the op amp has very large gain, any slight approximation in the analysis will show that the output voltage is far from being zero and is close to either \( +V_{EE} \) or \( -V_{EE} \). In actual practice, an op amp left open-loop will have an output voltage saturated close to one of the two supplies. To overcome this problem in the dc analysis, it will be assumed that the op amp is connected in a negative-feedback loop that stabilizes the output dc voltage to zero volts.

9.4.1 Reference Bias Current

The reference bias current \( I_{BB} \) is generated in the branch composed of the two diode-connected transistors \( Q_{1} \) and \( Q_{2} \) and resistor \( R_{f} \). With reference to Fig. 9.13, we can write

\[ I_{BB} = \frac{-V_{EE} - V_{EEI} - (V_{EE} + V_{EE})}{R_{f}} \]

For \( V_{EE} = V_{EE} = 15 \text{ V} \) and \( V_{EEI} = V_{EEI} = 0.7 \text{ V} \), we have \( I_{BB} = 0.73 \text{ mA} \).

9.4.2 Input-Stage Bias

Transistors \( Q_{1} \) is biased by \( I_{BB} \), and the voltage developed across it is used to bias \( Q_{15} \), which has a series emitter resistance \( R_{e} \). This part of the circuit is redrawn in Fig. 9.15 and can be recognized as the Widlar current source studied in Section 6.12.5. From the circuit, and assuming \( \beta_{e} \) to be large, we have

\[ V_{EE} - V_{EE} = I_{BB} R_{e} \]

Thus

\[ V_{EE} = \frac{I_{BB}}{R_{e}} = I_{BB} R_{e} \]  \hspace{1cm} (9.66)

where it has been assumed that \( I_{BB} = I_{BB} \). Substituting the known values for \( I_{BB} \) and \( R_{e} \), this equation can be solved by trial and error to determine \( I_{BB} \). For our case, the result is \( I_{BB} = 19 \mu\text{A} \).

9.5 For the standard npn transistor whose parameters are given in Section 9.3.4, find approximate values for the following parameters at \( V_{CC} = 1 \text{ mV}, V_{EE} = 0 \text{ V}, V_{CE} = 1 \text{ mV} \), and \( I_{C} = 1 \text{ mA} \).

9.10 For the circuit in Fig. 9.10, neglect base currents and use the exponential \( e^{-RC} \) relationship to show that

\[ I_{C} = \frac{V_{CC} - V_{CE}}{I_{C}} \]
Having determined $i_{CC}$, we proceed to determine the dc current in each of the input-stage transistors. Part of the input stage is redrawn in Fig. 9.16. From symmetry, we see that

$$I_{C1} = I_{C2}$$

Denote this current by $I$. We see that if the npn $\beta_1$ is high, then

$$I_{C2} = I_{MO} = I$$

and the base currents of $Q_1$ and $Q_2$ are equal, with a value of $1/2 \beta_1 = 1/\beta_2$, where $\beta_2$ denotes $\beta$ of the pnp devices.

The current mirror formed by $Q_1$ and $Q_2$ is fed by an input current of 2$I$. Using the result in Eq. (9.21), we can express the output current of the mirror as

$$i_{CM} = \frac{2I}{1 + 2/\beta_2}$$

We can now write a node equation for node X in Fig. 9.16 and thus determine the value of $I$. If $\beta_2 \gg 1$, then this node equation gives

$$2I = i_{CM}$$

For the 741, $i_{CM} = 19 \mu A$; thus $I = 9.5 \mu A$. We have thus determined that

$$I_{C1} = I_{C2} = I = I_{CM} = 9.5 \mu A$$

At this point, we should note that transistors $Q_1$, through $Q_4$, $Q_5$, and $Q_6$ form a negative-feedback loop, which works to stabilize the value of $I$ as approximately $I_{CM}/2$. To appreciate this fact, assume that for some reason the current $I$ in $Q_1$ and $Q_2$ increases. This will cause the current pulled from $Q_3$ to increase, and the output current of the $Q_3$, $Q_4$ mirror will correspondingly increase. However, since $i_{CM}$ remains constant, node X forces the combined base currents of $Q_2$, and $Q_5$ to decrease. This in turn will cause the emitter currents of $Q_3$ and $Q_4$, and hence the collector currents of $Q_4$ and $Q_5$ to decrease. This is opposite in direction to the change originally assumed. Hence the feedback is negative, and it stabilizes the value of $I$.

Figure 9.17 shows the remainder of the 741 input stage. If we neglect the base current of $Q_6$, then

$$i_{CM} = I$$

Similarly, neglecting the base current of $Q_4$, we obtain

$$I_{C2} = I$$

The bias current of $Q_1$ can be determined from

$$I_{C1} = I_{E2} = \frac{2}{\beta_1} \frac{V_{BAO} + 18}{R_3}$$

(9.67)

where $\beta_1$ denotes $\beta$ of the npn transistors. To determine $V_{BAO}$ we use the transistor exponential relationship and write

$$V_{BAO} = V_T \ln \frac{I}{i_{CM}}$$

Substituting $I = 10^{-14}$ A and $I = 9.5 \mu A$ results in $V_{BAO} = 517$ mV. Then substituting in Eq. (9.67) yields $i_{CM} = 10.5 \mu A$. Note that the base current of $Q_6$ is indeed negligible in comparison to the value of $I$, as has been assumed.
9.4.3 Input Bias and Offset Currents

The input bias current of an op amp is defined (Chapters 2 and 7) as

\[ I_B = \frac{I_{IPO} + I_{IOM}}{2} \]

For the 741, we obtain

\[ I_B = \frac{I_{IPO} + I_{IOM}}{2} \]

Using \( I_{IPO} = 200 \), yields \( I_B = 47.5 \) nA. Note that this value is reasonably small and is typical of general-purpose op amps that use BFTs in the input stage. Much lower input bias currents (in the picoamp or femtamp range) can be obtained using a FET input stage. Also, there exist techniques for reducing the input bias current of bipolar-input op amps.

Because of possible mismatches in the \( \beta \) values of \( Q_1 \) and \( Q_2 \), the input base current will not be equal. Given the value of the \( \beta \) mismatch, one can use Eq. (7.137) to calculate the input offset current, defined as

\[ I_{OS} = |I_{1B} - I_{2B}| \]

9.4.4 Input Offset Voltage

From Chapter 7 we know that the input offset voltage is determined primarily by mismatches between the two sides of the input stage. In the 741 op amp, the input offset voltage is due to mismatches between \( Q_1 \) and \( Q_2 \), between \( Q_3 \) and \( Q_4 \), and between \( Q_1 \) and \( Q_4 \), and between \( R_1 \) and \( R_2 \). Evaluation of the components of \( V_{OS} \) corresponding to the various mismatches follows the method outlined in Section 7.4. Basically, we find the current that results at the output of the first stage due to the particular mismatch being considered. Then we find the differential input voltage that must be applied to reduce the output current to zero.

9.4.5 Input Common-Mode Range

The input common-mode range is the range of input common-mode voltages over which the input stage remains in the linear active mode. Refer to Fig. 9.13. We see that in the 741 circuit the input common-mode range is determined at the upper end by saturation of \( Q_1 \) and \( Q_2 \), and at the lower end by saturation of \( Q_3 \) and \( Q_4 \).

**Exercise 9.32**

Sketch the voltage drops across \( R_1 \) and \( R_2 \), and assume that \( V_{DC} = V_{CC} = 15 \) V. Show that the input common-mode range of the 741 is approximately ±12.5 to ±14.7 V. (Assume that \( V_{BE} = 0.6 \) V and that to avoid saturation, \( V_{CE} > 0.3 \) V for an npn transistor, and \( V_{CE} > 0.3 \) V for a pnp transistor.)

9.4.6 Second-Stage Bias

If we neglect the base current of \( Q_3 \), then we see from Fig. 9.13 that the collector current of \( Q_3 \) is approximately equal to the current supplied by current source \( I_{CC} \). Because \( Q_{25} \) has a scale current 0.7% times that of \( Q_3 \), its collector current will be \( I_{C3} = 0.7 I_{CC} \). We must have assumed that \( \beta_2 \approx 1 \). Thus \( I_{C3} \) is 0.55 \( \mu \)A. At this current level the base-emitter voltage of \( Q_3 \) is

\[ V_{BE3} = V_T \log_{10} \left( \frac{I_{C3}}{I_{S}} \right) = 618 \text{ mV} \]

The collector current of \( Q_{25} \) can be determined from

\[ I_{C25} = I_{C3} = I_{C3} R_2 + V_{BE25} \]

This calculation yields \( I_{C3} = 16.2 \) \( \mu \)A. Note that the base current of \( Q_{25} \) will indeed be negligible compared to the input-stage bias \( I_B \) as we have assumed.

9.4.7 Output-Stage Bias

Figure 9.18 shows the output stage of the 741 with the short-circuit protection circuitry omitted. Current source \( Q_{28} \) delivers a current of 0.25\( I_{REF} \) (because \( I_B \) of \( Q_{28} \) is 0.25 times the \( I_B \) of \( Q_{25} \)) to the network composed of \( Q_{25} \), \( Q_{26} \), and \( R_{26} \). If we neglect the base currents of \( Q_{25} \) and \( Q_{26} \), then the emitter current of \( Q_{25} \) will also be equal to 0.25\( I_{REF} \). Thus

\[ I_{C3} = I_{C25} = 0.25 I_{REF} = 180 \mu \text{A} \]

Thus we see that the base current of \( Q_{25} \) is only 180/50 = 3.6 \( \mu \)A, which is negligible compared to \( I_{C3} \), as we have assumed.

![Figure 9.18 The 741 output stage without the short-circuit protection devices.](image-url)
If we assume that $V_{BE}$ is approximately 0.6 V, we can determine the current in $R_b$ as

$$I_{CB} = 180 - 15 = 165 \mu A$$

Also,

$$I_{CB} = I_{EB} = 165 \mu A$$

At this value of current we find that $V_{BE}$ is 588 mV, which is quite close to the value assumed. The base current of $Q_4$ is 165/200 = 0.8 $\mu A$, which can be added to the current in $R_b$ to determine the $Q_4$ current as

$$I_{CB} = I_{EB} = 15.8 \mu A$$

The voltage drop across the base–emitter junction of $Q_3$ can now be determined as

$$V_{BE} = V_T \ln \frac{I_{CB}}{I_s} = 588 mV$$

As mentioned in Section 9.3.5, the purpose of the $Q_1$-$Q_3$ network is to establish two $V_{BE}$ drops between the bases of the output transistors $Q_4$ and $Q_3$. This voltage drop, $V_{BE}$, can be now calculated as

$$V_{BE} = V_{FBE} + V_{FBB} = 588 + 530 = 1.118 V$$

Since $V_{BE}$ appears across the series combination of the base–emitter junctions of $Q_4$ and $Q_3$, we can write

$$V_{BE} = V_T \ln \frac{I_{CB}}{I_s} + V_T \ln \frac{I_{CB}}{I_s}$$

Using the calculated value of $V_{BE}$ and substituting $I_{CB} = I_{EB} = 3 \times 10^{-14} A$, we determine the collector currents as

$$I_{CB} = I_{EB} = 154 \mu A$$

This is the small signal at which the class A/B output stage is biased.

### 9.4.8 Summary

For future reference, Table 9.1 provides a listing of the values of the collector bias currents of the 741 transistors.

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### 9.5 SMALL-SIGNAL ANALYSIS OF THE 741

#### 9.5.1 The Input Stage

Figure 9.19 shows part of the 741 input stage for the purpose of performing small-signal analysis. Note that since the collectors of $Q_1$ and $Q_2$ are connected to a constant dc voltage, they are shown grounded. Also, the constant-current biasing of the bases of $Q_1$ and $Q_2$ is equivalent to having the common base terminal open-circuited.

The differential signal $v_i$ applied between the input terminals effectively appears across four equal emitter resistances connected in series—the bases of $Q_1$, $Q_2$, $Q_3$, and $Q_4$. As a result, emitter current flows as indicated in Fig. 9.19 with

$$i_e = \frac{V_f}{4r_e}$$

(9.68)

where $r_e$ denotes the emitter resistance of each of $Q_1$ through $Q_4$. Thus

$$r_e = \frac{V_f}{I_e} = \frac{25 mV}{9.5 \mu A} = 2.63 k\Omega$$

Thus the four transistors $Q_1$ through $Q_4$ supply the load circuit with a pair of complementary current signals $i_{e_1}$, as indicated in Fig. 9.19. The input differential resistance of the op amp can be obtained from Fig. 9.19 as

$$R_i = \frac{4(\beta_1 + 1)r_e}{\beta_1 + 1}$$

(9.69)

For $\beta_1 = 200$, we obtain $R_i = 2.1 M\Omega$.

**FIGURE 9.19** Small-signal analysis of the 741 input stage.
Proceeding with the input-stage analysis, we show in Fig. 9.20 the load circuit fed with the complementary pair of current signals found earlier. Neglecting the signal current in the base of Q₁, we see that the collector signal current of Q₁ is approximately equal to the input current io. Now, since Q₁ and Q₂ are identical and their bases are tied together, and since equal resistors are connected in their emitters, it follows that their collector signal currents must be equal. Thus the signal current in the collector of Q₁ is forced to be equal to io. In other words, the load circuit functions as a current mirror.

Now consider the output node of the input stage. The output current io is given by

\[ i_o = 2 i_{in} \]  

The factor of 2 in this equation indicates that conversion from differential to single-ended is performed without losing half the signal. The trick, of course, is the use of the current mirror to invert one of the current signals and then add the result to the other current signal (see Section 7.5).

Equations (9.68) and (9.70) can be combined to obtain the transconductance of the input stage, \( g_m \):

\[ g_m = \frac{I_b}{V_{be}} = \frac{g_m}{2r_e} \]  

Substituting \( r_e = 2.63 \text{ kΩ} \) and \( a = 1 \) yields \( g_m = 1.5 \text{ mA/V} \).

**EXERCISE**

9.34 For the circuit in Fig. 9.20, find in terms of \( i_i \) the signal voltage at the base of Q₁ (b) the signal current in the emitter of Q₁ (c) the signal current in the base of Q₂ (d) the signal voltage at the base of Q₂ (e) the base current of the signal current source \( i_i \).

**Ans.** (a) \( 0.63 \text{ kΩ} \times 0.01 = 0.0063 \) (b) \( 0.0063 \text{ kΩ} \times 1 \) (c) 3.94 mA

To complete our modeling of the 741 input stage we must find its output resistance \( R_o \). This is the resistance seen "looking back" into the collector terminal of Q₁ in Fig. 9.20. Thus \( R_o \) is the parallel equivalent of the output resistance of the current source supplying the signal current \( i_{in} \), and the output resistance of Q₁. The first component is the resistance looking into the collector of Q₁ in Fig. 9.19. Finding this resistance is considerably simplified if we assume that the common bases of Q₁ and Q₂ are at a virtual ground. This of course happens only when the input signal \( i_i \) is applied in a complementary fashion. Nevertheless, this assumption does not result in a large error.

Assuming that the base of Q₁ is at virtual ground, the resistance we are after is \( R_{out} \) indicated in Fig. 9.21(a). This is the output resistance of a common-base transistor that has a resistance \( r_e \) of Q₁ in its emitter. To find \( R_{out} \) we may use the following expression (Eq. 9.118):  

\[ R_{out} = r_o \left( 1 + \frac{R_o}{r_o} \right) \]  

Substituting \( r_o = r_e = 2.63 \text{ kΩ} \) and \( r_o = 30 \text{ kΩ} \) (where \( V_T = 50 \text{ V} \) and \( t = 9.5 \text{ pA} \) thus \( r_o = 5.26 \text{ MΩ} \)), neglecting \( r_o \) since it is \( (\beta + 1) \) times larger than \( R_e \), results in \( R_{out} = 10.5 \text{ MΩ} \).

The second component of the output resistance is that seen looking into the collector of Q₂ in Fig. 9.20. Although the base of Q₂ is not at virtual ground, we shall assume that the signal voltage at the base is small enough to make this approximation valid. The circuit then takes the form shown in Fig. 9.21(b), and \( R_{out} \) can be determined using Eq. 9.72 with \( R_e = R_o \).

Thus \( R_{out} = 18.2 \text{ MΩ} \).

Finally, we combine \( R_e \) and \( R_o \) in parallel to obtain the output resistance of the input stage, \( R_{out} = 6.7 \text{ MΩ} \).

Figure 9.22 shows the equivalent circuit that we have derived for the input stage.
EXAMPLE 9.3

We wish to find the input offset voltage resulting from a 2% mismatch between the resistances \( R_1 \) and \( R_2 \) in Fig. 9.13.

Solution

Consider the situation when both input terminals are grounded, and assume that \( R_1 = R \) and \( R_2 = R + \Delta R \), where \( \Delta R = 0.02R \). From Fig. 9.23 we see that while \( Q_1 \), still conducts a current equal to \( I \), the current in \( Q_2 \) will be smaller by \( \Delta I \). The value of \( \Delta I \) can be found from

\[
V_{GSX} + IR = V_{GSX} + (I - \Delta I)(R + \Delta R)
\]

Thus

\[
V_{GSX} + IR = V_{GSX} - \Delta I(R + \Delta R)
\]

The quantity on the left-hand side is in effect the change in \( V_{GSX} \) due to a change in \( I \) of \( \Delta I \). We may therefore write

\[
I = \frac{\Delta I}{R + \Delta R + \Delta V}
\]

Equations (9.73) and (9.74) may be combined to obtain

\[
\frac{\Delta V}{I} = \frac{\Delta R}{R + \Delta R + \Delta V}
\]

Substituting \( R = 1 \ k\Omega \) and \( \Delta V = 2.65 \ k\Omega \) shows that a 2% mismatch between \( R_1 \) and \( R_2 \) gives rise to an output current \( \Delta I = 5.5 \times 10^{-7} \). To reduce this output current to zero we have to apply an input voltage \( V_{IN} \) given by

\[
V_{IN} = \frac{\Delta I}{I} = \frac{5.5 \times 10^{-7}}{1 \ k\Omega} = 5.5 \mu\text{V}
\]

Substituting \( I = 9.5 \ \mu\text{A} \) and \( G_{mX} = 1/5.26 \ \mu\text{A/mV} \) results in the offset voltage \( V_{OS} = 0.3 \ \mu\text{V} \).

It should be pointed out that the offset voltage calculated is only one component of the input offset voltage of the 741. Other components arise because of mismatches in transistor characteristics. The 741 offset voltage is specified to be typically 2 mV.

**FIGURE 9.23** Input stage with both inputs grounded and a mismatch \( \Delta R \) between \( R_1 \) and \( R_2 \).

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**EXERCISES**

The purpose of this series of exercises is to determine the finite common-mode gain that results from a mismatch in the bias current of the input stage of the 741 op-amp. Figure 9.15 shows the input stage with an input common-mode signal \( \Delta V \) applied and with a mismatch \( \Delta R \) between the two resistors \( R_1 \) and \( R_2 \). Note that to simplify matters, we have opened the common-mode feedback loop and included a trans- resistance \( R_1 \), which is the resistance seen looking to the left of node 1 in the circuit of Fig. 9.13. Thus \( R_1 \) is the parallel equivalent of \( R_2 \), the output resistance of \( Q_2 \), and \( R_1 \), the output resistance of \( Q_2 \).

9.15 Show that the current \( I \) (Fig. 9.15) is given approximately by

\[
I = \frac{\Delta I}{R_1 + R_2 + \Delta R}
\]

9.16 Show that

\[
I = \frac{\Delta I}{R_1 + R_2 + \Delta R}
\]

9.17 Using the results of Exercises 9.15 and 9.16, and assuming that \( R_2 = (R_1 + R_2) \) and \( R_1 / R_2 (1 + \Delta I) \), show that the common-mode transconductance \( G_{CM} \) is given approximately by

\[
G_{CM} = \frac{I}{\Delta I} = \frac{R_1}{R_2} \Delta V
\]

**FIGURE 9.15**
9.5.2 The Second Stage

Figure 9.24 shows the 741 second stage prepared for small-signal analysis. In this section we shall analyze the second stage to determine the values of the parameters of the equivalent circuit shown in Fig. 9.25.

Input Resistance The input resistance $R_i$ can be found by inspection to be

$$R_i = \beta_1 (R_1 + R_2) / (\beta_1 + 1)$$

Substituting the appropriate parameter values yields $R_i = 4$ MΩ.

Transconductance From the equivalent circuit of Fig. 9.23, we see that the transconductance $G_{m2}$ is the ratio of the short-circuit output current to the input voltage. Short-circuiting the output terminal of the second stage (Fig. 9.24) to ground makes the signal current through the output resistance of $R_{out}$ zero, and the output short-circuit current becomes equal to the collector signal current of $Q_{1B}$ ($i_{c1}$). This latter current can be easily related to $u_{2}$ as follows:

$$i_{c1} = \frac{\alpha u_2}{r_{ce1} + R_2}$$

$$u_{2} = \frac{u_2}{(R_2/r_{ce1}) + r_{ce1}}$$

$$R_{out} = \left( \frac{R_2}{1 + r_{ce1} + R_2} \right)$$

These equations can be combined to obtain

$$G_{m2} = \frac{i_{c1}}{u_{2}}$$

which, for the 741 parameter values, is found to be $G_{m2} = 6.5$ mA/V.

Output Resistance To determine the output resistance $R_o$ of the second stage in Fig. 9.24, we ground the input terminal and find the resistance looking back into the output terminal. It follows that $R_o$ is given by

$$R_o = \frac{R_{10} + 1}{R_{10}}$$

where $R_{10}$ is the resistance looking into the collector of $Q_{1B}$ while its base and emitter are connected to ground. It can be easily seen that

$$R_{10} = r_{ce1}$$

For the 741 component values we obtain $R_{10} = 90.9$ kΩ.

The second component in Eq. (9.82), $R_{1}$, is the resistance seen looking into the collector of $Q_{1B}$ as indicated in Fig. 9.26. Since the resistance between the base of $Q_{1B}$ and ground is relatively small, one can considerably simplify matters by assuming that the base is grounded. Doing this, we can see Eq. (9.82) to determine $R_{1}$.

For our case the result is $R_{1} = 787$ kΩ. Combining $R_{10}$ and $R_{1}$ in parallel yields $R_{o} = 81$ kΩ.

Thévenin Equivalent Circuit The second-stage equivalent circuit can be converted to the Thévenin form, as shown in Fig. 9.27. Note that the stage open-circuit voltage gain is

$$A_{v2} = G_{m2} R_o$$

FIGURE 9.24 The '741 second stage prepared for small-signal analysis.

FIGURE 9.25 Definition of $R_{o}$. 

FIGURE 9.26 Small-signal equivalent circuit model of the second stage.
9.5.3 The Output Stage

The 741 output stage is shown in Fig. 9.28 without the short-circuit-protection circuitry. The stage is driven by the second-stage transistor Q6, and loaded with a 240Ω resistance. The circuit is of the AB class (Section 9.3.5), with the network composed of \( Q_{10}, Q_{20}, \) and \( R_{20} \) providing the bias of the output transistors Q6, and Q10. The use of this network rather than two diode-connected transistors in series enables Biasing the output transistors at a low current (0.15 mA) in spite of the fact that the output devices are three times as large as the standard devices. This is obtained by arranging that the current in Q10 is very small and thus its \( V_{CE} \) is also small. We analyzed the dc bias in Section 9.4.7.

Another feature of the 741 output stage worth noting is that the stage is driven by an emitter follower \( Q_{10} \). As will be shown, this emitter follower provides added buffering, which makes the open-circuit gain almost independent of the parameters of the output transistors.

Output Voltage Limits

The maximum positive output voltage is limited by the saturation of current-source transistor \( Q_{10} \). Thus

\[
V_{OUT_{max}} = V_C - V_{BE1} - V_{CE1}
\]

which is about 1 V below \( V_C \). The minimum output voltage (i.e., maximum negative amplitude) is limited by the saturation of \( Q_{10} \). Neglecting the voltage drop across \( R_{20} \), we obtain

\[
V_{OUT_{min}} = -V_T + V_{BE2} + V_{T2} + V_{BE1}
\]

which is about 1.5 V above \(-V_T\).

Small-Signal Model

We shall now carry out a small-signal analysis of the output stage for the purpose of determining the values of the parameters of the equivalent circuit model shown in Fig. 9.29. Note that this model is based on the general amplifier equivalent circuit presented in Table 5.5 as "Equivalent Circuit C." The model is shown fed by \( v_{IN} \), which is the open-circuit output voltage of the second stage. From Fig. 9.27, \( v_{IN} \) is given by

\[
v_{IN} = -G_{m2}R_{20}V_{T2}
\]

where \( G_{m2} \) and \( R_{20} \) were previously determined as \( G_{m2} = 6.5 \text{ mA/V} \) and \( R_{20} = 81 \text{ kΩ} \). Resistance \( R_{20} \) is the input resistance of the output stage determined with the amplifier loaded with \( R_{1} \). Although the effect of loading an amplifier stage on its input resistance is negligible in the input and second stages, this is not the case in general in an output stage. Defining \( R_{20} \) in this manner (see Table 5.5) enables correct evaluation of the voltage gain of the second stage, \( A_2 \), as

\[
A_2 = \frac{v_{OUT}}{v_{IN}} = -\frac{G_{m2}R_{20}^2}{R_{1} + R_{20}}
\]
To determine $R_{o2}$, assume that one of the two output transistors—say, $Q_2$—is conducting a current of, say, 5 mA. It follows that the input resistance looking into the base of $Q_{o2}$ is approximately $R_{o2}$. Assuming $R_{o2} = 50$, for $R_{o} = 2 \, \text{k}\Omega$ the input resistance of $Q_{o2}$ is 100 k\Omega. This resistance appears in parallel with the series combination of the output resistance of $Q_{o2}, r_{o2} = 280 \, \text{k}\Omega$ and the resistance of the $Q_{o1}, Q_{o2}$ network. The latter resistance is very small (about 160 \Omega; see later Exercise 9.26). Thus the total resistance in the emitter of $Q_{o2}$ is approximately (100 k\Omega/280 k\Omega) or 74 k\Omega and the input resistance $R_{o1}$ is given by

$$R_{o1} = R_{o2} \times 74 \, \text{k}\Omega$$

which for $R_{o2} = 50$ is $R_{o1} = 3.7 \, \text{M}\Omega$. Since $R_{o1} = 81 \, \text{k}\Omega$, we see that $R_{o1} \gg R_{o2}$ and the value of $R_{o1}$ will have little effect on the performance of the op amp. We can use the value obtained for $R_{o1}$ to determine the gain of the second stage using Eq. (9.87) as $A_2 = -315 \, \text{V/V}$. The value of $A_1$ will be needed in Section 9.6 in connection with the frequency-response analysis.

Continuing with the determination of the equivalent circuit model parameters, we note from Fig. 9.29 that $G_{o1}$ is the open-circuit overall voltage gain of the output stage,

$$G_{o1} = \frac{V_{o1}}{V_{o1}}$$

(9.88)

With $R_{o1} \rightarrow \infty$, the gain of the emitter-follower output transistor ($Q_{o2}$ or $Q_{o1}$) will be nearly unity. Also, with $R_{o1} \rightarrow \infty$ the resistance in the emitter of $Q_{o1}$ will be very large. This means that the gain of $Q_{o2}$ will be nearly unity and the input resistance of $Q_{o2}$ will be very large. We thus conclude that $G_{o1} \rightarrow 1$.

Next, we shall find the value of the output resistance of the op amp, $R_{o2}$. For this purpose refer to the circuit shown in Fig. 9.30. In accordance with the definition of $R_{o2}$, the input source feeding the output stage is grounded, but its resistance (which is the output resistance of the second stage, $R_{o2}$) is included. We have assumed that the output voltage $V_{o}$ is negative, and thus $Q_{o2}$ is conducting most of the current. Transistor $Q_{o1}$ has therefore been eliminated. The exact value of the output resistance will of course depend on which transistor ($Q_{o1}$ or $Q_{o2}$) is conducting and on the value of load current. Nevertheless, we wish to find an estimate of $R_{o2}$.

As indicated in Fig. 9.30, the resistance seen looking into the emitter of $Q_{o2}$ is

$$R_{o2} = \frac{V_{o1}}{I_{o1}}$$

(9.89)

Substituting $R_{o2} = 81 \, \text{k}\Omega$, $A_{o2} = 50$, and $r_{o2} = 25.0 \, \text{M}\Omega$ yields $R_{o2} = 1.73 \, \text{k}\Omega$. This resistance appears in parallel with the series combination of $C_{o2}$ and the resistance of the $Q_{o2}, Q_{o2}$ network. Since $r_{o2}$ alone (0.28 M\Omega) is much larger than $R_{o2}$, the effective resistance between the base of $Q_{o2}$ and ground is approximately equal to $R_{o2}$. Now we can find the output resistance $R_{o2}$:

$$R_{o2} = R_{o2} + r_{o2}$$

(9.90)

For $R_{o2} = 50$, the first component of $R_{o2}$ is 34 \Omega. The second component depends critically on the value of output current. For an output current of 5 mA, $r_{o2}$ is 5 \Omega and $R_{o2}$ is 39 \Omega. To this value we must add the resistance $R_{o2}$ (27 \Omega) (see Fig. 9.13), which is included for short-circuit protection. The output resistance of the 741 is specified to be typically 75 \Omega.

**EXERCISES**

28. Using the simple input model for each of the two transistors $Q_1$ and $Q_2$ in Fig. 9.26. Find the small-signal resistance between $A$ and $B$. Draw: From Table 9.1, $r_{o1} = 65 \, \mu$A and $r_{o2} = 16 \, \mu$A.

**Fig. 9.26**
Output Short-Circuit Protection If the op-amp output terminal is short-circuited to one of the power supplies, one of the two output transistors could conduct a large amount of current. Such a large current can result in sufficient heating to cause burnout of the IC (Chapter 14). To guard against this possibility, the 741 op amp is equipped with a special circuit for short-circuit protection. The function of this circuit is to limit the current in the output transistors in the event of a short circuit.

Refer to Fig. 9.13. Resistance \( R_3 \) together with transistor \( Q_3 \) limits the current that would flow out of \( Q_2 \) in the event of a short circuit. Specifically, if the current in the emitter of \( Q_2 \) exceeds about 20 mA, the voltage drop across \( R_3 \) exceeds 540 mV, which turns \( Q_3 \) on. As \( Q_3 \) turns on, its collector then diverts some of the current supplied by \( Q_2 \) thus reducing the base current of \( Q_2 \). This mechanism thus limits the maximum current that the op amp can source (i.e., supply from the output terminal in the forward direction) to about 20 mA.

Limiting of the maximum current that the op amp can sink, and hence the current through \( Q_{ON} \) is done by a mechanism similar to the one discussed above. The relevant circuit is composed of \( Q_2 \), \( Q_{ON} \), \( Q_{OFF} \), and \( Q_{OFF} \). For the components shown, the current in the forward direction is limited also to about 20 mA.