MMIC Design and Technology

Fabrication of MMIC

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Lecture 2 Fabrication Processes
Process Choice

• Substrate
  – Mobility & Peak Velocity: Frequency Response
  – Band-Gap Energy: Breakdown Voltage (Power-Handling)
  – Resistivity: Loss and Q of the Passives

• Transistor
  – Field-Effect Transistors
  – Bipolar Transistors
# Most Commonly Used Semiconductors

<table>
<thead>
<tr>
<th>Material</th>
<th>Electron Mobility (cm²/Vs)</th>
<th>Peak Velocity (10⁷ cm/s)</th>
<th>Frequency Range (GHz)</th>
<th>Noise Figure</th>
<th>Gain</th>
<th>Maturity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>900 – 1,100</td>
<td>0.3 – 0.7</td>
<td>&lt; 20</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Mature 12-in Wafer</td>
</tr>
<tr>
<td>SiGe</td>
<td>2,000 – 300,000</td>
<td>0.1 – 1.0</td>
<td>10 – 40</td>
<td>Lower</td>
<td>Better</td>
<td>Mature 6-in Wafer</td>
</tr>
<tr>
<td>SiC</td>
<td>500 – 1,000</td>
<td>0.15 – 0.2</td>
<td>15 – 20</td>
<td>Poor</td>
<td>Lower</td>
<td>4-in Wafer</td>
</tr>
<tr>
<td>GaAs</td>
<td>5,500 – 7,000</td>
<td>1.6 – 2.3</td>
<td>75</td>
<td>Lower</td>
<td>Higher</td>
<td>3, 4, 6-in Wafers</td>
</tr>
<tr>
<td>GaN</td>
<td>400 – 1,600</td>
<td>1.2 – 2.0</td>
<td>20 – 30</td>
<td>Poor</td>
<td>Lower</td>
<td>2-in Wafer</td>
</tr>
<tr>
<td>InP</td>
<td>10,000 – 12,000</td>
<td>2.5 – 3.5</td>
<td>115</td>
<td>Lower</td>
<td>Higher</td>
<td>2-in Wafer</td>
</tr>
</tbody>
</table>

Lecture 2 Fabrication Processes
# Transistors

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>SiGe HBT</th>
<th>GaAs/InP HBT</th>
<th>MESFET</th>
<th>HEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator</td>
<td>—</td>
<td>✓</td>
<td>✓</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Mixer</td>
<td>—</td>
<td>✓</td>
<td>✓</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LNA</td>
<td>—</td>
<td>✓</td>
<td>✓</td>
<td>—</td>
<td>✓</td>
</tr>
<tr>
<td>Power Amplifier</td>
<td>—</td>
<td>—</td>
<td>✓</td>
<td>—</td>
<td>✓</td>
</tr>
<tr>
<td>Switch</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Digital</td>
<td>✓</td>
<td>✓</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Lecture 2  Fabrication Processes
MMIC

Product Data Sheet

2-20 GHz Wideband AGC Amplifier

Key Features and Performance
- 0.5 um MESFET Technology
- 9 dB Nominal Gain
- 3.5 dB NF Typical Midband
- 17.5 dBm Nominal Pout @ P1dB
- Bias 5-8V @ 60 mA
- Dimensions 3.4 x 2.0 x 0.1 mm

Primary Applications
- Wideband Gain Block / LN Amplifier
- X-Ku Point to Point Radio
- IF & LO Buffer Applications

Chip Dimensions: 3.4 x 2.0 x 0.1 mm

Lecture 2  Fabrication Processes
MMIC Product Development Process

Lecture 2  Fabrication Processes
Why GaAs

• High Electron Mobility
  – High frequency operation

• Intrinsic GaAs is Semi-Insulating
  – Well suited for use as a substrate for stripline and passives
  – High Q

• Large Band Gap 1.4eV
  – High voltage = higher power
  – Radiation hard

Lecture 2  Fabrication Processes
MMIC Production Process

Lecture 2  Fabrication Processes

Features
- 0.6 \( \mu \text{m} \) Gate Length MESAFT Process
- 4 Active Devices:
  - Power & Gain D-FETs
  - E-FET
  - Schottky-Barrier Diodes
- High Density Interconnects:
  - 2 Global and 1 local
  - 6 \( \mu \text{m} \) total thickness
- High-Q Passives
- Bulk & Thin Film Resistors
- High Value Capacitors
- Dielectric Encapsulated Metals
- Planarized Surface; simplified plastic packaging
- Substrate Vias Available
- Volume Production Process
- Validated Models and Design Support
MESFET

Source and Drain Ohmic Contacts

Active Layer N/P

Plated Via Hole

Semi-Insulating GaAs

Back Plane Metal

Etch to Produce Mesa

Lecture 2 Fabrication Processes
HBT Process

Production Process

TQHBT3
InGaP HBT Foundry Service

Features
- 2- and 3-um emitter widths
- >22 dB MAG @ 6 GHz, with 3-um emitters
- Amplifier Ruggedness: VSWR 70:1 @ 5 V supply
- High Linearity in PA applications
- InGaP Emitter Process for High Reliability and Thermal Stability
- Base Etch Stop for Uniformity
- MOCVD Epitaxy
- High Density Interconnects:
  - 2 Global, 1 Local
  - Over 6 μm Total Thickness
- Dielectric Encapsulated Metals
- Thick Metal Interconnects:
  - Enhanced Thermal Management
  - Minimum Die Size

Lecture 2  Fabrication Processes
Resistor

Lecture 2  Fabrication Processes
Capacitors

Lecture 2  Fabrication Processes
Process list

Wafer fabrication
  Wet cleans
  Photolithography
  Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
  Dry Etching
  Wet Etching
  Plasma ashing
  Thermal treatments
  Rapid thermal anneal
  Furnace anneals
  Oxidation
  Chemical vapor deposition (CVD)
  Physical vapor deposition (PVD)
  Molecular beam epitaxy (MBE)
  Electroplating
  Chemical mechanical polish (CMP)

Wafer testing (where the electrical performance is verified)
  Wafer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card)
  Die preparation
  Wafer mounting
  Die cutting

Lecture 2  Fabrication Processes
Lithography

Light Source

Wavelength $\lambda$

Numerical aperture $NA$

Resolution $s$

Mask

Photo-resist

Wafer in Process

$s = \frac{k\lambda}{NA}$

$k$ is a constant of the process

Lecture 2 Fabrication Processes
Lithography

- Optical
- UV
- Deep UV, X-UV
- Electron Beam
  - Voltage $U$
- Direct write e-beam
  - Electronically scanned
  - No mask

\[ \lambda = \frac{h}{\sqrt{2m_0eU}} \frac{1}{\sqrt{1 + \frac{eU}{2m_0c^2}}} \]
Ion Implantation

Selectively implant impurities
Create n or p type semiconductor regions

Lecture 2 Fabrication Processes
Ion etch

Selectively remove material
Dry Etch Process

Ion beam or Plasma

Patterned Photo-resist

Wafer in Process

Lecture 2 Fabrication Processes
Wet Etch

Selectively remove material
Chemical Process

Chemical Bath

Patterned Photo-resist

Wafer in Process

Lecture 2 Fabrication Processes
MBE

• Molecular Beam Epitaxy
  – Selectively grow layers of material
• A beam of atoms or molecules produced in high vacuum
  – Deposited on wafer in a pattern defined by photoresist
CVD

- Chemical Vapor Deposition
  - A chemically produced vapor is deposited on the wafer
  - Pattern is defined by photoresist
PVD

• Physical Vapor Deposition
  – A vapor is produced by evaporation or sputtering
  – Deposited on wafer
  – Pattern defined by Photoresist
Electroplate

• Electroplating is an electrochemical process used to add metal
• Plating used to increase thickness of metal layers
Backside Processing

- Via Holes
- Back Plane Metal
Thermal Annealing

• High temperature processing to remove stress between process steps
Example

Apply Resist
Expose Resist
Remove Resist
Isolation Implant  Channel Dope  Contact Dope
Remove Resist

MASK 2
MASK 1
MASK 0

Semi-Insulating GaAs

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