Try to simulate circuits using SPICE (if possible) and compare the results with your answers. The extra problems are stared (*) and need not to be handed in.

1. A balanced monolithic series-shunt feedback amplifier is shown in Fig. 1.
   (a) If the common-mode input voltage is zero, calculate the bias current in each device. Assume that $\beta$ is large.
   (b) Calculate the voltage gain, input impedance, output impedance, and loop gain of the circuit at low frequencies using the following data: $\beta = 100$ $r_b = 50 \Omega$ $V_A = \infty$ $V_{BE \text{ on}} = 0.7V$

2. A CMOS feedback amplifier is shown in Fig. 2. If the dc input voltage is zero, calculate the overall gain $v_o/v_i$ and the output resistance. Compare your answer with a SPICE simulation. Use $\mu_n C_{ox} = 60 \mu A/V^2$ $= 30 \mu A/V^2$ $V_{Th} = 0.8V$ $V_{Tr} = -0.8V$ $\lambda_n = |\lambda_p| = 0.03 V^{-1}$
3. A simplified output stage of 741 is shown in Fig. 3. Assume that for all transistors $\beta_{npn} = 200$; $\beta_{pnp} = 50$; $V_{on} = 0.7$; $V_{sat} = 0.2$; $I_s = 10^{-4}A$ ($I_s1 \neq I_s$). The bias points for $q_1$ and $q_2$ are shown in Fig 3.

a) Find $V_o^{+\text{max}}$ and $V_o^{-\text{max}}$ for $R_L = 10k\Omega, 1k\Omega, 200\Omega$.

b) For $R_L = 1k\Omega$ what is the maximum power that can be delivered to the load without considerable distortion? Under such conditions what is efficiency of the push-pull stage? (for sinusoidal voltage)

c) What is the maximum power dissipation of $q_7$ and $q_8$. (for sinusoidal voltage)

d) If the maximum power dissipation of $q_7$ and $q_8$ is limited to 100mW, find $R_L$ and efficiency under such conditions. (for sinusoidal voltage)

e) If $V_o = -10V$ and $R_L = 1k\Omega$, find currents for all transistors. (Note that this is a DC voltage at output!)

Figure 3