Use ITRS 2011 available at public.itrs.net, to answer the following questions.

1. Minimum Feature Size
- What is the difference between "Flash 1/2 pitch", "DRAM 1/2 pitch", "MPU 1/2 pitch", "Printed Gate Length", and "Physical Gate Length"?
- Make a plot comparing these parameters as a function of year.

2. Oxide Thickness
- Make a plot of the \( T_{ox} \) “transistor oxide thickness” and “gate leakage per unit micron” as a function of year.

3. Supply Voltage (\( V_{dd} \))
- Make a plot of \( V_{dd} \) projections” and “the ratio of the threshold voltage (\( V_T \)) to the supply voltage (\( V_{dd} \))” for different processors as a function of year.

4. Drive Current (\( I_{on} \)) vs. Off Current (\( I_{off} \))
- Make a plot of the \( I_{on} \) current (in mA/\( \mu \)m) as a function of year.
- Make a plot of the \( I_{off} \) current (in nA/\( \mu \)m) as a function of year.
- Make a plot of the \( I_{on}/I_{off} \) as a function of year.

5. CV/I Metric, Clock Frequency
- Make a plot of the “\( t = CV/I \) metric” and “\( T = 1/f \)” as a function of year. (\( t = CV/I \) is the intrinsic gate delay and \( f \) is the on-chip local clock)

6. Chip Size, Power Dissipation
- Make a plot of the \( P \) “power dissipation” projected for the next generations. Given that you know the supply voltage projections, find the “\( I_{avg} \) =average current per gate” for different generations. Knowing that “\( I_G \) =current per logic gate” is \( k \) times “average current per gate” plot \( I_G \) as a function of year for \( k = 10 \).
- Make a plot of the “\( A=chip \) size” at production as a function of year. Knowing the number of transistors (\( N_T \)) for each generation and assuming that (by average) each gate consists of 6 transistors, relate “\( G_p=gate \) pitch” to \( A \) and \( N_T \). Plot \( G_p \) as a function of year.
- Estimate the ratio of the power dissipation in the wire to the power dissipation in the gates (\( P_w/P_G \)). You may use the total wire length given in the ITRS and assuming that the wiring structure is as shown in Figure 1.

7. Wire Delay
- Wire RC delay is defined as \( t_W = RC \) where \( R \) and \( C \) are resistance and capacitance of the wire. Consider a structure as shown in Figure 1. Assume length of the wire is \( L=100 \mu \)m and \( w \) is the minimum wire size for each technology generation. Plot \( t_W/t \) as a function of year.
- \( L^* \) is defined as the length of the wire at which \( t_W \) is equal to \( t = CV/I \) for that technology generation. Plot \( L^* \) vs. year. Assume repeater insertion and recalculate \( L^* \) and plot it on the previous curve. (Use data in ITRS to extract \( R_0 \) and \( C_0 \) for the repeater insertion)

(Extra credit) 8. Read “Executive Summary” of the ITRS 2011 and list all difficult challenges related to “interconnect.” Specifically highlight those related to the “modeling.”
(Extra credit) 9. Think of a method to plot as many important information as possible on a single plot (one possible idea could be: plotting all important variables vs. year, normalized to their value in the starting generation). Make such a plot based on the variables that you think contain the most important data for each technology generation.