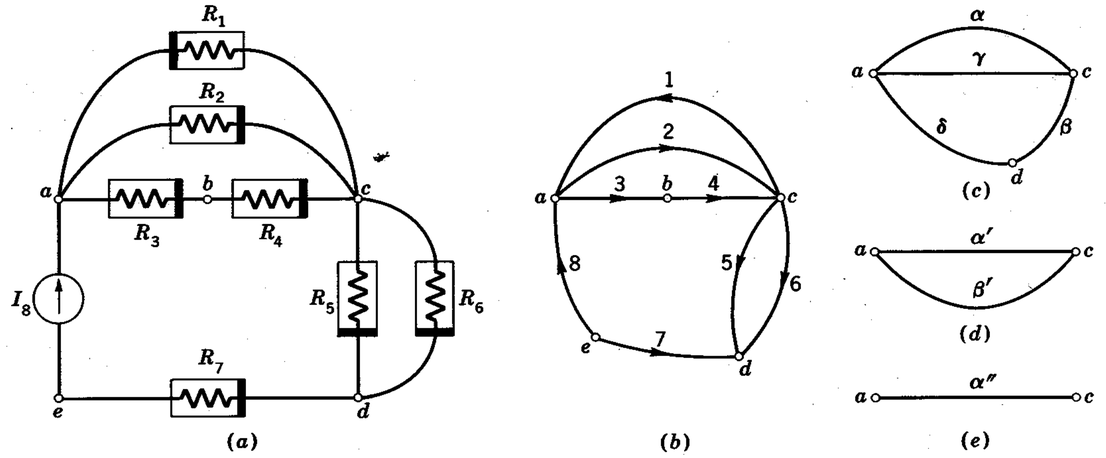


Fig. 6-1. If each set of series branches and each set of parallel branches of a series-parallel network is replaced repeatedly by a single branch, the resulting graph must reduce to one branch.

in Fig. 6-2*a*. The resulting graph shown in Fig. 6-2*b* can be reduced to that shown in Fig. 6-2*c*, but no further. Hence, this network is non-series-parallel.[1]

The class of series-parallel networks is important not only because many practical networks belong to it, but also because it is especially amenable to a graphical analysis. We shall present several simple, graphical procedures for determining the operating points, the DP plots, and the TC plots of any series-parallel networks. These basic procedures will then be generalized to analyze an important class of non-series-parallel networks. In particular, we shall formulate a number of graphical procedures for analyzing a subclass of nonlinear resistive networks containing two-terminal resistors, three-terminal resistors, and dc independent sources. However, we shall not include controlled sources in this chapter, because so far, no general *graphical* procedure is known for analyzing nonlinear networks containing controlled sources.

Exercise 1: Classify each of the following networks according to whether it is series-parallel or not: (*a*) the network in Fig. 4-2*a*; (*b*) the network in Fig. 4-4*a*; (*c*) the network in Fig. 4-7*a*.

Exercise 2: (*a*) Show that any network of two-terminal elements containing no more than three nodes is series-parallel. (*b*) Show that any "ladder" network is series-parallel.

[1] A network which contains one or more three-terminal elements is also non-series-parallel because the terms "series" and "parallel" are meaningful only for interconnections between two-terminal elements.

6-2 GRAPHICAL DETERMINATION OF THE OPERATING POINT

In order to determine the operating point, we must solve for the set of voltages and currents which simultaneously satisfies the equations of motion of a given dc-resistive nonlinear network. This task in concept consists of systematically eliminating one or more variables from the system of equations of motion, and

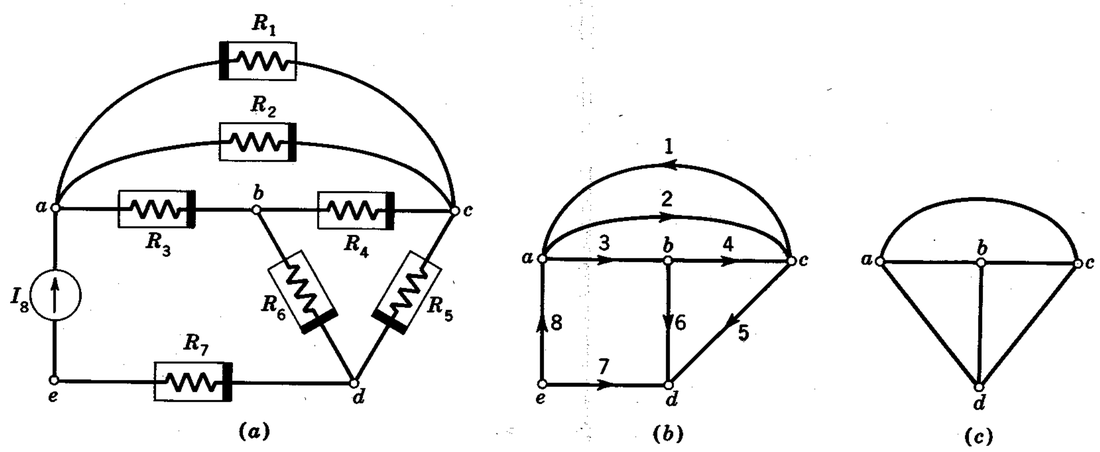


Fig. 6-2. An example showing how a non-series-parallel network fails the test.

eventually reducing the system of equations into one equation in one unknown. However, as was pointed out in Chap. 5, the equations of motion of most practical dc-resistive nonlinear networks usually contain functions specified graphically in the form of curves. Hence, the approach described above is not directly applicable. Instead, we apply the graphical approach, which is actually the implementation of the conceptual approach in graphical form. In this section, we shall present several graphical procedures for determining the operating points of two basic network configurations. Most of these procedures are used to carry out graphically the elimination and substitution operations required in the solution of nonlinear equations.

6-2-1 BASIC NETWORK CONFIGURATION 1, INTERCONNECTION BETWEEN 2 TWO-TERMINAL RESISTORS

The simplest network configuration involving two nonlinear resistors is shown in Fig. 6-3*a*. One of the two resistors is commonly referred to as the load. For convenience, we shall usually refer to the resistor with the simpler[1] *v-i* curve as the load. For example, suppose resistors R_1 and R_2 are characterized, respectively, by the curves shown in Fig. 6-3*b* and *c*. Then R_2 will be referred to as the load since its *v-i* curve is simpler than that for resistor R_1. To find the operating point of this network, we must first write the following equations of motion:

Equations from the laws of elements[2]

$$f_1(i_1,v_1) = 0 \qquad (6\text{-}1a)$$

$$f_2(i_2,v_2) = 0 \qquad (6\text{-}1b)$$

[1] A curve is said to be simpler than another if it can be approximated by fewer piecewise-linear segments.

[2] In order to include both current- and voltage-controlled resistors, as well as multivalued resistors, we have chosen the notation $f_1(i_1,v_1)=0$ and $f_2(i_2,v_2)=0$ to denote the *v-i* curves of R_1 and R_2, respectively.

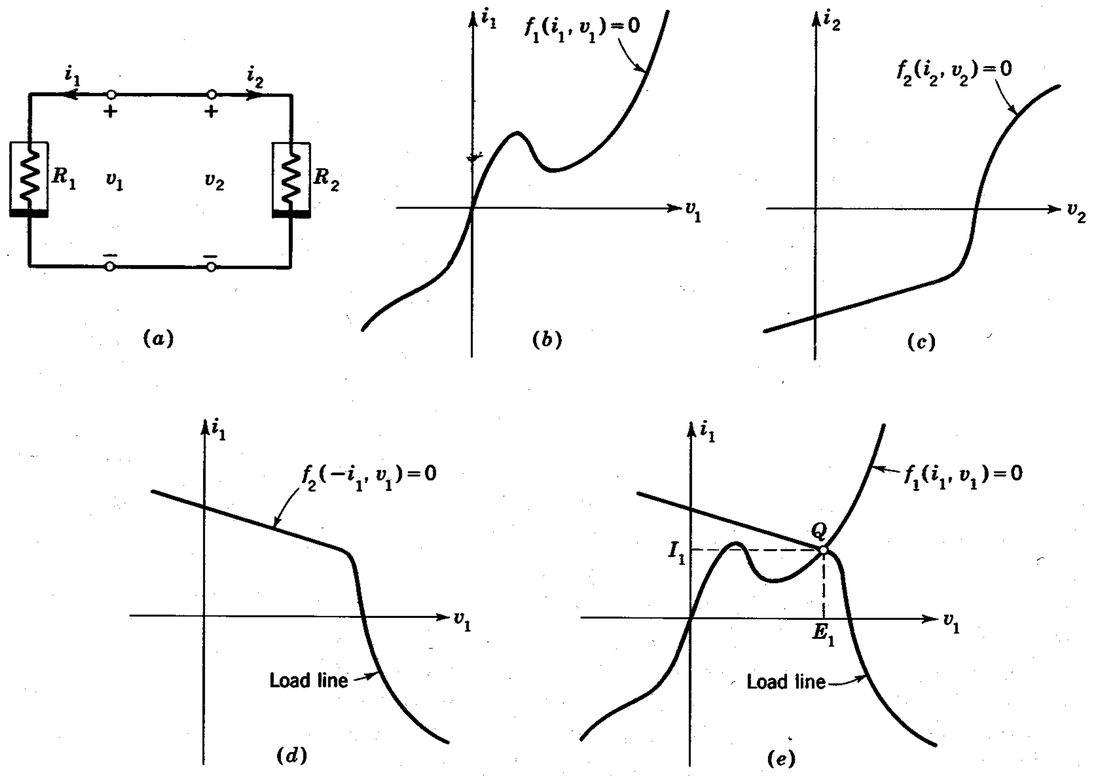


Fig. 6-3. The graphical procedure for determining the operating point of a resistive nonlinear network in basic configuration 1 by the load-line method.

Equations from the laws of interconnection

$$v_2 = v_1 \tag{6-1c}$$

$$i_2 = -i_1 \tag{6-1d}$$

Substituting Eqs. (6-1*c*) and (*d*) into Eqs. (6-1*a*) and (*b*), we obtain

$$f_1(i_1,v_1) = 0 \tag{6-2a}$$

$$f_2(-i_1,v_1) = 0 \tag{6-2b}$$

The operating point can be found by solving for i_1 and v_1 from these equations. Equation (6-2*a*) is still the v_1-i_1 curve shown in Fig. 6-3*b*. However, Eq. (6-2*b*) represents a curve related to the v_2-i_2 curve in Fig. 6-3*c* but with the current coordinates reversed in sign. Hence, Eq. (6-2*b*) represents a curve obtained by reflecting the v_2-i_2 curve in Fig. 6-3*c* with respect to the v_2 axis, as shown in Fig. 6-3*d*. Since the operating point must satisfy both Eqs. (6-2*a*)

and (*b*), it can be found by superimposing the curve $f_2(-i_1,v_1) = 0$ (Fig. 6-3*d*) on top of the curve $f_1(i_1,v_1) = 0$ (Fig. 6-3*b*). The point where the curves intersect is the operating point. In Fig. 6-3*e*, this point is labeled Q and has the coordinates (E_1,I_1) in the v_1-i_1 plane. Once E_1 and I_1 are found, the remaining coordinates can be determined from Eqs. (6-1*c*) and (*d*), namely, $i_2 = -I_1$ and $v_2 = E_1$. Thus, the operating point is completely specified by the four values $(E_1,E_1,I_1,-I_1)$. The reflected curve shown in Fig. 6-3*d* is usually called the *load line,* because it is obtained from the *v-i* curve of the load. Accordingly, the above method is often referred to as the *load-line method.*

There is an alternate and perhaps more intuitive way of interpreting the load-line method. Instead of substituting Eqs. (6-1*c*) and (*d*) into Eq. (6-1*b*), let us enclose R_2 by a black box and define the terminal variables i_3 and v_3 as shown in Fig. 6-4*a*. Since $i_3 = -i_2$ and $v_3 = v_2$, the v_3-i_3 curve of the black box must be as shown in Fig. 6-4*b*. Observe that this curve is identical with the load line in Fig. 6-3*d*. Since the laws of interconnection for this network are given by $i_1 = i_3$ and $v_1 = v_3$, the operating point is simply the intersection between the v_1-i_1 curve of R_1 and the v_3-i_3 curve of the black box, as shown in Fig. 6-4*c*. In both cases, we obtain the same answers, as they should be. These two methods are obviously applicable to any network which can be redrawn as an interconnection between two black boxes in basic configuration 1, provided the DP plot of each black box is given or can be determined.

EXAMPLES

1. Consider the simple switching circuit shown in Fig. 6-5*a* and the tunnel diode v_1-i_1 curve shown in Fig. 6-5*b*. The black box

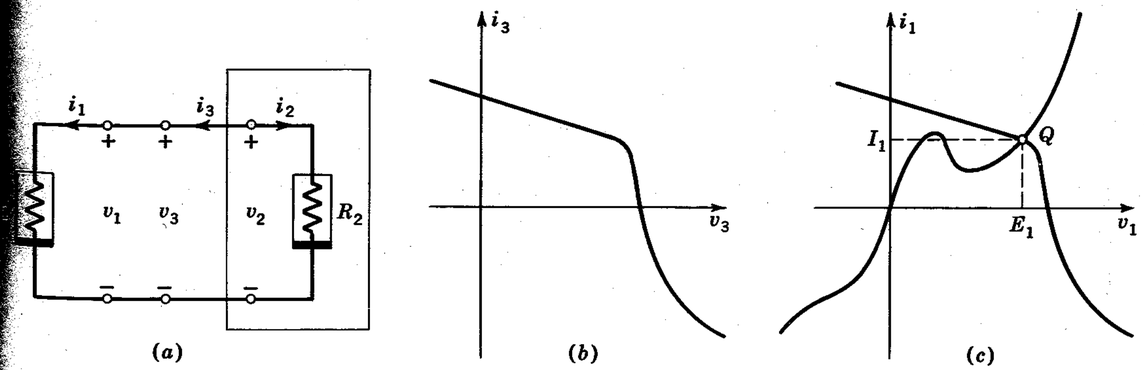


Fig. 6-4. An alternate method for finding the operating point of a network in basic configuration 1.

representing the resistor-battery combination is represented by the DP plot

$$v_2 = Ri_2 + E = 500i_2 + 0.45$$

The load line is obtained by substituting $i_2 = -i_1$ and $v_2 = v_1$ in this equation to obtain

$$v_1 = -(500)i_1 + 0.45$$

The load line corresponding to this equation is drawn on top of the v_1-i_1 curve in Fig. 6-5*b*. Observe that there are three operating points, namely, Q_1:(v_1=0.05 volt, i_1=0.8 ma); Q_2:(v_1=0.135 volt, i_1 = 0.6 ma); and Q_3:(v_1 = 0.35 volt, i_1 = 0.2 ma).

Since the load consisting of a linear resistor R in series with a battery E is quite common in practice, it is worthwhile to be able to draw the corresponding load line by inspection. This can be done by remembering that the voltage intercept is equal to E, and the current intercept is equal to E/R. Observe that the effect of changing the value of the voltage E is simply to move the load line parallel to itself, and the effect of changing the value of R is to change the slope of the load line. Hence if the value of E in Fig. 6-5*a* is too large or too small, there will be only one operating point. Similarly, if the load line is exactly tangent to the middle portion of the tunnel diode v_1-i_1 curve, there will be two operating points. In practice, of course, only one operating point is observable at any one time. Which of these *possible* operating points is actually attained at a given time is decided by the parasitic elements which are invariably present. The methods for obtaining this important information are presented in Part 3 of this book.

It is important to recognize that the load-line method is not restricted to a network containing only two resistors, a most unlikely if not trivial situation. On the contrary, the use-

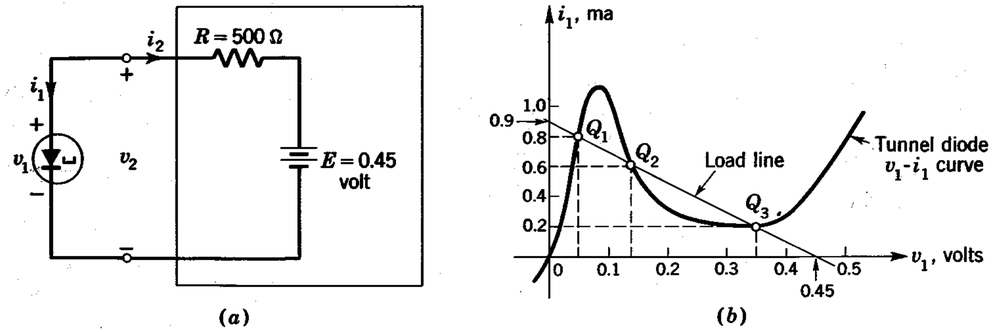


Fig. 6-5. A simple tunnel-diode switching circuit.

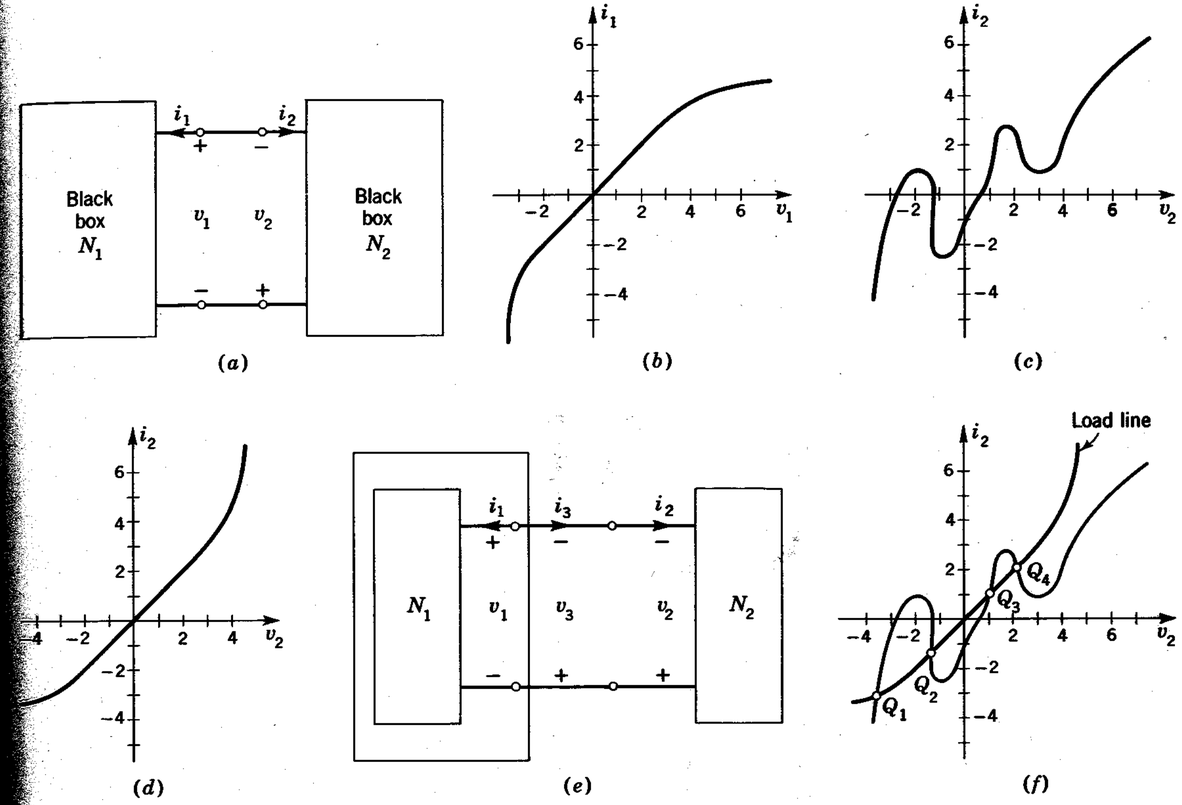


Fig. 6-6. The graphical procedure for determining the operating point of two resistive black boxes connected in the form of basic configuration 1 by the load-line method.

fulness of the load-line method lies in the fact that there are many practical networks whose elements can be combined into two separate black boxes in the form of basic configuration 1.

2. Consider two black boxes N_1 and N_2 connected as shown in Fig. 6-6*a*. Each black box may contain an arbitrary interconnection of other resistive network elements such as zener diodes, transistors, and gyrators. As far as we are concerned, however, only the external DP plots of N_1 and N_2 are necessary for determining the operating points. Assume for the time being that these have been found and are given in Fig. 6-6*b* and *c*, respectively.[1] Notice that although this network is in the form of basic configuration 1, the references of the current and voltage variables (for which the DP plots are based) are not identical with those shown in Fig. 6-3*a*. Since the v_1-i_1 curve is simpler, the black box N_1 is chosen to be the load. The laws of interconnection are $i_1 = -i_2$ and $v_1 = -v_2$. Hence, the load line is obtained by reflecting the v_1-i_1 curve, first with respect

[1] For reasons that will soon be obvious, it may be more convenient to choose a particular set of reference voltage polarity and reference current direction in the process of determining the DP plot of each black box. Hence, we must always watch for the references associated with a given DP plot.

to the v_1 axis, and then with the i_1 axis. The net effect is equivalent to a 180° rotation with respect to the origin as shown in Fig. 6-6*d*.

The load line in Fig. 6-6*d* could also be obtained by redefining a new set of terminal variables i_3 and v_3 for the black box N_1 as shown in Fig. 6-6*e*. Since $i_3 = -i_1$ and $v_3 = -v_1$, the new v_3-i_3 curve coincides with the load line in Fig. 6-6*d*. In either case, the intersections between the load line, or the v_3-i_3 curve, with the v_2-i_2 curve give the four operating points Q_1, Q_2, Q_3, and Q_4 shown in Fig. 6-6*f*. Using the voltage and current values at each operating point, it is possible to determine the voltage and current solutions of the network elements inside N_1 and N_2. The procedure for doing this will be discussed in the next chapter.

6-2-2 BASIC NETWORK CONFIGURATION 2, INTERCONNECTION BETWEEN 2 TWO-TERMINAL RESISTORS AND A THREE-TERMINAL RESISTOR

Another very common network configuration of practical interest is shown in Fig. 6-7. To be specific, let the three-terminal resistor be characterized by the set of characteristic curves shown in Fig. 6-8*a* and *b*, and let the nonlinear resistors R_3 and R_4 be characterized by the curves shown in Fig. 6-8*c* and *d*, respectively. The equations of motion for this network are as follows:

Equations from the laws of elements

$$\text{Three-terminal resistor:} \quad \begin{cases} i_1 = g_1(v_1, i_2) & (6\text{-}3a) \\ i_2 = g_2(v_2, v_1) & (6\text{-}3b) \end{cases}$$

$$\text{Resistor } R_3: \quad i_3 = g_3(v_3) \qquad (6\text{-}3c)$$

$$\text{Resistor } R_4: \quad i_4 = g_4(v_4) \qquad (6\text{-}3d)$$

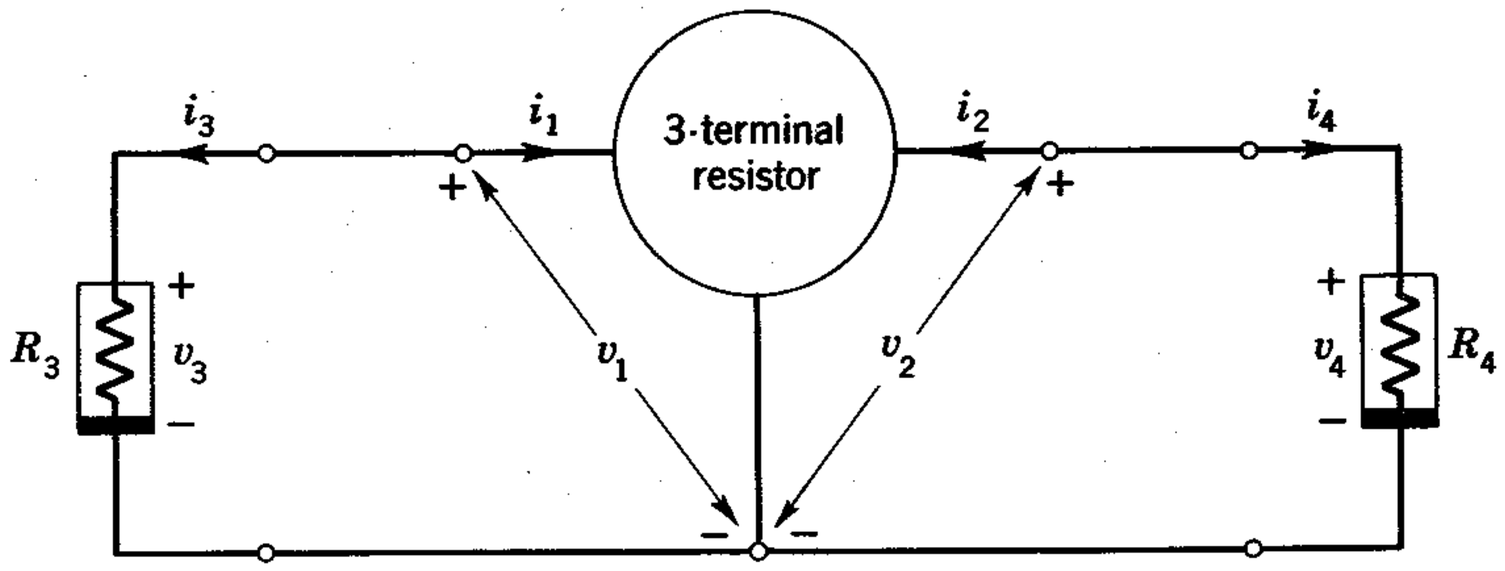


Fig. 6-7. The basic network configuration 2 consists of a nonlinear resistor connected across the input and the output ports of a three-terminal resistor.

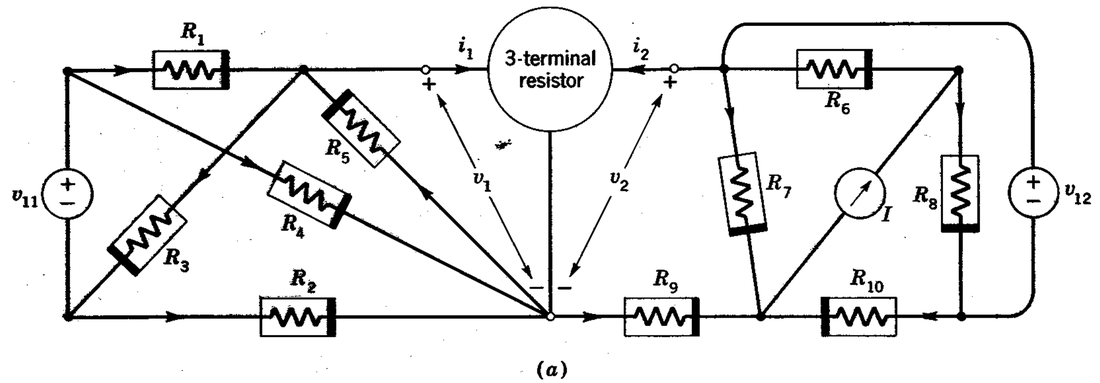


Fig. 6-12. Example of a complicated network which can be redrawn into the form of basic configuration 2.

Exercise 1: Consider the tunnel diode network shown in Fig. 6-5. (*a*) If $R = 500\ \Omega$, find the range of values of E for which there will be one, two, or three operating points. (*b*) If $E = 0.45$ volt, find the range of values of R for which there will be one, two, or three operating points.

Exercise 2: Give an alternate interpretation of the double load-line method by redefining the terminal variables of resistors R_3 and R_4 in Fig. 6-7.

Exercise 3: Sketch the graphical construction for determining the operating point of the network shown in Fig. 6-11, but with resistors R_1 and R_2 replaced by two identical varistors.

6-3 GRAPHICAL DETERMINATION OF DP PLOTS OF SERIES-PARALLEL NETWORKS

Using graphical methods, we can readily obtain the DP plot across the driving-point terminals of any black box containing only series-parallel interconnection of two-terminal resistors and dc sources. The procedure consists of a repeated application

of two basic graphical techniques, namely, the *series-combination technique* and the *parallel-combination technique.*

6-3-1 THE SERIES-COMBINATION TECHNIQUE

Consider first the simplest case of two nonlinear resistors connected in series as shown in Fig. 6-13*a*. Since the negative terminal of R_1 is connected to the positive terminal of R_2, we shall call this the *back-to-front series connection.* One method for determining the DP plot of this network consists of applying an adjustable current source I across terminals a-b and measuring the corresponding voltage. Since $I = i_1 = i_2$ and $v = v_1 + v_2$, the DP plot can be obtained by first aligning the v_1 axis with the v_2 axis, and then for each value of current $i_1 = i_2 = I$ graphically adding the value of v_1 from the v_1-i_1 curve, and the value of v_2 from the v_2-i_2 curve. This step can be carried out easily by drawing horizontal guidelines. If there are more than two resistors, the same procedure can obviously be applied, provided all resistors are connected in the back-to-front configuration shown in Fig. 6-13*c*.

EXAMPLES

1. Suppose the two resistors of Fig. 6-13*a* are linear with resistances R_1 and R_2. The v-i curves corresponding to R_1 and R_2 are, therefore, straight lines as shown in Fig. 6-14*a* and *b*. The DP plot of the two linear resistors in series is readily obtained by the above graphical procedure and is shown in Fig. 6-14*c*. Observe that since two points determine a straight line, we

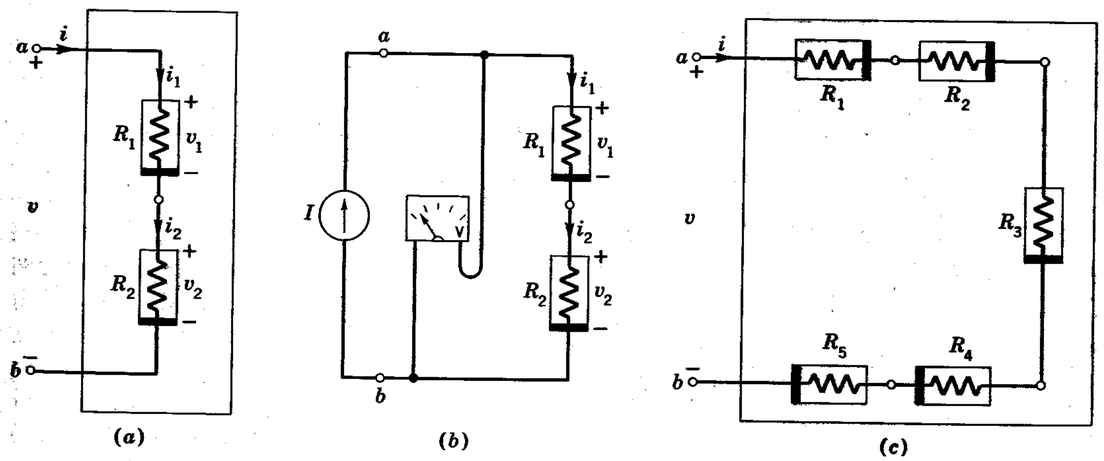


Fig. 6-13. A string of back-to-front series-connected nonlinear resistors.

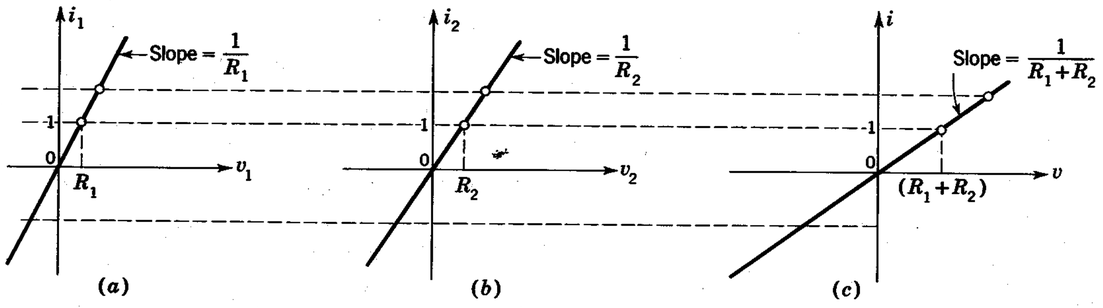
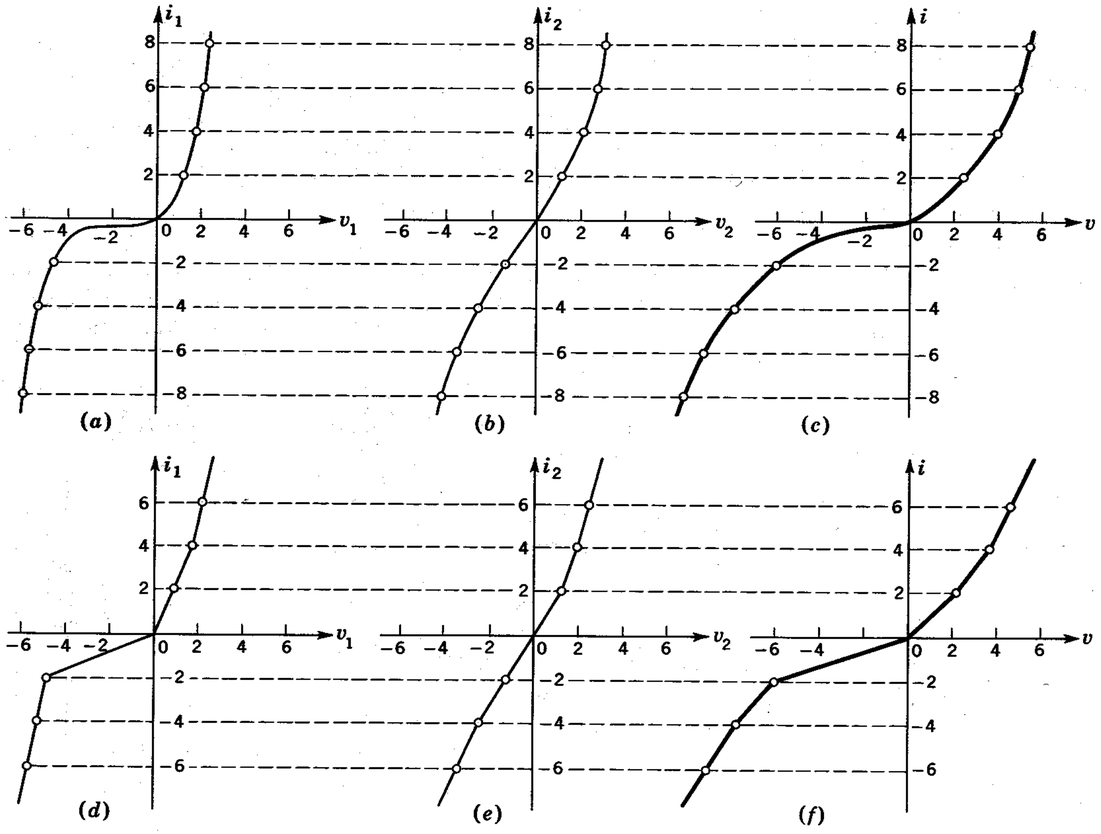


Fig. 6-14. The graphical procedure for determining the DP plot of two linear resistors in series.

Fig. 6-15. The DP plot of two nonlinear resistors in a back-to-front series connection can be obtained by adding the voltage of each curve along each horizontal guideline.

only have to apply this graphical procedure to two values of current. One convenient value of current to choose for this example is obviously $i_1 = i_2 = 0$.

2. Consider next the case where resistors R_1 and R_2 are characterized by the v_1-i_1 and v_2-i_2 curves shown in Fig. 6-15*a* and *b*, respectively. The DP plot obtained by the graphical procedure is shown in Fig. 6-15*c*. Although only a few horizontal guidelines



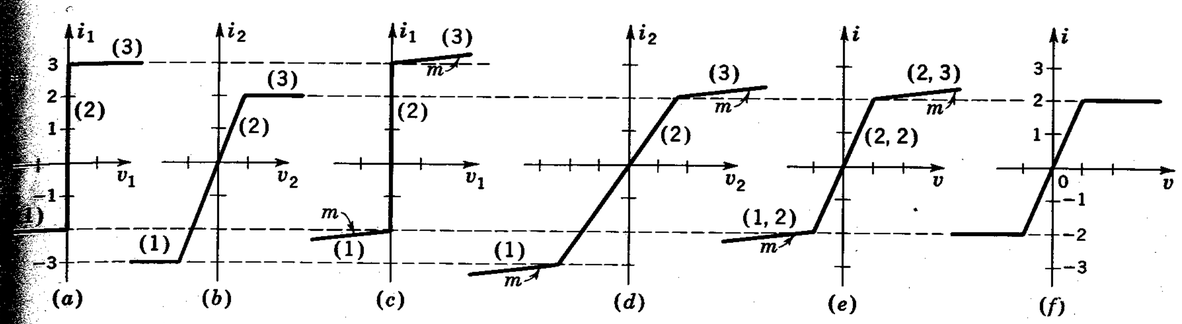


Fig. 6-16. The DP plot corresponding to v-i curves with horizontal segments can best be determined by a limiting process.

are shown, it is clear that more points must be found in order to obtain an accurate solution. This could be a rather time-consuming process. In most practical cases, we can simplify the task by first approximating the v-i curves with piecewise-linear segments as shown in Fig. 6-15*d* and *e*. From Example 1 we know two things: (1) The DP plot will also be piecewise-linear. (2) The horizontal guidelines need be drawn only through the breakpoints on each curve and one convenient point on each end segment. The resulting DP plot for this case is shown in Fig. 6-15*f*.

The above piecewise-linear procedure is relatively simple to carry out for most cases except when the v-i curves contain one or more horizontal segments. The confusions that sometimes resulted from the presence of horizontal segments can be resolved by a number of ways. One way is to interpret the horizontal segment as an open circuit and make use of the fact that any element in series with an open circuit results in another open circuit. The corresponding segment of the DP plot must therefore be horizontal. Another and perhaps more satisfactory way to resolve the above confusion is to replace each horizontal segment by a segment with a small but finite slope. The DP plot can then be determined by a limiting process. For example, suppose the v_1-i_1 and v_2-i_2 curves of R_1 and R_2 are shown in Fig. 6-16*a* and *b*, respectively. Since the end segments of both v-i curves are horizontal, let us replace them by the near-horizontal segments with a small positive slope m, as shown in Fig. 6-16*c* and *d*, respectively. If we label each segment combination consisting of segment n_1 of R_1 and n_2 of R_2 by (n_1,n_2), then segment (1,2) in Fig. 6-16*e* is obtained by adding the abscissas of segment 1 of R_1, segment 2 of R_2, etc.[1] If we gradually reduce the slope m to zero in the limit, we obtain the DP plot shown in Fig. 6-16*f*. In this case, segments (1,1) and (3,3) are located at $\pm\infty$, respectively.

[1] Notice that segments (1,1) and (3,3) are not shown because they are located off the page.

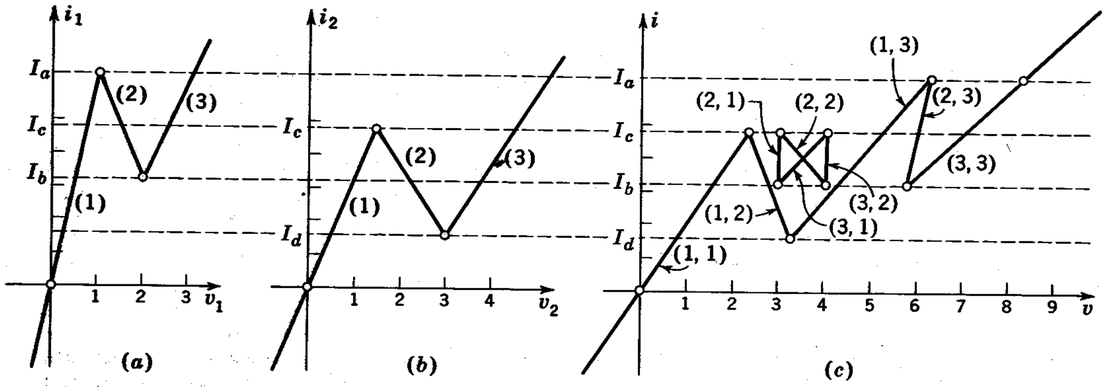


Fig. 6-17. A nine-segment multivalued DP plot is obtained by combining two appropriate tunnel diodes in series.

3. Let us now consider the case where the v-i curves are not monotonic. In particular, suppose R_1 and R_2 are tunnel diodes with the v_1-i_1 and v_2-i_2 curves shown in Fig. 6-17*a* and *b*, respectively. Since some horizontal guidelines would intersect the v_1-i_1 or the v_2-i_2 curves at more than one point, we must be more careful in carrying out the graphical procedure. If we recall that each point on the DP plot must correspond to the operating point of the network, then it is clear that if there are more than one operating points at a given current $i = I$, the DP plot must have a corresponding number of points at $i = I$. Hence, the DP plot will be *multivalued*. In order that we do not miss any operating points while carrying out the graphical procedure, it is important that we consider one segment of the v_1-i_1 curve at a time and combine this segment with *each* of the segments of the v_2-i_2 curve. For example, let us pick segment 2 of the v_1-i_1 curve first. Observe that this segment is defined only for $I_b \leq i_1 \leq I_a$. To combine this segment with segment 1 of the v_2-i_2 curve, which is defined only for $-\infty \leq i_2 \leq I_c$, we must first determine a range of current for which both segments are defined. In this case, the common range is $I_b \leq i \leq I_c$. Any current outside this range will not intersect one of the two segments, and hence no operating point is possible. The next step is to apply the above graphical procedure and obtain segment (2,1) as shown in Fig. 6-17*c*. Repeating the same procedure for segment 2 of R_1 and segment 2 of R_2, we obtain segment (2,2). Similarly, combining segment 2 of R_1 and segment 3 of R_2 leads to segment (2,3). As soon as all combinations with segment 2 of R_1 are exhausted, we pick another segment and repeat the procedure all over again. For the present example, the v_1-i_1 and the v_2-i_2 curves have three segments each. Accordingly, there is a total of nine combinations. The reader should verify that the DP plot shown in Fig. 6-17*c* is indeed obtained by this procedure.

Before going to the next section, it must be emphasized that the above graphical procedure is valid under only two assumptions: (1) The resistors are connected in the back-to-front manner shown in Fig. 6-13. (2) The usual reference voltage polarity and current direction are chosen for each element. Since the same procedure is applicable to the case where the resistors are replaced by black boxes (which may contain other elements inside), the above two assumptions must be carefully checked. If the reference polarity and direction do not satisfy these conditions, they must first be redefined properly before the graphical procedure is carried out.

Exercise 1: Consider the network shown in Fig. 5-12*b* consisting of two junction diodes connected back to back in series. (*a*) Sketch the DP plot of this network. (*b*) If the two diodes are replaced by ideal diodes, find the DP plot. HINT: Redefine the polarity and direction of one of the two diodes.

Exercise 2: Show that the DP plot of any resistor with a v-i curve Γ in series with a battery of terminal voltage E is simply a horizontal translation of Γ by E volts along the v axis.

Exercise 3: (*a*) Show that the DP plot segment (s_1,s_2) corresponding to segments s_1 of R_1 and s_2 of R_2 does not exist if the range of definition for segment s_1 and the range of definition for segment s_2 do not overlap. (*b*) Show that if the v_1-i_1 curve has n_1 segments and the v_2-i_2 curve has n_2 segments, then the DP plot will have n segments, where $n \leq n_1 n_2$. Why is the inequality sign needed?

6-3-2 THE PARALLEL-COMBINATION TECHNIQUE

Consider next the back-to-back parallel connection of two nonlinear resistors as shown in Fig. 6-18*a*. The reader will recognize this to be the dual of the series circuit presented earlier. Indeed, if we construct the dual graph of the series circuit of Fig. 6-13*b* as shown in Fig. 6-18*b*, we obtain the parallel network shown in Fig. 6-18*a*. Hence, the procedure for determining the DP plot is the dual of the procedure for the series case. In order to avoid interchanging the current and the voltage axes, we could carry out the graphical procedure by aligning the current axes and by drawing vertical guidelines. For example, corresponding to the v_1-i_1 and the v_2-i_2 curves shown in Fig. 6-18*c* and *d*, we obtain the DP plot shown in Fig. 6-18*e*.

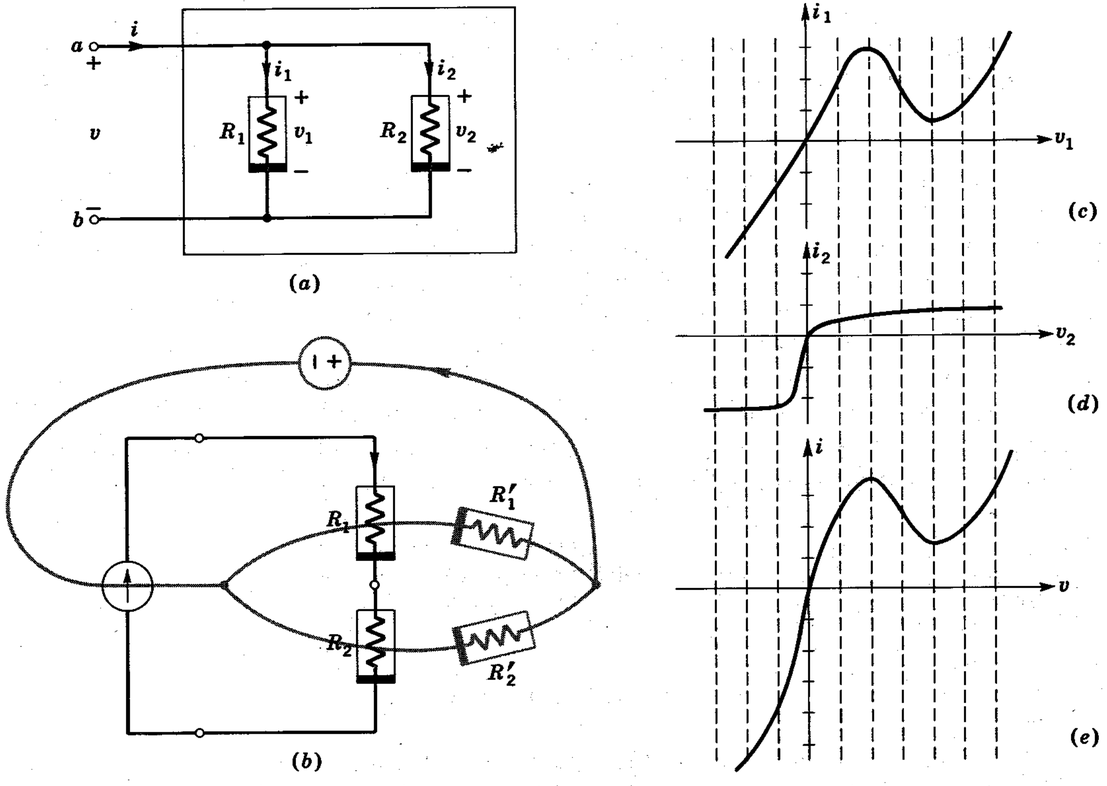


Fig. 6-18. A back-to-back parallel network and the graphical procedure for obtaining its DP plot.

Exercise 1: Consider two junction diodes connected in parallel (with opposite polarities). (*a*) Find the DP plot. (*b*) Replace the diodes by ideal diodes and obtain the DP plot.

Exercise 2: Discuss the procedure for finding the DP plot of a parallel network of nonmonotonic resistors.

Exercise 3: Show that the DP plot of any resistor with *v-i* curve Γ in parallel with a current source with terminal current I is simply a vertical translation of Γ by I amperes along the i axis.

6-3-3 COMBINATION OF SERIES-PARALLEL TECHNIQUES

By a repeated application of the series-combination and the parallel-combination techniques, the DP plot across any series-parallel network can be obtained. The basic idea is to replace all resistors in series or in parallel by a new resistor whose *v-i* curve is the DP plot of the two-terminal black box containing the resistors. Each application of this reduction technique will reduce the number of resistors in series or in parallel. The reduction technique is applied repeatedly until the network reduces to one resistor.[1]

As an illustration of the reduction technique, consider the network N shown in Fig. 6-19*a*. To emphasize that N is a series-parallel network, it is redrawn as shown in Fig. 6-19*b*. We can now apply the series-combination technique by replacing resistors R_1 and R_2 by R_{18}, and resistors R_{16} and R_{17} by R_{22}, as shown in Fig. 6-19*c*. Similarly, we apply the parallel-combination technique by replacing resistors R_5 and R_6 by R_{19}, resistors R_7 and R_8 by R_{20}, and resistors R_{11} and R_{12} and the current source by R_{21}. But now with the new resistors, there are new groups of series-parallel resistors. These new groups can be reduced further. We can reduce the network in Fig. 6-19*c* by replacing parallel resistors R_3 and R_{18} by R_{23}, series resistors R_9 and R_{20} by R_{24}, and parallel resistors R_{15} and R_{22} by R_{25}, as shown in Fig. 6-19*d*. Of course, this circuit can be reduced still further. For example, resistor R_4, R_{23} can be replaced by resistor R_{26}, as shown in Fig. 6-19*e*. Resistor R_{26} can then be combined with R_{19} to form R_{27} in Fig. 6-19*f*. By this time, we can see that by applying the reduction procedure a few more times to the chain of black boxes shown in Fig. 6-19*f*, the network would eventually reduce to only one resistor whose DP plot is the desired solution.

6-4 SOME PRACTICAL APPLICATIONS OF DP PLOT AND OPERATING-POINT CONCEPTS

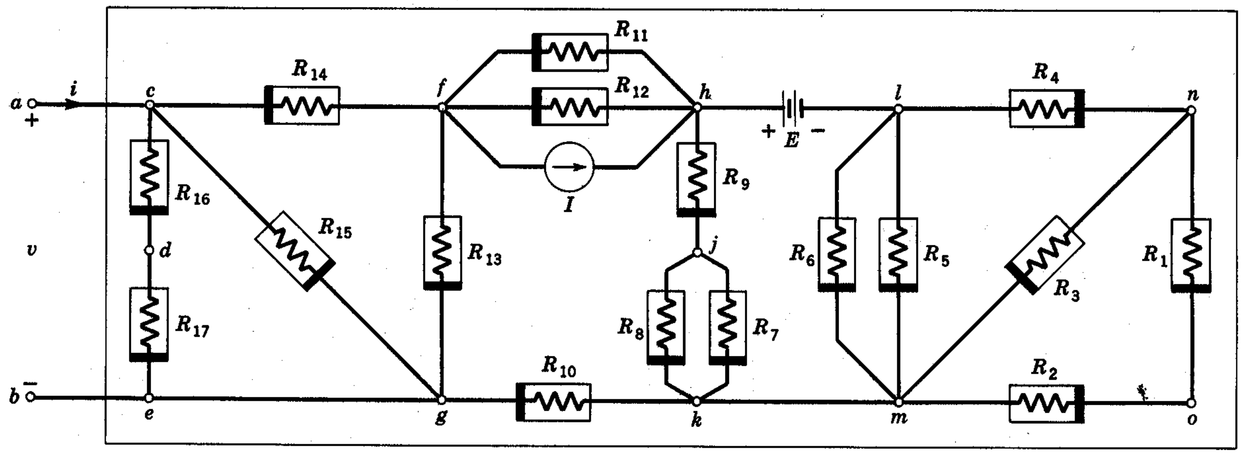
The techniques presented so far can be applied to a surprisingly large class of practical electronic circuits. While it is true that most practical circuits are more complex than those discussed earlier, many of these can be reduced to simpler circuits by combining appropriate groups of elements into black boxes. Once the DP plots of these black boxes are found, the problem becomes a lot simpler. One of the objectives of this book is to bring forth the power of this black-box approach. Let us consider some concrete examples.

6-4-1 CONCAVE AND CONVEX RESISTORS

The black box shown in Fig. 6-20*a* is made up of a junction diode, a zener diode, and a linear resistor in series. It is called a *concave resistor*.[2] The v_1-i_1 curve of the junction diode and the v_2-i_2 curve of the zener diode are shown by the dotted curves in Fig. 6-20*b* and *c*, respectively. For simplicity, we shall approximate

[1] A computer subroutine for implementing this algorithm can be easily written. A brief discussion of this subroutine is given in L. O. Chua, "A Computer Oriented Sophomore Course in Nonlinear Network Theory," *IEEE Trans. Circuit Theory*, Special Issue on Computer Applications in Education, September, 1969.

[2] A *v-i* curve is said to be concave if its slope di/dv is a nondecreasing function of v. It will be shown in Chap. 8 that concave resistors can be used as building blocks for synthesizing any prescribed concave *v-i* curve.



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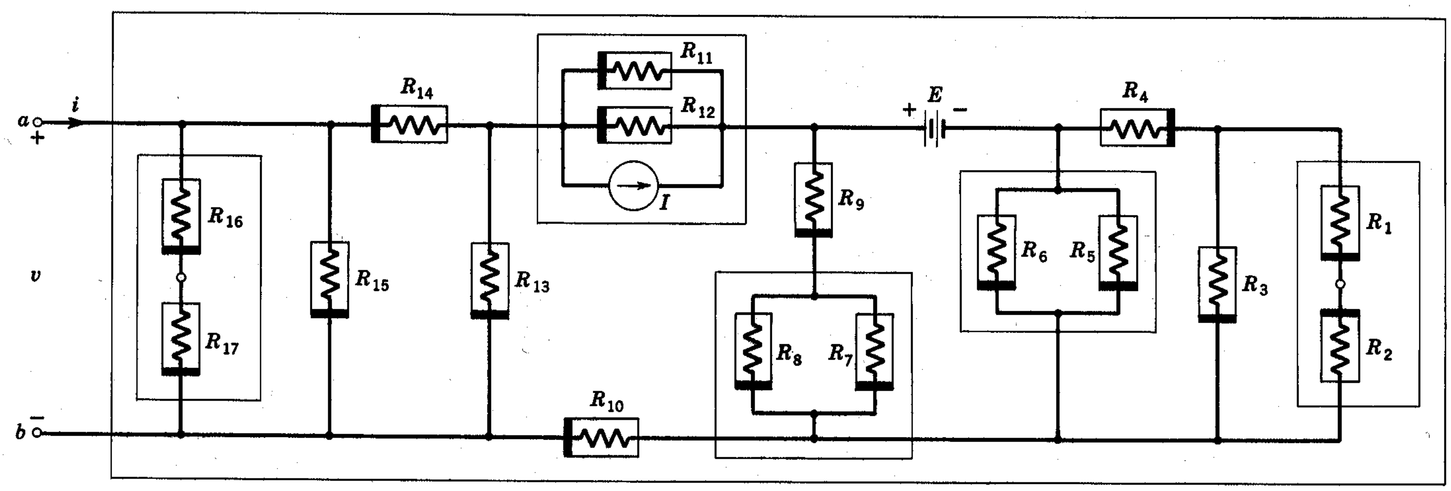

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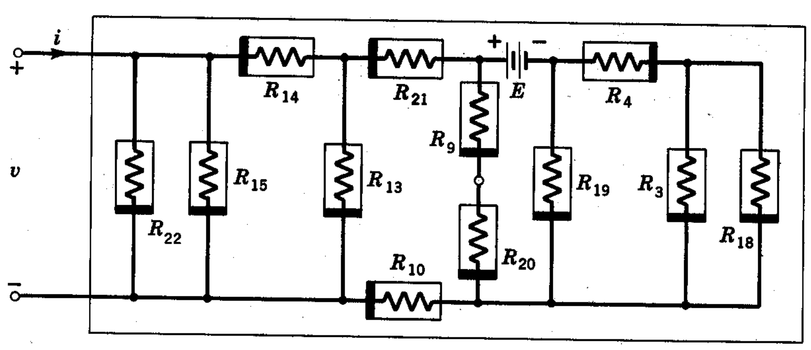

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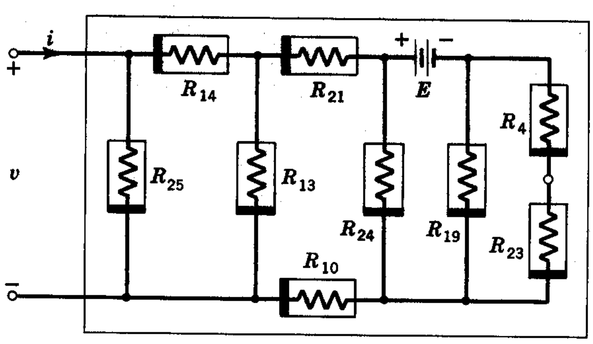

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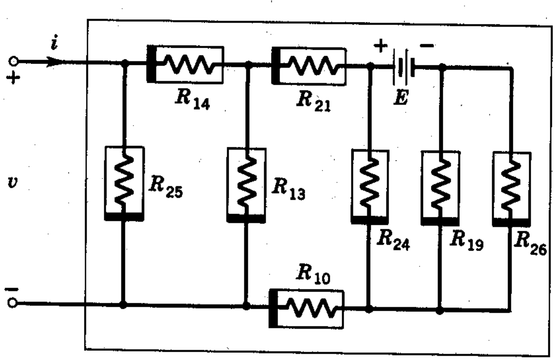

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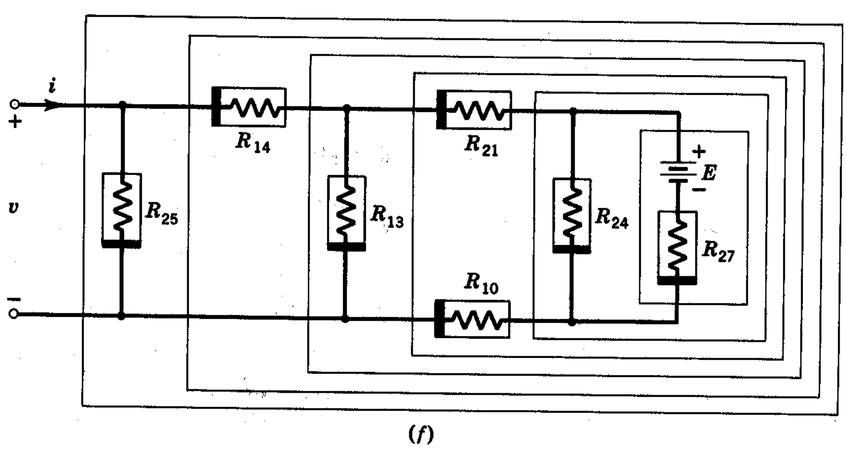


(f)

Fig. 6-19. The step-by-step reduction techniques for determining the DP plot of a series-parallel network.

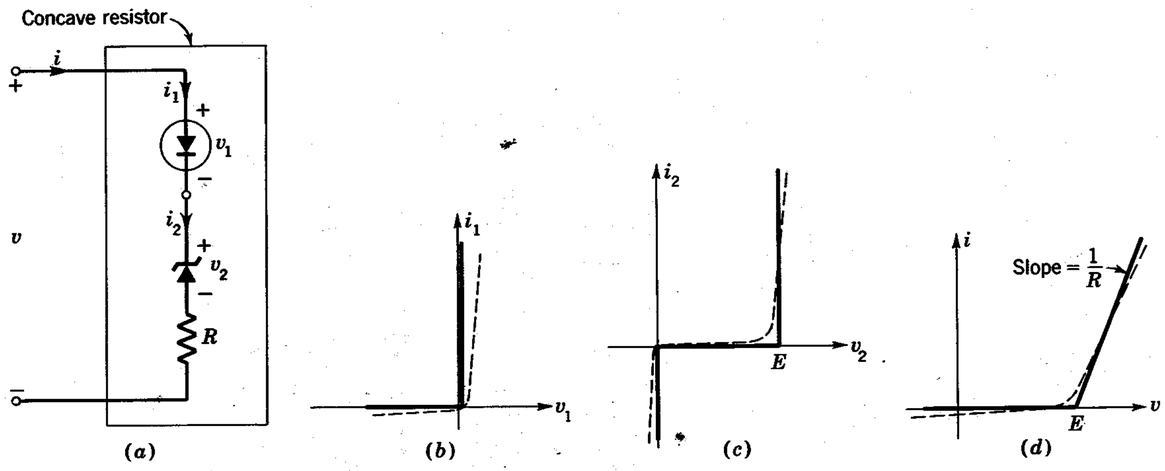


Fig. 6-20. By changing the value of the zener breakdown voltage E and the resistance R, the breakpoint and slope of the DP plot of the concave resistor can be easily adjusted to suit a particular application.

these curves by the piecewise-linear solid segments shown in the same figures. The DP plot of this black box is easily seen to be given by Fig. 6-20*d*, where the voltage E at the breakpoint is equal to the zener breakdown voltage (also known as the *avalanche voltage*), and the slope is equal to the reciprocal of the resistance R. This means that a concave resistor with any breakdown voltage E and slope $1/R$ can be easily synthesized in practice.[1] As such, concave resistors are indispensable building blocks for synthesizing arbitrary DP plots (see Chap. 8).

Consider next the black box shown in Fig. 6-21*a* consisting of a junction diode, a constant-current diode,[2] and a linear resistor. It is called a *convex resistor*.[3] The v_2-i_2 curve of the constant-current diode is shown by the dotted curve in Fig. 6-21*b*. For simplicity, we shall approximate this curve by the solid piecewise-linear segments shown on the same figure. Using this v_2-i_2 curve and an ideal diode curve for the junction diode, we obtain the DP plot shown in Fig. 6-21*c*. Observe that the breakpoint current and the slope of this DP plot can be adjusted by choosing an appropriate constant-current diode with the desired current I and an appropriate resistance R. Observe also that the v-i curve of the convex resistor is the dual of the concave resistor, and vice versa. Together, they constitute a fundamental set of building blocks for synthesis purposes (see Chap. 8).

6-4-2 ELEMENTS WITH A HORIZONTAL SEGMENT

A commonly used technique for obtaining a DP plot with a horizontal segment is to connect a linear resistor in parallel with a voltage-controlled resistor whose v-i curve contains a negative-resistance region.

A simple circuit consisting of a tunnel diode and a linear resistor in parallel is shown in Fig. 6-22*a*. The graphical construction for obtaining the DP plot is shown in Fig. 6-22*b*. Notice that if we choose the value of R equal to the magnitude of the tunnel-diode negative resistance, we would obtain the horizontal segment shown in this figure. In view of the low-voltage characteristics of the tunnel diode, this segment is horizontal only over a limited voltage range. To increase the range of the horizontal segment, a tunnel diode-battery combination can be added as shown in Fig. 6-22*c*. The v_a-i_a curve of the first tunnel diode is shown in Fig. 6-22*d*. Directly below it is the v_b-i_b DP plot of the tunnel diode-battery combination. The resulting v_1-i_1 DP plot is shown in Fig. 6-22*f*. Notice that the effect of adding the tunnel diode-battery combination is to compensate for each of the two negative-resistance segments so that they result in a single negative-resistance segment with a larger voltage range. The DP plot of the complete network is easily obtained and is shown in Fig. 6-22*g*. Notice that the operating range of the horizontal segment is almost three times that shown in Fig. 6-22*b*.

There are, of course, many other practical circuits using different devices that can achieve the same objective. However, the principles are quite similar. Which circuit to choose in any particular application depends on various practical considerations such as cost, operating range, linearity, and power rating.

6-4-3 ELEMENTS WITH A VERTICAL SEGMENT

A practical technique for obtaining a DP plot with a vertical segment is to connect a linear resistor in series with a current-controlled resistor whose v-i curve contains a negative-resistance region. A widely used circuit consisting of an NTC thermistor is shown in Fig. 6-23*a*. Clearly, a vertical segment can be obtained by choosing the value of the resistance R to be equal to the magnitude of the negative resistance of the thermistor.

6-4-4 MULTITHRESHOLD ELEMENTS

In many practical applications such as switching circuits, a DP plot with several negative-resistance segments alternating with positive-resistance segments is required. A simple circuit for achieving this consists of a string of tunnel diodes in series as

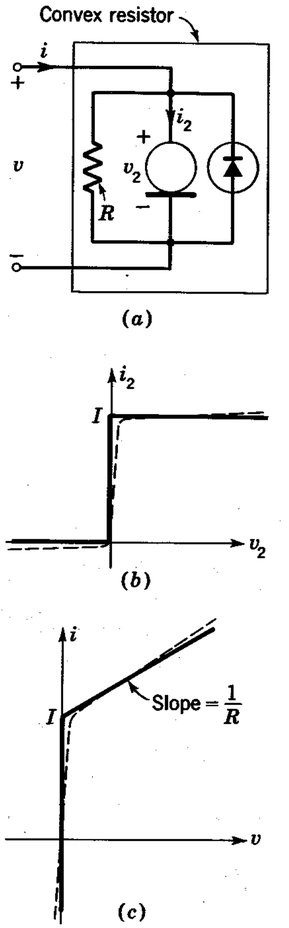
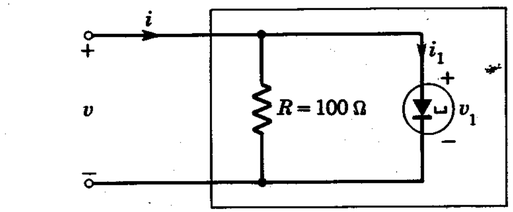


Fig. 6-21. By changing the values of I and R, the DP plot of a convex resistor can be adjusted to suit a particular application.

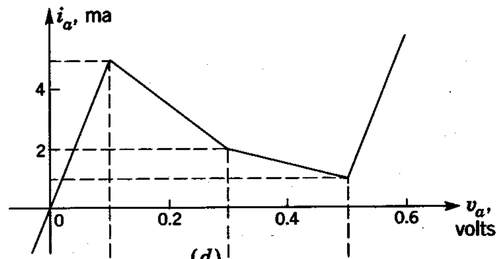
[1] For more accurate results, a small correction factor representing the forward voltage drop (0.2 to 0.7 volt) of the junction diode must be added to the zener voltage E.

[2] This relatively new device is also known as a *currector* or as a *field-effect current-limiting diode.* It can be approximately realized in practice from an FET upon short-circuiting the gate and the source terminals. In this case, the solid horizontal segment in the left-half plane of Fig. 6-21*b* must be replaced by a vertical segment, thereby obviating the need for the junction diode in the convex resistor (see the footnote in Sec. 1-6-2).

[3] A v-i curve is said to be convex if its slope di/dv is a nonincreasing function of v. It will be shown in Chap. 8 that convex resistors can be used as building blocks for synthesizing any prescribed convex v-i curve.



(a)



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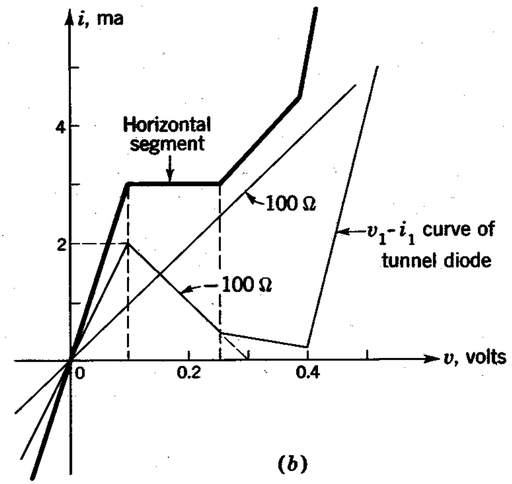

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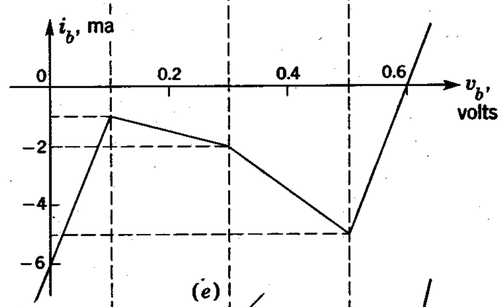

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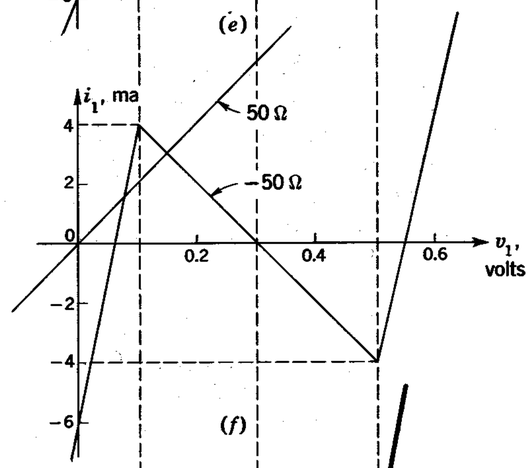

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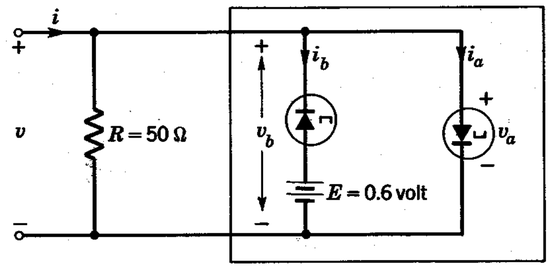

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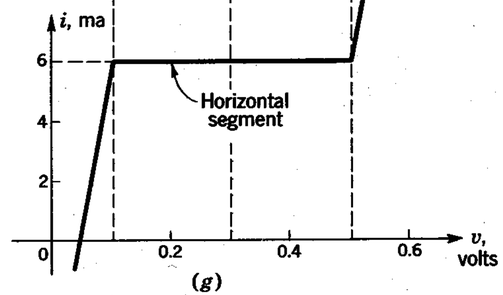
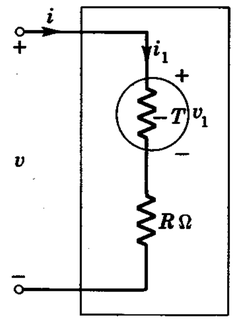
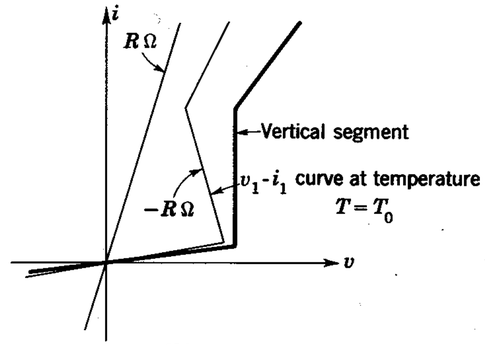


(g)

Fig. 6-22. Two practical tunnel-diode circuits for obtaining a DP plot with a horizontal segment.



(a)



(b)

Fig. 6-23. The DP plot of an NTC thermistor in series with an appropriate linear resistor will contain a vertical segment at a given temperature $T = T_0$.

shown in Fig. 6-24*a*. Observe in Fig. 6-24*b* that the valley current of each tunnel diode was chosen greater than the peak current of the preceding tunnel diode.[1] This arrangement prevents the existence of additional segments, thereby making the graphical construction very easy. The resulting DP plot shown in Fig. 6-24*c* contains three negative segments alternating with four positive segments. Observe that if we excite the black box with a current source, and if we assume that the operating point is initially on segment 1, then as we increase the driving-point current i beyond $i = I_a$, the operating point will switch to segment 3. A further increase in the current to $i = I_c$ would switch the operating point from segment 3 to segment 5, etc. Obviously, by connecting more tunnel diodes in series, we can obtain any number (within the practical current range of available tunnel diodes, of course) of such alternating segments. If we monitor the voltage across the black box, then it is clear that each time the current i exceeds a *threshold* value (such as I_a, I_c, I_e, etc.), the voltage jumps to a higher value, thereby indicating a change in state. As such, this black box has found applications in multithreshold circuits. Observe that if we make the threshold currents I_a, I_c, and I_e differ only by a very small preset amount, we would obtain a very sensitive threshold device in the sense that a small change in current would be registered by the monitor, such as a voltmeter, as a relatively large change in voltage. This property is very useful in many control applications. For example, if several relays with different actuating voltages are connected across the black box, then each time a threshold current is exceeded, a relay will close, thereby actuating some external control mechanism.

[1] The currents at the minima and maxima of a tunnel diode *v-i* curve are often called the *valley* and the *peak currents,* respectively.

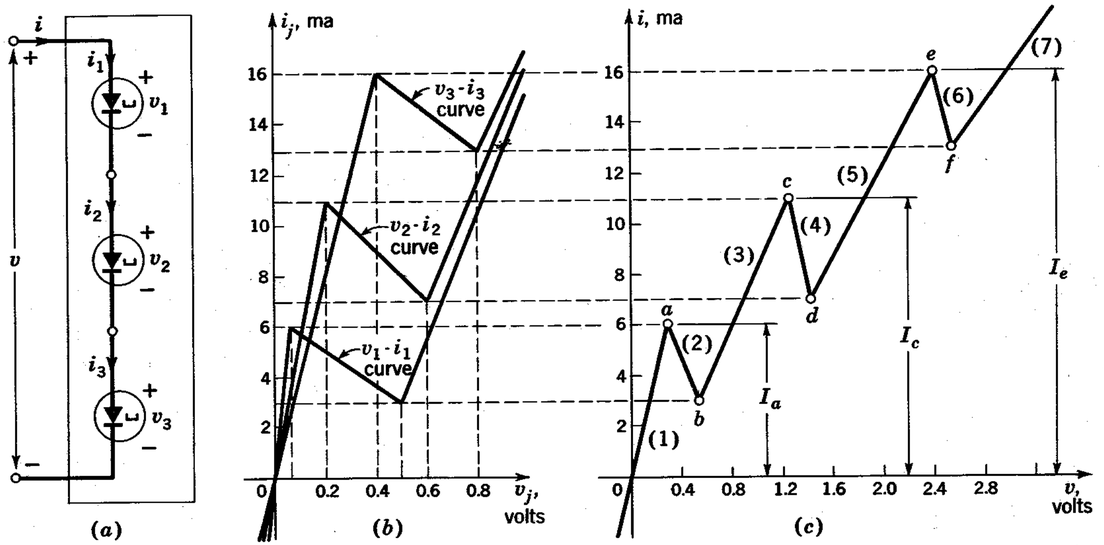
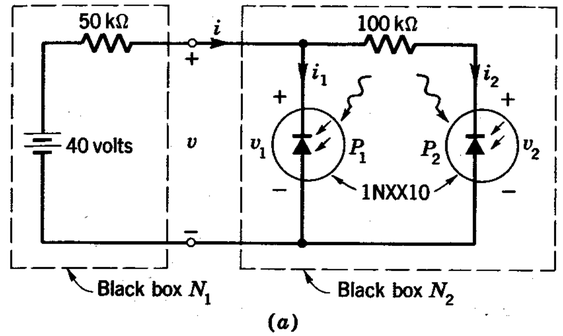
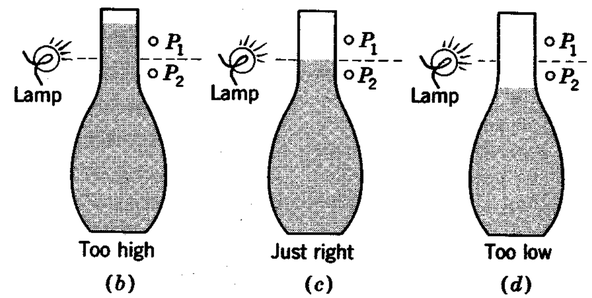


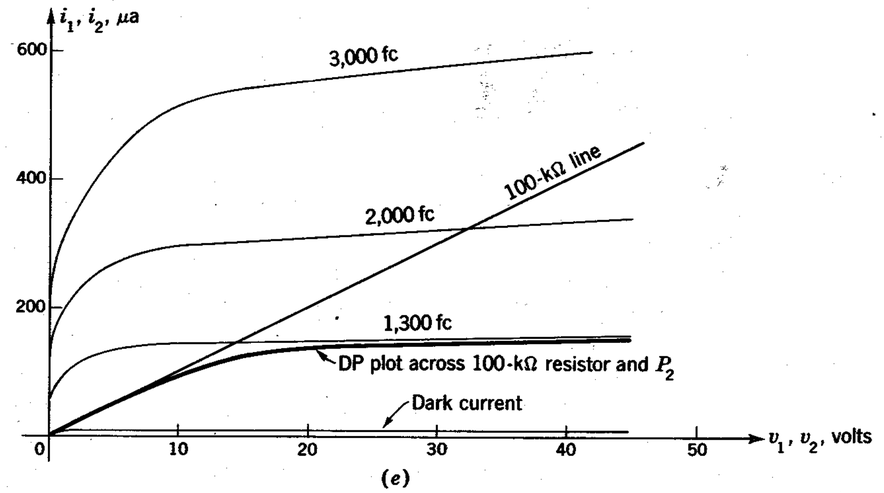
Fig. 6-24. A multithreshold DP plot can be realized by connecting a string of tunnel diodes in series.

6-4-5 AUTOMATIC SORTING CIRCUIT

One of the most common applications of the operating-point concept is the design of automatic sorting circuits for furnishing different preset output voltages in accordance with some "quality" of a product in the production line. A simple circuit of this nature is shown in Fig. 6-25*a*. This circuit is used in many beer bottling plants for sorting the liquid level of beer bottles on a production line. The basic idea stems from the fact that the intensity of a light beam is attenuated as it passes through a colored liquid such as beer. Hence, if we install a light source at the desired liquid level and two identical photodiodes situated as shown in Fig. 6-25*b* to *d*, then the amount of illumination received by each photodiode will depend on the level of the liquid. To be specific, let us assume that if the level is too high, as in Fig. 6-25*b*, both photodiodes receive an illumination of 1,300 fc. If the level is just right, as in Fig. 6-25*c*, photodiode P_1 receives an illumination of 2,000 fc and photodiode P_2 receives an illumination of 1,300 fc. Finally, if the level is too low, both photodiodes receive an illumination of 2,000 fc. Since the *v-i* curve of each photodiode changes with light illumination, it is clear that the voltage developed across the photodiode P_1 will not be the same in each case. Hence, if appropriate voltage-sensing devices such as relays are connected across the photodiode P_1 (for simplicity, let us assume the loading effect is negligible), then depending on the voltage across P_1, one relay will be actuated at a given time. This relay will in turn actuate an







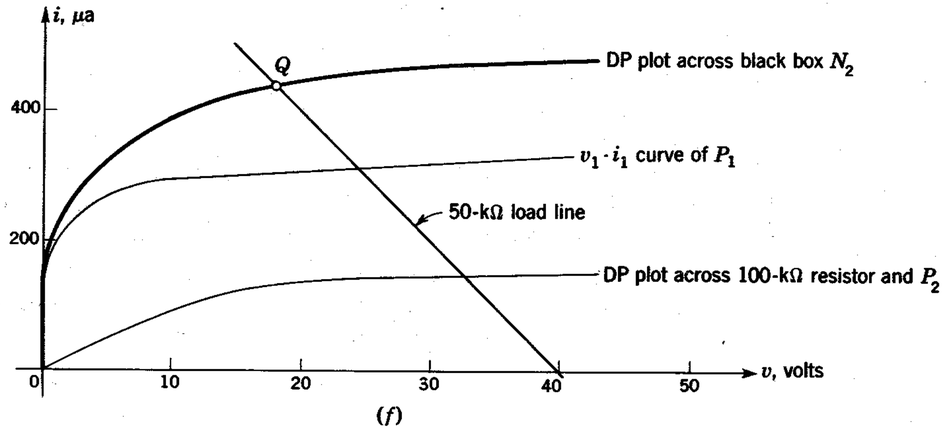


Fig. 6-25. A basic liquid-level sorting circuit and the graphical construction for determining the operating voltage corresponding to the case where the level is just right.

automatic mechanism to channel the bottle into the proper conveyor. In this way, only the bottle filled to the right level will arrive at the final sealing location; bottles not filled properly will be diverted into separate lines designed to correct the discrepancy.

In order to choose the appropriate relays, we must solve for the operating point of the circuit shown in Fig. 6-25*a*. Since the voltage across P_1 is our only concern, it is obvious that we locate the two black boxes N_1 and N_2 as shown by the dotted line. Since the procedure is identical in each instance, let us consider only the one where the liquid level is just right. Referring to the characteristic curves of the photodiode type 1NXX10 in Appendix D, we locate the two curves corresponding to a light illumination of 1,300 and 2,000 fc. These two curves are drawn in light lines in Fig. 6-25*e*. The DP plot across the resistor-photodiode combination is obtained by adding the voltage coordinates of the 100-kΩ line and the v_2-i_2 curve of P_2 as shown in Fig. 6-25*e*. If we add the current coordinates of this curve with the v_1-i_1 curve of P_1 we obtain the DP plot across the black box N_2 as shown in Fig. 6-25*f*. The intersection Q between this DP plot and the load line is the operating point. Hence, the voltage corresponding to this case is $v = 18$ volts. Carrying out the same construction for the remaining cases, we find the voltage $v = 25.2$ volts when the level is too high and $v = 16.6$ volts when the level is too low.

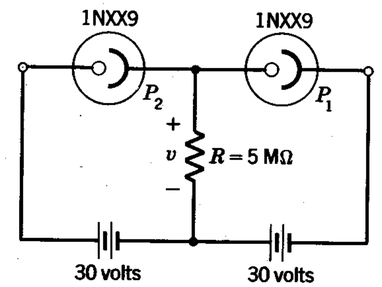
The above principle has been utilized in the design of many instrumentation circuits. It is also used in the design of photometers for measuring light illumination; densitometers for measuring the density of liquid solutions; colorimeters for analyzing the color content of translucent materials and chemical solutions; and spectrophotometers for measuring the spectrum of a light source. It should be clear that we need not restrict ourselves to photodiodes. A phototube or a solar cell would do just as well. In fact, in the latter case, no external battery is necessary. Since the current and voltage furnished by a solar cell are very small, the price we pay for saving a battery is that a more sensitive monitoring device or circuit will be needed. This principle is not restricted to light-sensitive controlled resistors only. In many applications such as manometers, anemometers, flowmeters, and thermal conductivity detectors, the choice of temperature-sensitive controlled resistors such as thermistors is more suitable.

6-4-6 AUTOMATIC COMPARISON AND NULL DETECTION CIRCUIT

We shall now consider an extremely useful circuit for comparing the distance, position, direction, etc., between two objects as well

as other physical quantities. A typical circuit of this nature is shown in Fig. 6-26*a*. This circuit has been proposed for achieving the three-spaceship flight formation scheme shown in Fig. 6-26*b*. This flight formation is part of an elaborate experiment proposed to qualify the spaceships for interplanetary expedition. The experiment calls for spaceship 1 to maintain a fixed distance d from

Fig. 6-26. A basic position-comparison and null-detection circuit and the graphical construction for determining the operating voltage corresponding to three different relative positions.



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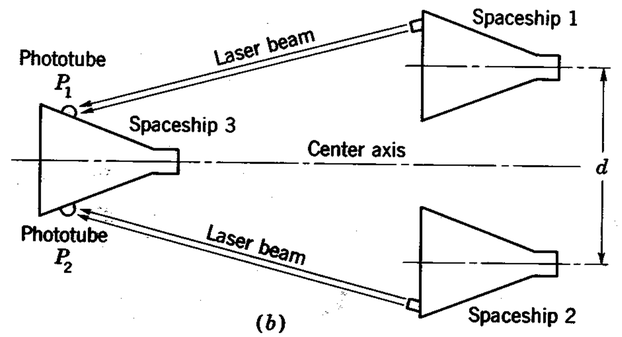

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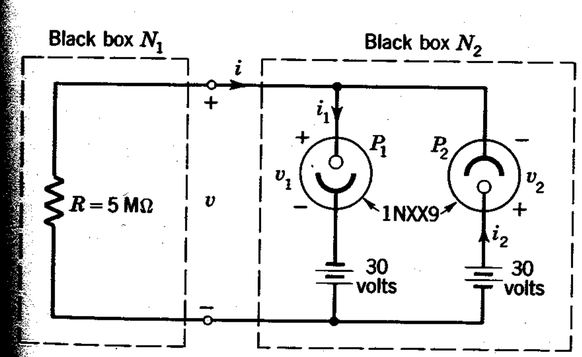

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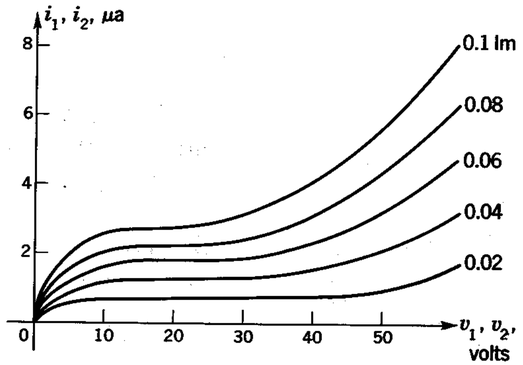

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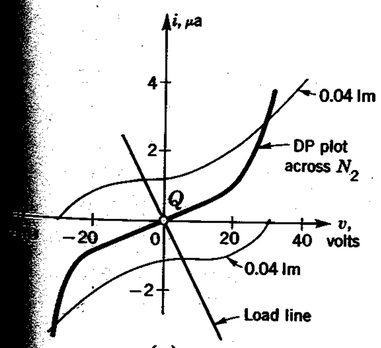

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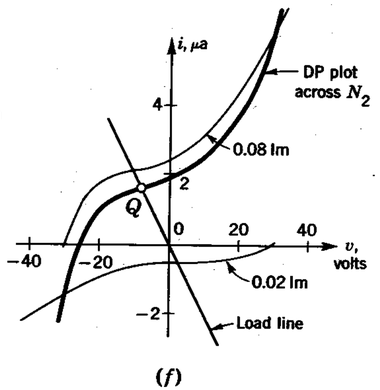

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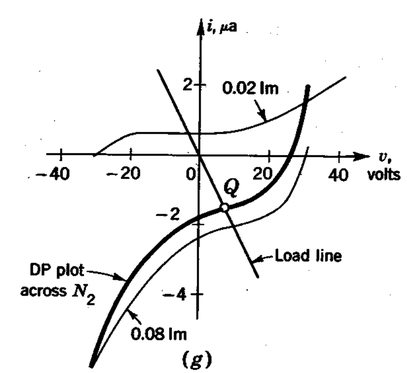


(*g*)

spaceship 2, and for spaceship 3 to move along an imaginary center axis between spaceships 1 and 2. The first requirement can be satisfied by simple radar control. Our problem, therefore, consists of maintaining the position of spaceship 3 along the center axis. To achieve this task, it is proposed that two laser beams of equal intensity be directed from spaceships 1 and 2 toward a phototube mounted on each side of spaceship 3, as shown in Fig. 6-26*b*. If spaceship 3 is exactly on the center line, both phototubes will receive equal light intensity. On the other hand, if spaceship 3 is closer to spaceship 1, phototube 1 will receive a higher light intensity than phototube 2 because the second laser beam has to travel a greater distance, thereby becoming more attenuated.[1] The opposite situation is encountered if spaceship 3 is closer to spaceship 2. Our problem is to find the voltage across the 5-MΩ resistor corresponding to different locations of spaceship 3 so that the astronaut inside would be able to steer his spaceship in accordance with the instrument reading.[2]

Since we are interested only in the voltage across the resistor, let us redraw the circuit into the black-box configuration shown in Fig. 6-26*c*. Our object is to find the DP plot across the black box N_2. For convenience, the characteristic curves for the phototube 1NXX9 are redrawn in Fig. 6-26*d*. Let us suppose that both phototubes receive a light illumination of 0.04 lm when the spaceship is on the center axis. The graphical construction corresponding to this case is shown in Fig. 6-26*e*. The resulting DP plot intersects the load line at the origin, and hence $v = 0$ for this case. The monitoring device must therefore indicate a *null reading* when spaceship 3 is on the center line.

Suppose, next, spaceship 3 is closer to spaceship 1 such that phototube 1 receives 0.08 lm while phototube 2 receives only 0.02 lm. The DP plot in this case is shown in Fig. 6-26*f*, and the voltage at the operating point is given by $v = -7.5$ volts. The opposite case where phototube 1 receives 0.02 lm and phototube 2 receives 0.08 lm is shown in Fig. 6-26*g*. By carrying out the same procedure for different light illuminations, a "flight-control curve" can be plotted indicating the relationship between the voltmeter reading and the relative location of spaceship 3. The astronaut can, therefore, steer his spaceship in accordance with this curve. Alternately, a control circuit can be designed to do this automatically.

It should be obvious by now that this principle can be utilized for designing many other control circuits, such as an airplane instrument-landing system. The phototubes in this case are mounted at the end of each wing, and the two light beams

[1] It is assumed that the distance from one spaceship to another is so vast that the laser beam becomes sufficiently attenuated to register a significant unbalance in the light intensity received at the phototubes. The alert reader should recognize the contrived nature of this example. The important concept to learn here is the *balancing property* of the bridge phototube circuit. This property has been widely used in many more mundane applications.

[2] This resistor represents the input resistance of the monitoring device such as a voltmeter or other control circuitry.

are directed from opposite sides of the runway. In all cases, a null reading indicates an optimum operation, and the control circuitry's job is to try to achieve a null by comparing the deviation from the desired position. Because of this interpretation, this class of circuit is called a *comparison and null-detection circuit.*

A closer inspection of the circuit shown in Fig. 6-26*a* shows that it is a bridge circuit with the "sensing" element located at opposite arms. The ability to detect any unbalance between the two arms is a basic property that makes the bridge circuit so useful for comparison purposes. If we replace the phototubes by two thermistors, the result is, of course, a sensitive temperature-comparison circuit. There is an almost endless variety of useful circuits that are based primarily on this basic bridge configuration. However, since the principle is the same, we shall not labor any longer to discuss them. After all, one of the merits of the black-box approach is the possibility of extracting the general concepts from many seemingly unrelated circuits.

Exercise 1: (*a*) Using the *v-i* curves for the junction diode type 1NXX2 and the zener diode type 1NXX3, obtain the exact DP plot of the concave resistor shown in Fig. 6-20*a* with R equal to 50 Ω, 100 Ω, 500 Ω, and 1 kΩ. (*b*) Compare each DP plot with that obtained from piecewise-linearizing the *v-i* curves. (*c*) Formulate a simple rule to correct the error resulting from the piecewise-linearization.

Exercise 2: Show how a convex resistor may be synthesized by a concave resistor and a 45° reflector or gyrator.

Exercise 3: (*a*) Verify the DP plot shown in Fig. 6-24*c*. (*b*) Find the new DP plot if the valley current of each tunnel diode is less than the peak current but greater than the valley current of the preceding tunnel diode.

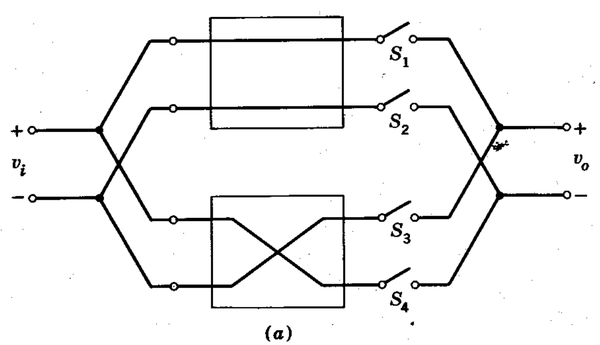
Exercise 4: (*a*) Find the operating voltage of the liquid-level sorting circuit in Fig. 6-25*a* when the level is too high and when it is too low. (*b*) Why is the 100-kΩ resistor needed? How should its value be chosen?

Exercise 5: Using the solar cell type 1NXX11, design a liquid-level sorting circuit without batteries for carrying out the same task as in Fig. 6-25.

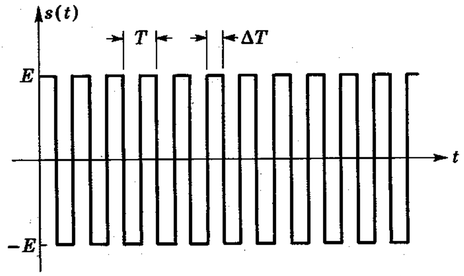
Exercise 6: To improve reliability, it is desirable that the operating voltage in each case of the sorting circuit in Fig. 6-25 differ by a relatively large amount. Show that this can be achieved by replacing the 50-kΩ linear resistor by a nonlinear resistor with an appropriate *v-i* curve. Specify a *v-i* curve so that the operating voltage in Fig. 6-25*c* differs from the operating voltage in Fig. 6-25*b* and *d* by an equal amount.

Exercise 7: Verify the graphical construction shown in Fig. 6-26*e* to *g*.

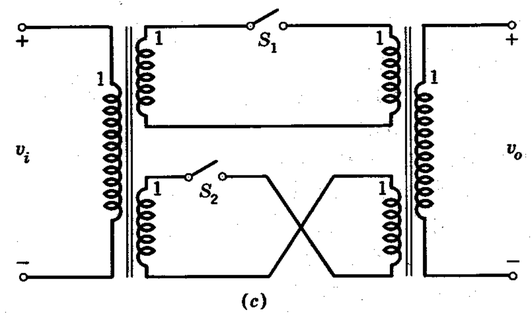
Exercise 8: In practice, the two phototubes shown in Fig. 6-26*a* may not be identical. To achieve a null reading when spaceship 3 is on the center axis, a resistance may be inserted in series with each phototube. Show how the values must be chosen to achieve a null. Assume that the *v-i* curves of phototube 2 are displaced in the vertical direction from the original *v-i* curve by 1 μa.



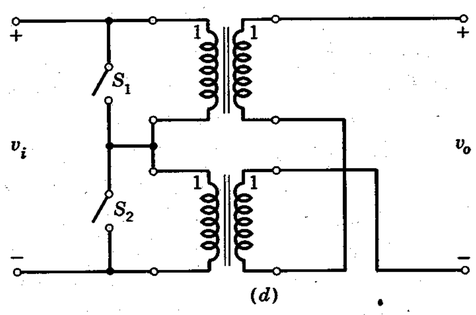
(a)



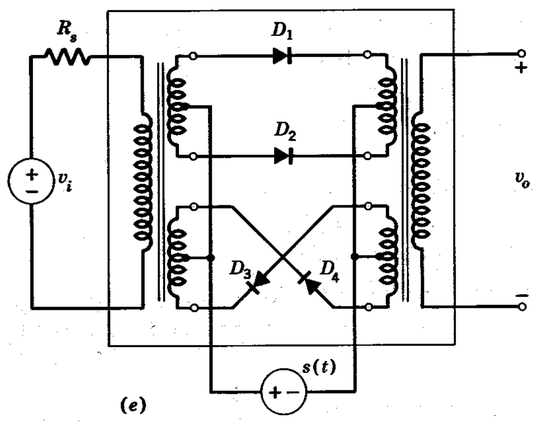
(b)



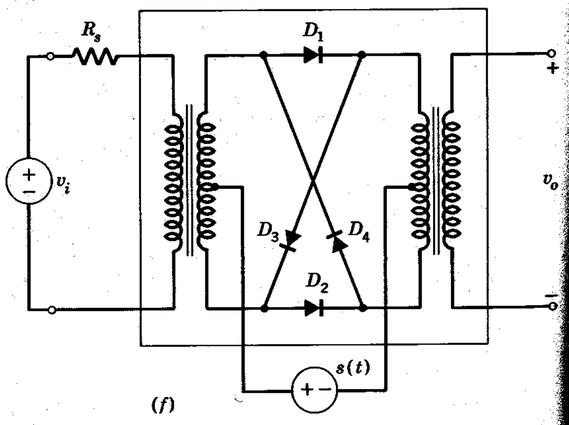
(c)



(d)



(e)



(f)

Fig. 10-11. The step-by-step procedure leading to the synthesis of a ring modulator.

cuits. Moreover, the two cases are independent of one another in the sense that only two of the diodes have an effect in the network at any one time. This observation suggests that if we combine the two sets of diodes as shown in Fig. 10-11*f*, we would still obtain the same result. The two networks shown in Fig. 10-11*e* and *f* are, therefore, equivalent. Observe that if we trace along the forward direction of each diode in Fig. 10-11*f*, we would eventually return

to the original point. For example, starting with diode D_1, we proceed to D_3, then to D_2, then to D_4, and finally back to D_1. This gives the appearance of a ring, and hence the above network is commonly called a *ring modulator.*

Both the chopper and the amplitude modulator are widely used in telemetering equipment and other long-distance communication systems. Some of these applications are given in the form of problems at the end of this chapter.

Exercise 1: Discuss the disparity between the TC plots of the practical chopper circuits in Fig. 10-8 and the ideal TC plots shown in Fig. 10-9*c*.

Exercise 2: Show that the transformers in the ring modulator can be replaced by four linear resistors. What are the disadvantages of doing this in terms of the disparity between the resulting TC plots and that shown in Fig. 10-9*f*?

Exercise 3: Find another circuit for realizing an amplitude modulator.

10-5 SYNTHESIS OF MULTICONTROLLED ELECTRONIC SWITCHES

So far we have considered only electronic switches which are turned on and off by a single switching signal $s(t)$. Let us now consider the more general case where a predesignated combination of several switching signals $s_1(t)$, $s_2(t)$, . . . , $s_n(t)$ are needed to turn on and off the switch. We shall refer to this class of circuits as *multicontrolled switches.* While a single-controlled switch is analogous to a padlock, a multicontrolled switch is analogous to a combination lock. Just as the latter is much more versatile, the multicontrolled switch has a much wider field of application. Referring again to the general configuration shown in Fig. 10-2*c*, it is clear that the DP plot of a multicontrolled bidirectional switch is still given by Fig. 10-3, and that for a multicontrolled unidirectional switch is given by Fig. 10-4.

We shall consider only the synthesis of a multicontrolled unidirectional switch. The bidirectional case can be realized in a manner similar to that presented in Sec. 10-3. Consider what happens if we connect the two unidirectional switches in parallel as shown in Fig. 10-12*a*. Let us assume for simplicity that the switching signals $s_1(t)$ and $s_2(t)$ are stepwise waveforms as shown in Fig. 10-12*b* and *c*, respectively. The DP plots across each switch at any time $t = t_0$ are shown in Fig. 10-12*d* and *e*. The resulting DP plot is shown in Fig. 10-12*f*.[1] Observe that the breakpoint voltage $v = E$ at $t = t_0$ is always equal to the smaller of the two breakpoint voltages $s_1(t_0)$ and $s_2(t_0)$. In other words, the breakpoint voltage of the resulting DP plot at any time t depends on

[1] Review Sec. 6-3-1 on how to combine DP plots with vertical segments.

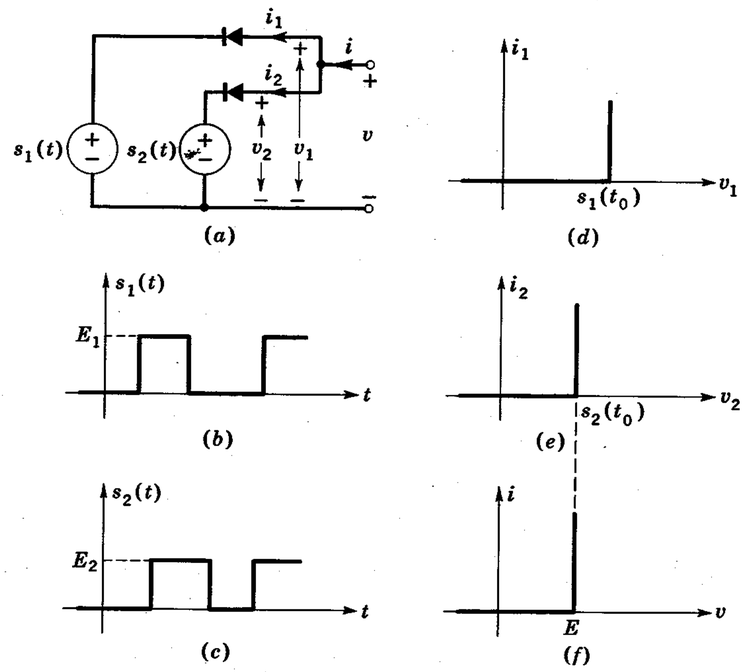


Fig. 10-12. The DP plot of two unidirectional switches in parallel has a breakpoint voltage equal to the smaller of the breakpoint voltages of the component DP plots.

the particular amplitude combination of $s_1(t)$ and $s_2(t)$ at the same time. More generally, if n sections of this unidirectional switch are connected in parallel with switching signals $s_1(t)$, $s_2(t)$, . . . , $s_n(t)$, then the DP plot at any time t is still given by Fig. 10-12*f*, where the breakpoint voltage E is equal to the smallest amplitude of these signals at the same time. Since the smallest amplitude of each switching signal is zero, the DP plot will look like a short circuit (switch is on) whenever one switching signal is zero at a given time. This is equivalent to saying that the resulting switch will open at a given time t if, and only if, all switching signals are simultaneously present (not zero) at the same time t. It should now be clear that this property allows us to choose all kinds of combinations to make the switch open or close at a given time. For example, this property can be used in the design of an electronic combination lock. Let us now consider two common applications.

10-5-1 SYNTHESIS OF A COINCIDENCE GATE

If we substitute an n-section multicontrolled switch in place of the black box shown in Fig. 10-2*c*, we would obtain the equivalent circuit shown in Fig. 10-13*a*.[1] Notice that if we let $E_1, E_2, \ldots, E_n$

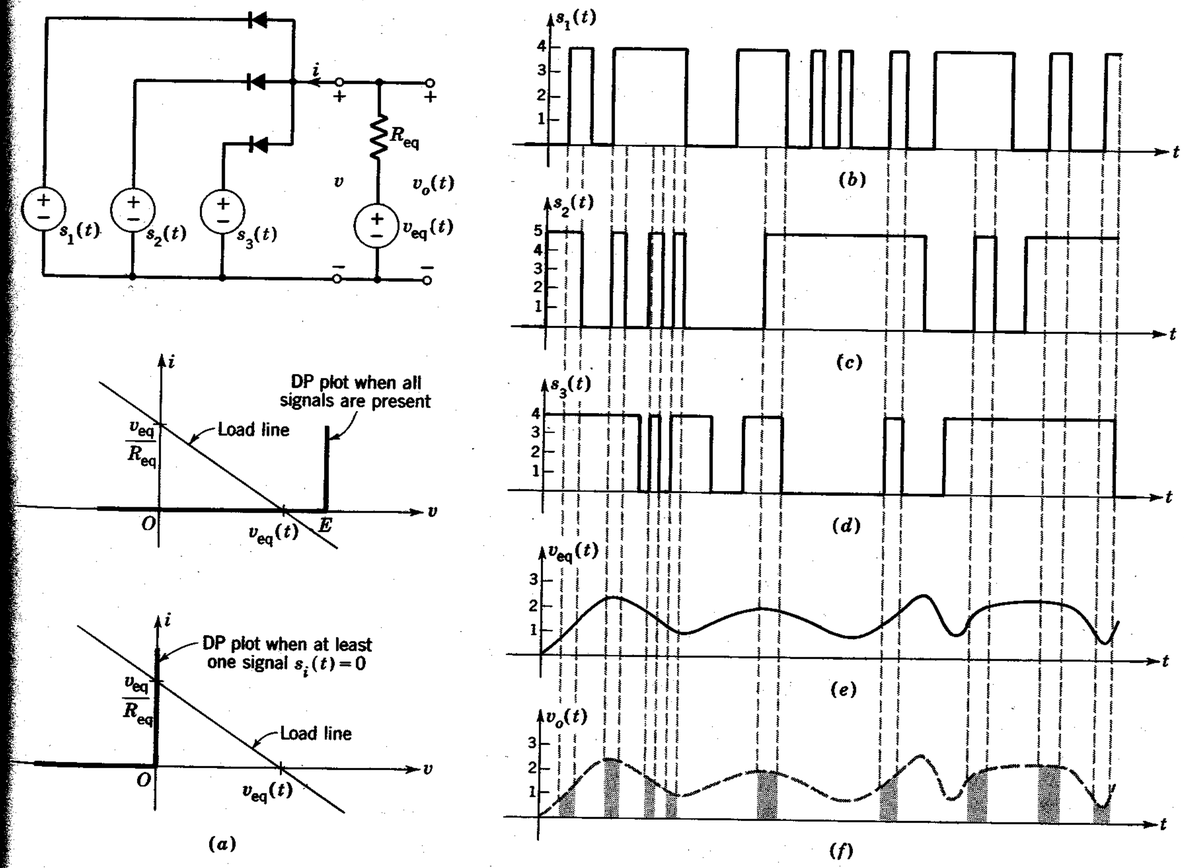
[1] To avoid unnecessary complexity in drawing, only three sections are shown.

be the amplitude of the respective switching signals, and if E is the smallest among these, then it is necessary that the equivalent input signal satisfies

$$0 \leq v_{eq}(t) \leq E \tag{10-15}$$

for all time t. Under this condition, the output voltage $v_o(t) = v_{eq}(t)$ if, and only if, none of the switching signals is zero at the same time. On the other hand, if at least one switching signal is zero, then $v_o(t) = 0$. The sample waveforms shown in Fig. 10-13*b* to *f* would illustrate this property more clearly. Since the input signal can arrive at the output terminals only if all switching signals coincide (not zero) at a given time, this circuit is generally known as a *coincidence gate*. We shall now show how coincidence gates can be combined to synthesize what is known as a transmission gate.

Fig. 10-13. The synthesis of a coincidence gate and a demonstration of its operating properties.



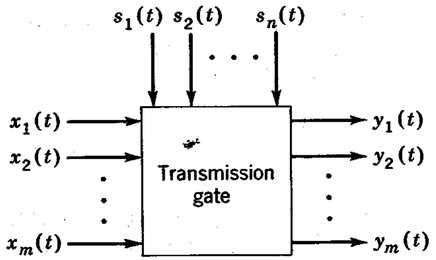


Fig. 10-14. Symbolic representation of a multi-input, multi-output transmission gate.

10-5-2 SYNTHESIS OF MATRIX TRANSMISSION GATES

Consider the multi-input multi-output black box shown in Fig. 10-14, where the input and output signals are represented by $x_1(t), x_2(t), \ldots, x_m(t)$ and $y_1(t), y_2(t), \ldots, y_m(t)$, respectively. The switching signals are given, as usual, by $s_1(t), s_2(t), \ldots, s_n(t)$. This black box is called a *transmission gate* if for some specified combination of switchings, a number of preselected input signals appear at the output terminals. For example, Fig. 10-15 shows a circuit made up of coincidence gates.[1] This is easily seen by applying the v-shift theorem to shift $s_2(t)$ into two identical but separate sources. One of the two coincidence gates is made up of diodes D_1 and D_2 and is controlled by $s_1(t)$ and $s_2(t)$. The other gate consists of diodes D_3 and D_4 and is controlled by $s_2(t)$ and $s_3(t)$.

Observe that aside from the fact that the two coincidence gates share one common switching signal $s_2(t)$, they are completely independent of each other. The three switching signals can be used to select any desired combination of output signals. For example, if we want $y_1(t) = x_1(t)$ and $y_2(t) = 0$, we simply apply the signals $s_1(t) = s_2(t) = E$ and $s_3(t) = 0$. If we want $y_1(t) = 0$ and $y_2(t) = x_2(t)$, we apply the signals $s_1(t) = 0$ and $s_2(t) = s_3(t) = E$. If we want both $y_1(t) = x_1(t)$ and $y_2(t) = x_2(t)$, we apply the signals $s_1(t) = s_2(t) = s_3(t) = E$. Finally, if we want $y_1(t) = 0$ and $y_2(t) = 0$, then we apply any combination of the switching signals other than those considered above. Hence, with three switching signals we can select four possible combinations of the output signals.

Clearly, by an extension of this idea, it is possible to select any number of input signals to appear at the output terminals by applying a suitable combination of switching signals to an appropriate interconnection of coincidence gates. When more than two coincidence gates are used, it is convenient to draw the network in a more systematic form. One common configuration consists of an array or matrix of diodes such as the network shown in

[1] To simplify the schematic diagram, it is common practice to omit drawing all wires connecting voltage sources or current sources to a common terminal, usually called the ground.

Fig. 10-16, where there are 10 input signals, 10 output signals, and eight switching signals. Observe that the diodes in each row of this diode matrix constitute a coincidence gate. Hence, there are a total of 10 coincidence gates in this diode matrix. An examination of the transmission gate shows that by a suitable choice of four out of the eight switching signals, we can select any combination of input signals. For example, to obtain $y_9(t) = x_9(t)$, we have to apply only the switching signals $s_2(t) = s_4(t) = s_6(t) = s_7(t) = E$. On the other hand, if we want to have $y_2(t) = x_2(t)$ and $y_{10}(t) = x_{10}(t)$ simultaneously, then we must apply $s_1(t) = s_4(t) = s_6(t) = s_7(t) = s_8(t) = E$.

Exercise 1: Find what happens if the switching signals in Fig. 10-12 are allowed to become negative. What is its effect on the coincidence gate?

Exercise 2: Synthesize a multi-input bidirectional switch.

Exercise 3: Show how a coincidence gate may be synthesized to function as a chopper.

Exercise 4: Synthesize a coincidence gate capable of transmitting an input signal of both polarities.

Exercise 5: Design an electronic combination lock to be used in a bank vault. You may use one or more matrix transmission gates.

10-6 SYNTHESIS OF LOGIC-CIRCUIT BUILDING BLOCKS

Logic can be defined as the science of correct thinking. It dispenses with human intuition and concerns itself with the truth and falsity of statements as judged strictly from the light of a given set of axioms which define the rules of the game. For example, if we let

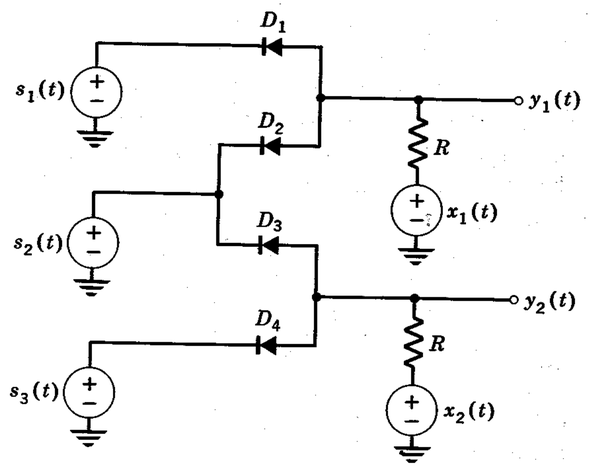


Fig. 10-15. An example of a transmission gate made up of two coincidence gates.

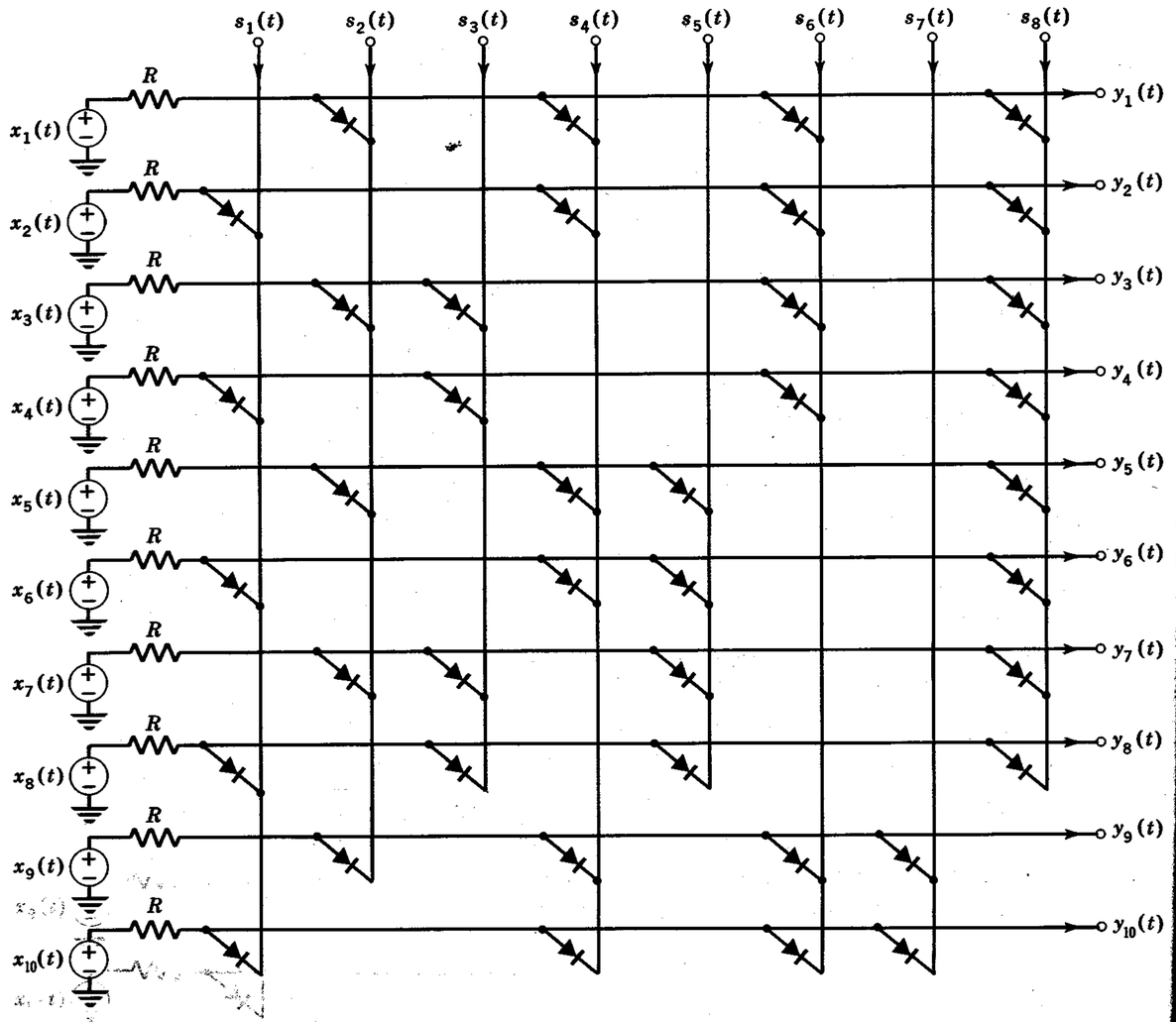


Fig. 10-16. An example of a matrix transmission gate containing 10 coincidence gates and eight switching signal sources.

x_1 and x_2 represent any two statements or propositions, each of which may either be true or false, and if we combine these statements to form a new statement y, then we may define a "rule" to the effect that statement y is true if, and only if, both statements x_1 and x_2 are true. Instead of stating this in so many words, we can express this rule by the following table:

x_1	x_2	y
True	True	True
True	False	False
False	True	False
False	False	False

Notice that this table is an equivalent and somewhat more precise way for stating the above rule. It is called a *truth table.* Instead of spelling out the words *true* and *false,* much time is saved by denoting them by symbols. It is customary to denote the word *true* by a 1 and the word *false* by a 0. It is important to realize that the 1 and the 0 are strictly symbols. They have no numerical significance whatsoever. Under this new notation, the above truth table becomes

x_1	x_2	y
1	1	1
1	0	0
0	1	0
0	0	0

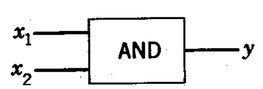
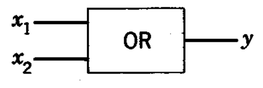
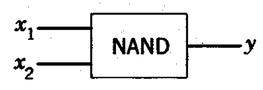
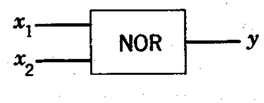
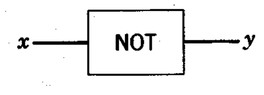
This particular rule is called a *logic AND function.* Since it is one of the most commonly encountered functions, it is tabulated in Table 10-1 with the four other common logic functions, namely, the *logic OR function,* the *logic NAND function,* the *logic NOR function,* and the *logic NOT function.*[1] Using these five logic functions as basic building blocks, we can synthesize an infinite variety of more complex logic functions. Such logic functions are indispensable in the design of automatic machines with a certain amount of built-in artificial intelligence. For example, a logic function can be found to perform all possible alternatives in the routing of elevators. They can be used in place of the mechanical system of cams in an automatic washing machine. In fact, they are the basic building blocks of all digital systems, including digital computers. The study of how to find the logic functions for performing a given task is usually given in a course called *switching circuit theory.* Our objective in this section will be to study how the five basic logic functions can be implemented by nonlinear networks. Once we have these networks, then we can interconnect them to realize any logic function we need, provided we are careful to take the loading effects into consideration.[2]

Since each input variable can assume only state 1 or state 0, we can easily represent these two states by two possible voltage or current levels. If we choose two convenient voltage levels E_1 and E_0 and associate the level E_1 with state 1 and level E_0 with state 0, then all we need to find are networks that will give an output voltage level corresponding to a combination of input voltage levels in accordance with the desired logic function. For reasons that will soon be obvious, the networks which realize the five basic logic functions in Table 10-1 are called AND gates, OR

[1] For simplicity, these functions are given only for one or two input variables; it should be recognized, however, that they (except for the NOT function) can be defined for any number of input variables.

[2] These five types of basic building blocks are now available commercially as black boxes with only the pertinent terminals brought out for external connections.

TABLE 10-1 *Five common logic functions and their defining truth tables.*

Logic function	Symbol	Truth table
AND		x_1 x_2 | y 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		x_1 x_2 | y 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NAND (NOT-AND)		x_1 x_2 | y 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR (NOT-OR)		x_1 x_2 | y 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
NOT		x | y 0 | 1 1 | 0

gates, NAND gates, NOR gates, and NOT gates. Since we are concerned only with stepwise signals which can assume one of two levels, E_1 or E_0, at any given time, we can apply the results in the preceding sections to realize the above logic gates. Again, for simplicity, we shall restrict our discussions to one or two input variables only. The extension to n input variables is quite obvious.

10-6-1 SYNTHESIS OF AND GATES

From the truth table for the AND gate in Table 10-1, we find a network which produces an output voltage $v_o(t) = E_1$ if, and only if, both input signals $v_1(t) = E_1$ and $v_2(t) = E_1$. Otherwise $v_o(t) = E_0$.

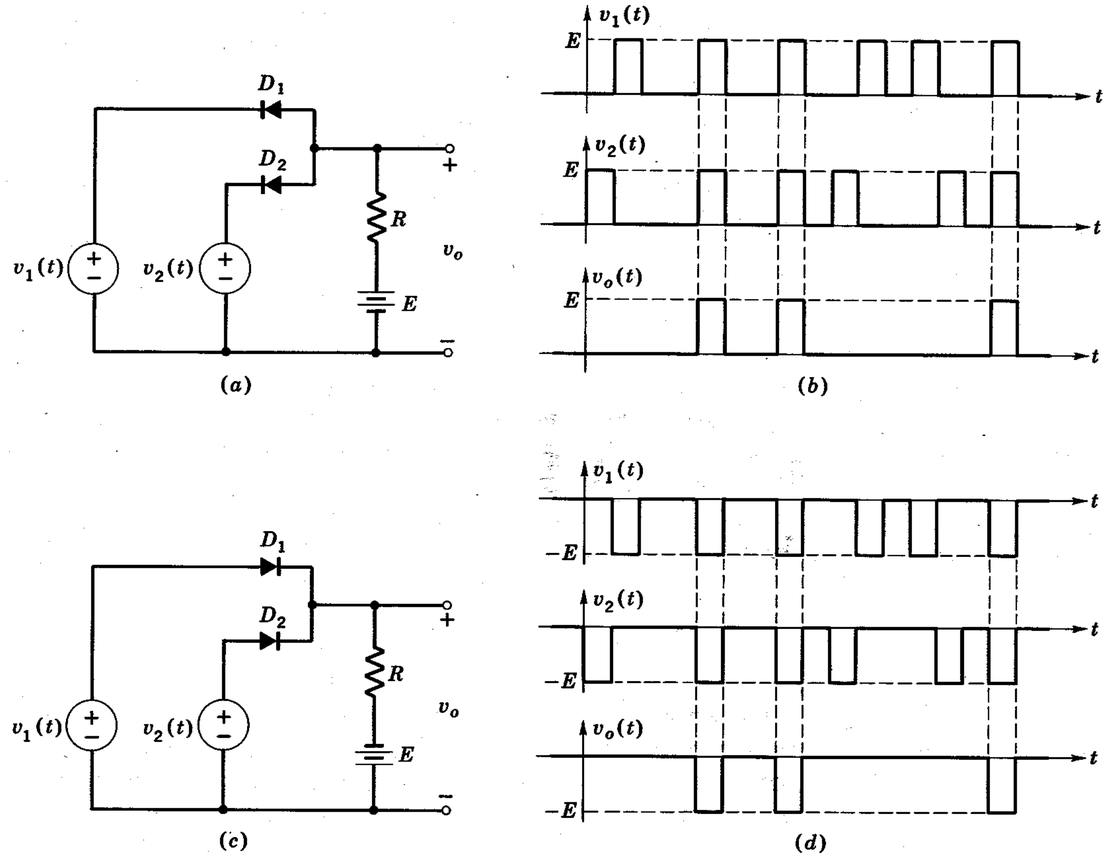


Fig. 10-17. Two circuits showing the complement of a positive logic AND gate is a negative logic AND gate.

Observe that this requirement can be satisfied by the *coincidence gate* shown in Fig. 10-13*a* with $v_{eq}(t) = E$ and with the switching signal amplitudes also set equal to E. In this case, our two switching levels are given by $E_1 = E$ and $E_0 = 0$. The resulting circuit is shown in Fig. 10-17*a* together with a set of typical input signals and the corresponding output signal as shown in Fig. 10-17*b*.

Notice that if we take the complementary network to the AND gate of Fig. 10-17*a* as shown in Fig. 10-17*c*,[1] we still obtain an AND gate provided we let the two levels be represented by $E_1 = -E$ and $E_0 = 0$. Notice that the waveforms shown in Fig. 10-17*d* are exactly the negative of the original waveforms in Fig. 10-17*b*. Since we are interested only in satisfying the truth table, the two AND gates in Fig. 10-17 are equally good realizations. In practice, however, sometimes one version is more convenient than the other. In order to distinguish between these two alternatives, however, it is customary to call the positive voltage version

[1] This is drawn in accordance with the complementary-network theorem in Sec. 7-8. Observe that we can either reverse the polarities of the two input voltage sources or keep the polarities but change the sign of the original voltage waveforms. We have elected to choose the latter alternative as shown in Fig. 10-17*d*.

the *positive logic AND gate* and negative voltage version the *negative logic AND gate.* In fact, in view of the complementary-network theorem, it is clear that each of the remaining logic gates in Table 10-1 can be classified into *positive logic gates* and *negative logic gates,* depending on whether the signal waveforms are positive or negative. In fact, as a very useful corollary to the complementary-network theorem, we can state the following:

POSITIVE-NEGATIVE LOGIC NETWORK CONVERSION THEOREM

Any positive (negative) logic gate or combinations of positive (negative) logic gates can be converted into a negative (positive) logic gate or combinations of negative (positive) logic gates by replacing all nonlinear resistors by their complements,[1] and by reversing the terminals of all dc voltage and current sources. The polarities of all ac sources remain unchanged, but the signs of all waveforms are changed to the negative of the original waveforms.

10-6-2 SYNTHESIS OF OR GATES

From the truth table in Table 10-1, an OR gate must give a nonzero output voltage $v_o = E_1$ when one or both of the input voltages are nonzero. The circuit shown in Fig. 10-18*a* is a simple realization of a two-input positive logic OR gate provided $E_1 = E > 0$ and $E_0 = 0$. In order to verify this realization, we only need to find the DP plot seen across the resistor as shown in Fig. 10-18*b* corresponding to a typical case $v_1(t) = E$ and $v_2(t) = 0$. Notice that in contrast with the case of a coincidence gate, the breakpoint of the DP plot is always equal to the *larger* of the breakpoint voltages of the component DP plots. This is why the breakpoint voltage of the DP plot of this circuit will never be zero as long as one input signal is not zero. The load-line construction shows that the circuit behaves exactly as a positive logic OR gate. A negative logic OR gate for this case is obtained simply by reversing the terminals of the diodes.

Logic gates using ideal diodes can often be analyzed by inspection using a few shortcuts which are peculiar to ideal diode networks. This is the *method of contradiction.* It is based on the observation that at any time, an ideal diode is either an open circuit or a short circuit. It is an open circuit if the voltage across the diode is negative, and a short circuit if the current flowing through the diode is positive.[2] In order to prove an assertion by the method of contradiction, we first assume that the assertion is not true, and

[1] Recall that the complements of ideal diodes are obtained by reversing their terminals; the complements of *p-n-p* (*n-p-n*) transistors are *n-p-n* (*p-n-p*) transistors; the complements of *p*-channel (*n*-channel) FETs are *n*-channel (*p*-channel) FETs.

[2] This rule is based on the usual reference direction and polarity as shown in Fig. 10-18*a*.

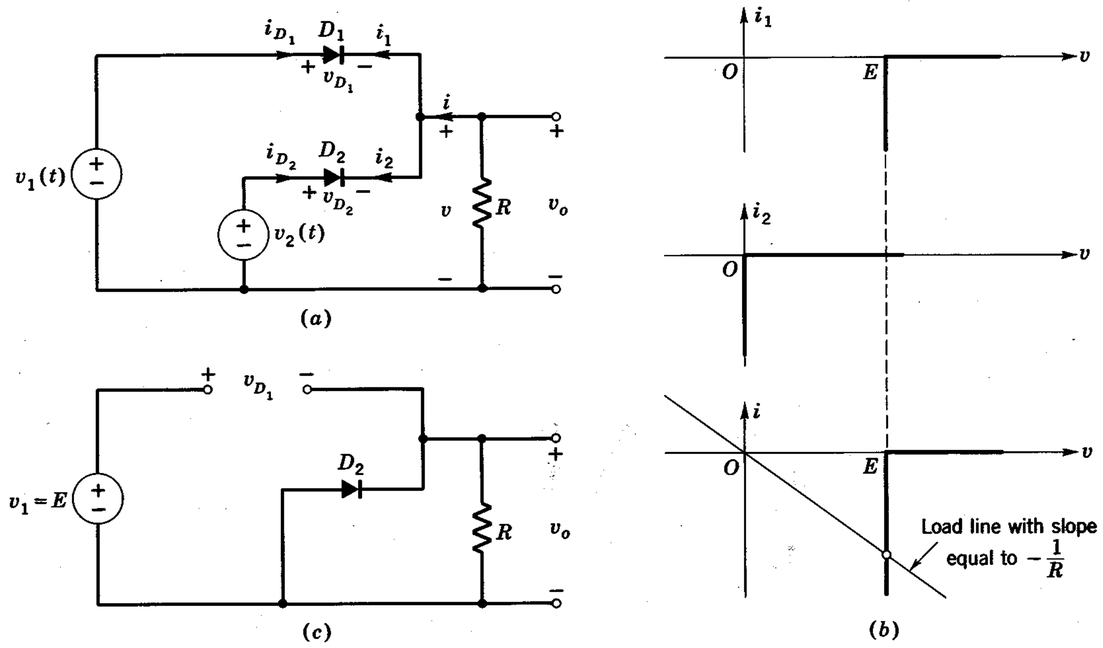


Fig. 10-18. The operation of a positive logic OR gate can be analyzed by either the graphical load-line method or the analytical method of contradiction.

going on this assumption, we try to establish a contradiction. If such a contradiction can indeed be established, then our original assumption is illegal, and hence the assertion is proved. The contradiction we seek consists of showing that the voltage across a supposedly open-circuited diode is positive. In the case of a supposedly short-circuited diode, we seek to show that the current flowing through it is negative. To illustrate this method, let us verify that the output voltage is equal to E when $v_1(t) = E$ and $v_2(t) = 0$. This assertion would require that diode D_1 be a short circuit. Hence, let us suppose the contrary and redraw the network as shown in Fig. 10-18*c* with D_1 replaced by an open circuit. This shows that $v_o = 0$ (since no current flows through the resistor R), and hence by KVL, $v_{D_1} = v_1 - v_o = E - 0 > 0$. But this contradicts the requirement that an ideal diode is an open circuit *only* if its terminal voltage is negative. This establishes the desired contradiction, and the assertion is proved.

With a little practice, it is possible to apply the method of contradiction mentally to a large class of ideal-diode logic circuits. It must be emphasized, however, that this method is applicable only for networks all of whose nonlinear elements are ideal diodes. If the ideal diodes are replaced by junction diodes, as is usually the case in practice, this method no longer applies, and