Three-Phase Quasi-Z-Source Inverter with Constant Common-Mode Voltage for Photovoltaic Application

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***Abstract*—In trasformerless grid-connected photovoltaic (PV) systems, common-mode voltage (CMV) fluctuations cause leakage current flow through the stray capacitance of the PV panels. Shoot-through (SH) states in a quasi-Z-source inverter (q-ZSI), increase the amplitude of high order harmonics of CMV. In this paper, by using the modulation technique based on odd PWM (OPWM) and minor change in the Z network of the three-phase q-ZSI, the leakage current is blocked. No extra semiconductor element is added. By the proposed technique, CMV is kept nearly constant during switching cycles. The experimental results for CMV analysis in a $1kW$ prototype are presented to verify the theoretical analysis.**

***Index Terms*— common-mode voltage, leakage current, Quasi-Z-Source inverter, photovoltaic power system, odd PWM.**

I. Introduction

Most of the installed PV systems are grid-connected. According to International Energy Agency Photovoltaic Power System report (IEA-PVPS Annual Report 2016), at the end of 2015, more than 99 % of the globally installed PV capacity (228 GW) were grid-connected. A transformerless PV system has higher efficiency and lower weight and size; but, by removing the galvanic isolation between the DC source and the grid, the leakage current issue is appeared [1]. The leakage current is originated from CMV fluctuations. In a transformerless system, the leakage current flows through the parasitic capacitance, mainly the stray capacitance between the PV array and the grounded PV frame. Safety issues may arise from this current [2]. Increasing radiated electromagnetic emissions, grid current distortions and losses are the other disadvantages of a transformerless structure [3].

Several methods are proposed for CMV and leakage current reduction in literatures [4]-[15]. Some methods are based on the structure modification adding some extra semiconductor elements to the main structure [4]-[7]. In [5], H7 topology, using seven switches, is proposed for CMV reduction in three-phase grid-connected system. Four-leg inverter with modified modulation technique is proposed in [6]. Structure-based methods usually increase the complexity and the cost of the system. Some other reduced CMV methods (RCM) are based on modulation modification which are less expensive and have simpler implementation. For example, active zero state PWM (AZSPWM), remote state PWM (RSPWM) and near state PWM (NSPWM) in [8]-[13] are all based on modulation modification. Interleaved carrier-based CMV reduction method introduced in [14], is another method from this type. RSPWM is the only method which can keep CMV constant in a classic voltage source inverter (VSI); however, it entails some limitations in the system. The amount of CMV reduction and the total performance of these methods are compared in [11] and [14]-[15].

Z-source inverter (ZSI) is a beneficial structure in PV applications with buck/boost characteristic in a single stage [16]-[18].Various structures are derived from the original ZSI structure and named as q-ZSIs [19]-[24]. q-ZSI with the structure shown in Fig. 1(a), is applied widely in distributed generation [21]-[26]. The hybrid structure of q-ZSI with battery storage is presented in [27]-[30]. q-ZSI shown in Fig. 1(a), has some advantages comparing with the traditional ZSI.

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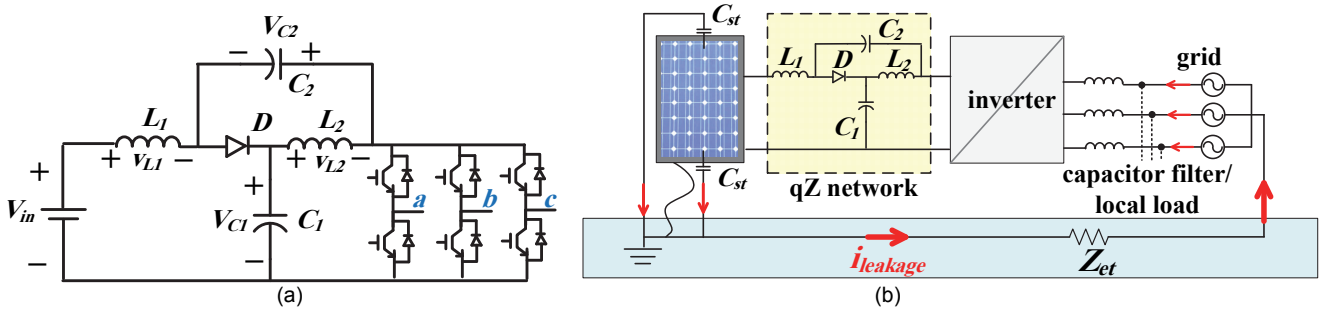


Fig. 1. Three-phase q-ZSI. (a) the main topology; (b) grid-connected q-ZSI with PV connection at the input: including the stray capacitors and the ground modeling impedance.

Its input current is continuous and the voltage across C_2 is much lower than that on C_1. The later leads to reduced passive component rating and lower manufacturing cost [31].

None of the modulation-based RCM methods is ideal for Z-source family inverters. Because of SH states, high-frequency harmonics of CMV are larger than those in a simple VSI and leads to higher disrupting leakage current. The leakage current path and the stray capacitance (C_{st}) in a q-ZSI are shown in Fig. 1(b). In [3], the three-phase ZSI with extra fast recovery diode (ZSI_D) is presented to decrease the leakage current in transformerless PV systems. ZSI_D applies odd and even PWM method (OEPWM). In ZSI_D, an extra fast recovery diode is connected to the negative terminal of the PV. The input diodes in ZSI_D provide isolation in terminals of the PV array from the inverter switches during SH states. In ZSI_D, the CMV still contains high-frequency harmonics. Although the leakage current is reduced in ZSI_D, but in practice, the leakage current could flow in both turning-on and off moments of diodes. In addition, using extra semiconductor element increases the cost of the system. In [32] the modified near state method is presented for CMV reduction in ZSI. Similarly, the CMV is not cancelled completely by using this method.

In this paper, by a minor change in the q-ZSI input inductor design, while using OPWM method (also called RSCMV1 [8]-[13]), the CMV is kept constant and the leakage current is completely blocked. In section II, the main topology of q-ZSI is reviewed. The CMV is analyzed in a three-phase q-ZSI in section III. In section IV, OPWM is described and the implementation of the proposed CMV reduction method is presented. The detailed experimental results presented in section V show that the CMV and the leakage current are canceled in three-phase q-ZSI by using the proposed method.

II. SVM-BASED QUASI-Z-SOURCE INVERTER

The q-ZSI shown in Fig. 1(a), has two operating modes [33]:

1) Inverter mode: Similar to classic inverters, in this mode, q-ZSI has six active vector states and two zero states. This mode is named as "non-shoot-through mode" or "inverter mode". In this mode, the input current flows through the input side diode (D in Fig. 1(a)) and the q-ZSI impedance network capacitors (C_1 and C_2) are charged during this mode.

2) Shoot-through mode: In this mode, the inverter is shorted by its one, two or all three legs. In this mode, the network diode (D in Fig. 1(a)) is turned off via the reveres-bias voltage and the impedance network capacitors charge the two inductors (L_1 *and* L_2) at the same time.

The voltage across the leg terminals during SH mode is approximately zero and during inverter mode is equal to:

$$V_{DC} = B \times V_{in} \tag{1}$$

V_{in} shown in Fig. 1(a), is the input DC source. In (1), B is the boost factor of a q-ZSI and is defined as,

$$B = \frac{1}{1-2D_{sh}} \tag{2}$$

D_{sh} in (2) is the relative duration of SH state in a switching period which is obtained by the controller. The value of D_{sh} is calculated based on source voltage or as an output variable of the maximum power point tracking (MPPT) module, or as a control output which is compatible with the battery situation in a hybrid q-ZSI [34]. In a simple q-ZSI, V_{DC} is usually regulated by a voltage control loop through D_{sh} adjustment.

In steady state, the impedance network capacitors voltage are obtained as ([33]):

$$V_{C1} = (1 - D_{sh})V_{DC} \tag{3}$$

$$V_{C2} = (D_{sh})V_{DC} \tag{4}$$

In SVM method, there are six active switching states and two zero states. Fig. 2, shows the voltage space vectors and A-type sectors in αβ plane. In addition to the eight traditional switching states of a VSI, in a q-ZSI, there are seven SH states; when both the upper and lower switches of one or multiple phase legs are on [3].

The duration of the vectors in a switching cycle is calculated like that of a simple SVM inverter [35]. For example, if the reference vector is in the first sector (A_1 in Fig. 2), the duration of the active and passive vectors are obtained as below [35]:

$$T_{\mathrm{a}} = \frac{\sqrt{3}}{2} M_{qz} T_{sw} \sin\left(\frac{\pi}{3} - \theta\right), \theta = \omega_m t \ (0 \le \theta < \frac{\pi}{3}) \tag{5}$$

$$T_{\mathrm{b}} = \frac{\sqrt{3}}{2} M_{qz} T_{sw} \sin(\theta) \tag{6}$$

$$T_0 = T_7 = 0.5(\mathrm{T_{sw}} - T_{\mathrm{a}} - T_{\mathrm{b}}) \tag{7}$$

In (7), T_0 refers to the duration of the passive state in which the three lower switches are on (V_0 vector); while T_7 is related to the interval in which the three upper switches are on (V_7 vector). T_{sw} is the switching period and ω_m is the line frequency. M_{qz} is modulation index in q-ZSI, where:

$$M_{qz} = \frac{Vref}{\frac{V_{in}}{2} \times B} = \frac{Vref}{\frac{V_{DC}}{2}} \tag{8}$$

The modulation index definition in q-ZSI is similar to a traditional VSI.

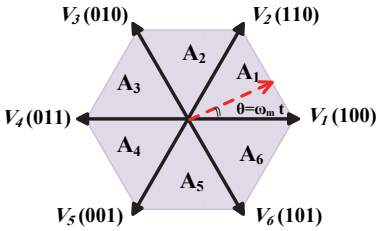


Fig. 2. The space vectors and A-type sectors in SVM method.

TABLE I
THE CMV VALUES IN Q-ZSI

Vector	CMV
$\vec{V}_1, \vec{V}_3, \vec{V}_5$(odd vectors)	$\frac{V_{DC}}{3}$
$\vec{V}_2, \vec{V}_4, \vec{V}_6$(Even vectors)	$2\frac{V_{DC}}{3}$
$\vec{V}_7(zero\ vetor)$	V_{DC}
$\vec{V}_0(zero\ vector)$	0
$\vec{V}_{sh} * (shoot\ through\ vector)$	0

* Seven vectors for the shoot through states.

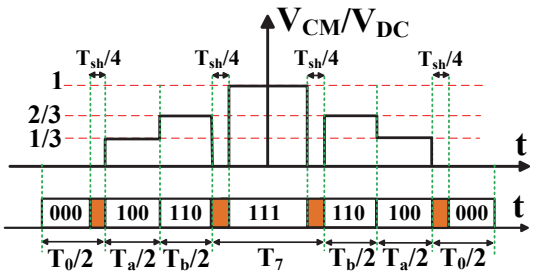


Fig. 3. The switching states and the CMV waveform for SVM-based q-ZSI during a switching period in A_1 sector.

III. Common Mode Voltage in Quasi-Z-Source Inverter

The CMV for three-phase inverter is defined as [3]:

$$V_{CM} = \frac{V_{aN}+V_{bN}+V_{cN}}{3} \tag{9}$$

Table I, shows the switching states and the CMV values in a q-ZSI. The CMV waveform in q-ZSI is not uniform within a switching period and it includes step variations. For example as it is seen in Table I, applying odd and even states cause $1/3V_{DC}$ and $2/3V_{DC}$ levels in the CMV waveform respectively. Therefore, the arrangement of odd, even and zero states affects the CMV waveform and it can be concluded that, the CMV waveform is changed by applying different modulation techniques. The arrangement of the state vectors and SH intervals during a switching period (in A_1 sector) for a SVM-based q-ZSI is shown in Fig. 3, in which the SH intervals are determined by the filled rectangles. The CMV waveform for this switching cycle is also depicted in Fig. 3. The fluctuations in the CMV waveform leads to leakage current flow in the grid-connected PV system.

In [36]-[37], the equivalent circuit for the common mode current flow in three-phase inverters is presented. The equivalent circuit is shown in Fig.4. L_f and R_f in Fig. 4 are the line inductance filter elements, scaled by one-third in the equivalent circuit. The CMV obtained from (9) is used to estimate the leakage current. The stray capacitance is about $50–150nF/kW$ [36]. The ground impedance, Z_{et}, has an uncertain value and is mostly resistive. It might be around a few Ohms. The equivalent impedance through the path (for the frequency of ω_k) equals to:

$$Z_{leakage}(j\omega_k) = Z_{et} + \frac{(j\omega_k)L_f}{3} + \frac{R_f}{3} + \frac{1}{2(j\omega_k)C_{st}} \tag{10}$$

If the CMV includes the harmonic of ω_k, the effect of this harmonic appears in the leakage current due to the path impedance. According to (10), the path impedance for zero frequency is infinite; therefore, theoretically there is no DC current flow in the circuit.

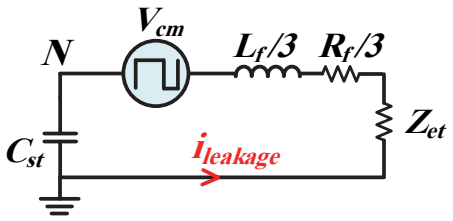


Fig. 4. The equivalent circuit for leakage current flow [37].

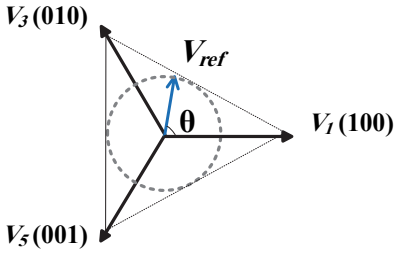


Fig. 5. The odd vectors and sectors in OPWM method.

IV. Odd Vector PWM Method

Using only the odd vectors in OPWM method or the even vectors in even PWM (EPWM) are two similar ways to CMV cancellation in VSIs, which are presented in literature as [3] and [32]. In OPWM method, only the odd vectors (V_1, V_3, V_5) are used to compose the output reference vector. As shown in Fig. 5, in this method, the αβ plane is divided in three sectors. According to [3], in a classic VSI, the relative time for each odd vector in a switching period $(\tau_i, i = 1,3,5)$ is calculated as:

$$\begin{cases} \tau_1 = \frac{1}{3} + \frac{|V_{ref}|}{U_{in}}\cos(\theta) \\ \tau_3 = \frac{1}{3} + \frac{|V_{ref}|}{U_{in}}\sin(\theta - \frac{\pi}{6}) \\ \tau_5 = \frac{1}{3} + \frac{|V_{ref}|}{U_{in}}\sin(-\theta - \frac{\pi}{6}) \end{cases} \tag{11}$$

In (11), U_{in} is the DC voltage across the leg terminals, and θ equals to the reference phase angle.

OPWM method is applicable in q-ZSI. From vector calculations, the relative duration for odd vectors in a q-ZSI are obtained as:

$$\begin{cases} \tau_1 = \frac{1}{3} - \frac{D_{sh}}{3} + \frac{|V_{ref}|}{V_{DC}}\cos(\theta) \\ \tau_3 = \frac{1}{3} - \frac{D_{sh}}{3} + \frac{|V_{ref}|}{V_{DC}}\sin(\theta - \frac{\pi}{6}) \\ \tau_5 = \frac{1}{3} - \frac{D_{sh}}{3} + \frac{|V_{ref}|}{V_{DC}}\sin(-\theta - \frac{\pi}{6}) \end{cases} \tag{12}$$

One-third of SH duration could be applied between each two odd vectors.

A. Scalar Implementation of OPWM in DSP

For scalar implementation of OPWM in DSP-controlled inverters, "timer phase shift" method is proposed. In Fig. 6, the timer signals and the switching commands are depicted for OPWM method. "Timer_a", "Timer_b," and "Timer_c" are related to the phases "a","b" and "c" respectively. The period of timers, PRD, is selected due to the switching period. "Timer_a" is assumed the reference timer. Using (12), in each switching cycle the phase of timers are set as:

$$\begin{cases} phs_a = 0 \\ phs_b = PRD - PRD \times (\tau_1 + \frac{D_{sh}}{3}) \\ phs_c = PRD - PRD \times (\tau_1 + \tau_3 + \frac{2D_{sh}}{3}) \end{cases} \tag{13}$$

The compare signals values $(CMPR_{iH}, CMPR_{iL}, i = a,b,c)$ for S_{iH} and S_{iL} switches equal to:

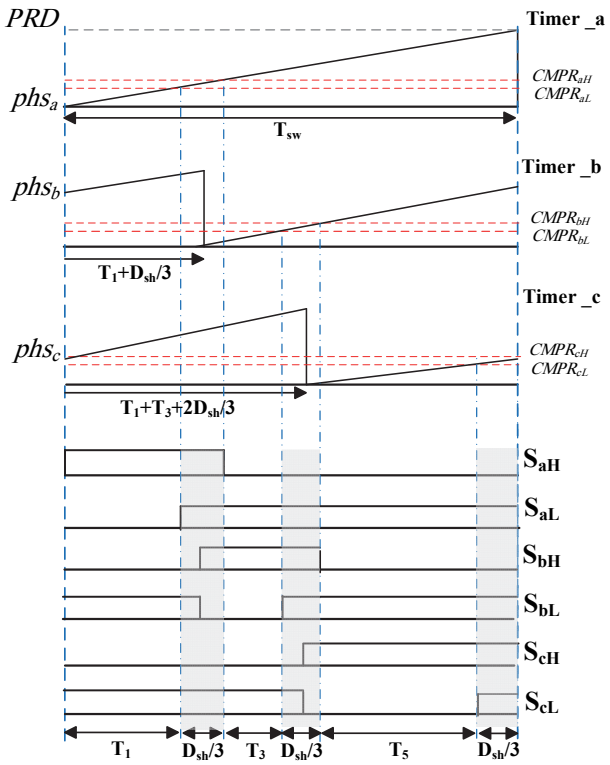


Fig. 6. Timer phase shift method for scalar implementation of OPWM in DSP-controlled q-ZSI.

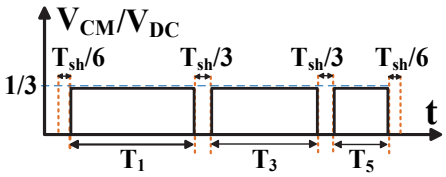


Fig. 7. The CMV in q-ZSI using OPWM modulation technique.

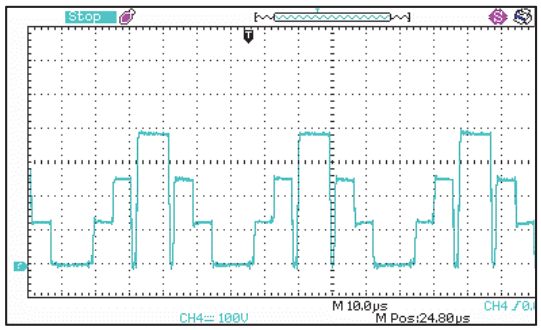
$$\begin{cases} CMPR_{aH} = PRD.(\tau_1 + \frac{D_{sh}}{6})\,;\; CMPR_{aL} = PRD.(\tau_1 - \frac{D_{sh}}{6}) \\ CMPR_{bH} = PRD.(\tau_3 + \frac{D_{sh}}{6})\,;\; CMPR_{bL} = PRD.(\tau_3 - \frac{D_{sh}}{6}) \\ CMPR_{cH} = PRD.(\tau_5 + \frac{D_{sh}}{6})\,;\; CMPR_{cL} = PRD.(\tau_5 - \frac{D_{sh}}{6}) \end{cases} \quad (14)$$

In Fig. 6, the compare signals are shown.

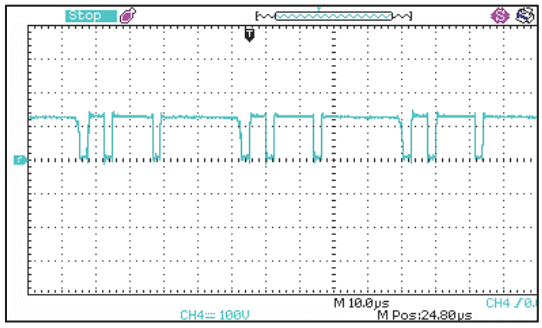
B. Common-Mode-Voltage in OPWM q-ZSI

Due to SH states between odd vectors, applying OPWM method in q-ZSI doesn't lead to a constant CMV (unlike traditional VSI). In Fig. 7, the typical CMV waveform for OPWM q-ZSI is depicted. Comparing with CMV in SVM q-ZSI in Fig. 3, the step variations of CMV are reduced in OPWM method, but the CMV still contains high-frequency harmonics.

A q-ZSI with specification shown in Table II is considered as an example. The CMV for SVM and OPWM methods are shown in Fig. 8(a) and Fig. 8(b) respectively. V_{DC} , D_{sh} and M_{qz} equals 380v, 0.15 and 0.6. The CMV harmonics are measured through a high-frequency spectrum analyzer (Agilent HP 8561B) and shown in Fig. 9(a)-(b) for SVM and OPWM methods respectively. From Fig. 9 (a)-(b), it is seen that, for the same leg voltage and the same modulation index, using OPWM method in q-ZSI results in CMV harmonic reduction, but the issue of high-frequency harmonics is not disappeared completely. Considering that the leg voltage in OPWM method is larger than in SVM, the harmonics are even larger than shown in Fig. 9(b).

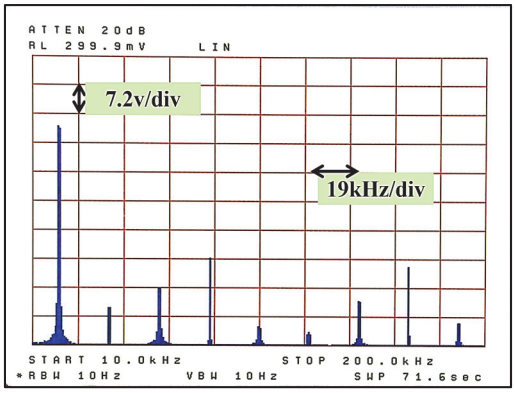


(a)

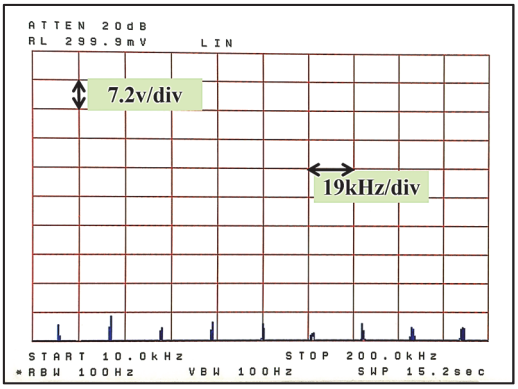


(b)

Fig. 8. The CMV waveform of the q-ZSI. (a) using SVM modulation; (b) using OPWM modulation.



(a)



(b)

Fig. 9. The CMV harmonics. (a) Using SVM method. (b) Using OPWM method.

C. Modified quasi –Z-Source using Odd-PWM

According to (3)-(4), the voltage across the Z network inductor (with the polarity shown in Fig. 1(a)) during the inverter and SH modes is calculated as:

$$\begin{cases} v_{L1} = v_{L2} = -D_{sh}V_{DC} & : inverter\ mode \\ v_{L1} = v_{L2} = (1 - D_{sh})V_{DC} & : SH\ mode \end{cases} \quad (15)$$

The CMV waveform in OPWM method and typical voltage across the inductor L_1 (v_{L1}), are depicted in Fig. 10. In despite of the CMV waveform, v_{L1} , equals its maximum value in SH intervals ($(1 - D_{sh}).V_{DC}$) and during the inverter mode it has its minimum value ($(-D_{sh}).V_{DC}$).

As shown in Fig. 11, the input inductor is divided to two series inductors, L'_1 and $''_1$, with the ratio of x, where:

$$\begin{cases} L'_1 = xL_1 \\ L''_1 = (1-x)L_1 \end{cases} \Rightarrow \begin{matrix} v'_{L1} = xv_{L1} \\ v''_{L1} = (1-x)v_{L1} \end{matrix} \quad (16)$$

CMV in this case is obtained as:

$$CMV = \frac{V_{AN}+V_{BN}+V_{CN}}{3} = v'_{L1} + \frac{V_{AN'}+V_{BN'}+V_{CN'}}{3} \quad (17)$$

The node, N', is shown in Fig. 11. From (15) and Table I, CMV is equal to:

$$CMV = \begin{cases} x\,(-D_{sh}V_{DC}) + V_{DC}/3 & : inverter\ mode \\ x(1 - D_{sh})V_{DC} + 0 & : SH\ mode \end{cases} \quad (18)$$

The CMV waveform becomes constant, if x equals $1/3$. In other words, if L'_1 and L''_1 are selected as $1/3L_1$ and $2/3L_1$, the CMV is equal to a constant value:

$$CMV = \frac{(1-D_{sh})V_{DC}}{3} \quad (19)$$

q-ZSI with two-piece input inductance is named as modified q-ZSI (mq-ZSI). CMV in mq-ZSI using OPWM is a DC voltage, without high-frequency harmonics.

D. OPWM Comparing with SVM

As presented in [3], the modulation index in OPWM method is limited to 0.61, while in SVM it is limited to 1.15.

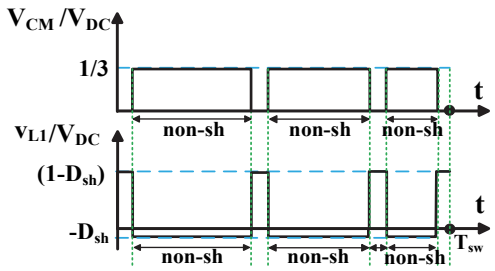


Fig. 10. The typical voltage across the network inductor comparing with the CMV.

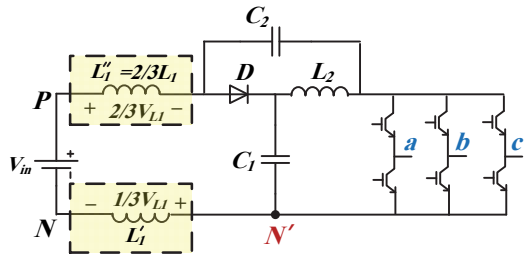


Fig. 11. mq-ZSI main structure.

This means that, in OPWM method, higher DC voltage is required at the leg terminals and the input source. However, in Z-source family inverters, SH intervals boosts the leg terminals voltage and the problem of need to a higher input voltage could be rather relieved.

In SVM method, the passive state is implemented through zero vectors (V_0 and V_7), while in OPWM method, it is implemented through applying equally the three odd vectors. For example, if the relative passive time is D_{psv} in OPWM method, each odd vector is applied for $T_{sw} \times D_{psv}/3$. The relative passive duration in OPWM method is equal to:

$$D_{psv}\,(\theta) = 3 \times min\{\tau_1, \tau_3, \tau_5\} \quad (20)$$

In Z-source family, SH duration shouldn't exceed the passive duration; therefore, for proper operation of the inverter using OPWM, it is concluded:

$$D_{sh} \le min\left(D_{psv}(\theta)\right) \quad (21)$$

From (12) and (20)-(21), it can be said:

$$D_{sh} \le 1 - \frac{3}{2}M_{qz} \quad (22)$$

Using SVM method, the permitted range for D_{sh} is obtained, as:

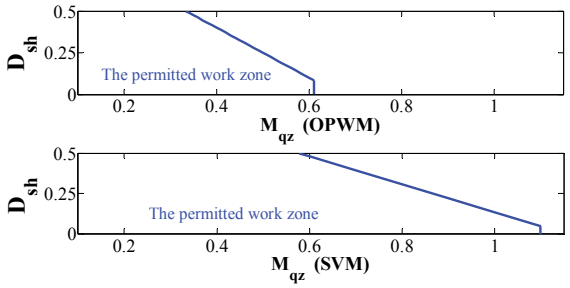


Fig. 12. The permitted work zones in q-ZSI using SVM or OPWM.

TABLE II
THE TOTAL SPECIFICATION OF THE DESIGNED PROTOTYPE.

line to neutral voltage	$V_g = 110V$	**line frequency**	$f_m = 50Hz$
Z network capacitance	$C_1 = C_2 = 220uF$	**Z network inductance**	$L_1 = L_2 = 1mH$

TABLE III
SVM AND OPWM METHODS PARAMETERS FOR THE Q-ZSI.

	SVM	OPWM
permitted input voltage (V_{in})	160V-357V	342V-554V
permitted SH duration (D_{sh})	0.03-0.29	0.03-0.21
the peak of leg voltage (V_{DC})	380v	590v
modulation index (M_{qz})	0.82	0.53

TABLE IV
SIMULATION RESULTS FOR SVM Q-ZSI AND OPWM MQ-ZSI

$2C_{st}$	current THD		voltage THD		leakage current	
	SVM q-ZSI	OPWM mq-ZSI	SVM q-ZSI	OPWM mq-ZSI	SVM q-ZSI	OPWM mq-ZSI
0	1.8%	4.8%	128%	195%	0	0
$150nF^*$	62%	4.8%	130%	195%	15.3A	$4mA$
$250nF$	7.6%	4.8%	128%	195%	1.74A	$2mA$
$350nF$	5.2%	4.8%	129%	195%	1.52A	$2mA$
$450nF$	4.1%	4.8%	128%	195%	0.84A	$1mA$

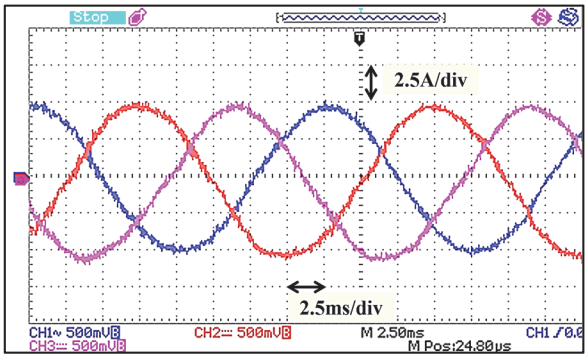
*Resonant frequency of the leakage impedance is equal to $1/T_{sw}$

$$D_{sh} \le 1 - max\left(\frac{Ta+Tb}{T_{sw}}\right) \Rightarrow D_{sh} \le 1 - \frac{\sqrt{3}}{2} M_{qz} \qquad (23)$$

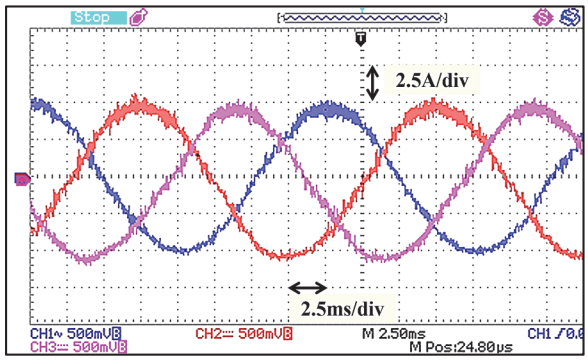
The permitted range of D_{sh} due to the modulation index is shown in Fig. 12 for both SVM and OPWM methods. To have a boost factor of 2 ($D_{sh} = 0.25$), the modulation index should be designed less than 0.5 and .87 in OPWM and SVM methods respectively.

The output voltage total harmonic distortion (THD) in OPWM is larger than that in SVM method. In [11], a total comparison is done for THD levels in different RCM methods. Flowing leakage current increases THD level in the output current, while THD of the output voltage is not significantly affected. Two $3kW$ systems with specification shown in Table II-III are designed and simulated. Due to (22)-(23), the permitted input voltage and D_{sh} ranges for the selected M_{qz} are shown in Table III. The THD levels of the output currents and voltages and also the amount of leakage current for different values of stray capacitance are shown in Table. IV. The blocking voltage of the IGBTs is $600V$. The inverter output filter inductance is $6mH$ and the switching frequency is equal to $9.2kHz$. For the stray capacitance of 150nF, the resonant frequency of the leakage current path is equal to the switching frequency, which leads to the worst case THD and leakage current in SVM q-ZSI. In Table IV, D_{sh} equals its maximum value and V_{DC} is less than $600V$ in both SVM q-ZSI and OPWM mq-ZSI. The voltage rating of the IGBTs limits the lower value of M_{qz} ($M_{qz} \ge 0.51$) and also due to practical considerations, D_{sh} is not selected higher than 0.3. While in SVM q-ZSI the maximum practical level of D_{sh} is achievable by selecting 0.82 for M_{qz}, D_{sh} maximum value is lower in OPWM q-ZSI because of M_{qz} lower value limitation (Table III). In the simulation, Z_{et} is zero. The current THD in SVM q-ZSI, is affected by the value of stray capacitance, while this parameter is constant in OPWM mq-ZSI. As shown in Table IV, for zero leakage, the current THD in SVM q-ZSI and OPWM mq-ZSI are 1.8% and 4.8% respectively. The current THD is increased to 62% for 150nF stray capacitance in SVM q-ZSI while it is constant in OPWM mq-ZSI. Due to higher voltage THD in OPWM mq-ZSI comparing to SVM mq-ZSI, larger output inductance is required to have the same current THD level. However, higher leakage current increases significantly current THD in SVM q-ZSI.

In OPWM q-ZSI, L'_1 and L''_1 tolerances affect their ratio, and consequently the leakage current; but, for a small tolerance this effect is negligible. For example, $\pm 5\%$ and $\pm 10\%$ tolerance in the inductors values (for the case of 150nF stray capacitor), leads to the leakage currents of 7mA and 20mA respectively for the worst case.



(a)



(b)

Fig. 14. The three-phase output current; RMS value is 3.5 A (the sensor gain is 200mv/A). (a) using SWM; (b) using OPWM.

V. THE EXPERIMENTAL RESULTS

A low-voltage q-ZSI prototype is designed and both SVM and OPWM control methods are implemented. The total specification of the system is shown in Table II-III. The inverter output inductance and the switching frequency are $3mH$ and $21kHz$. The implemented prototype is shown in Fig. 13. The digital signal processor, TMS320F2808 is used as the main controller, providing the switching and the protection commands. The phase locked loop (PLL) based on dq transformation is implemented for being synchronized to the grid when the system is grid-connected. Isolated voltage and current measurements are provided by LEM sensors, the measured values from the sensors are transferred to the

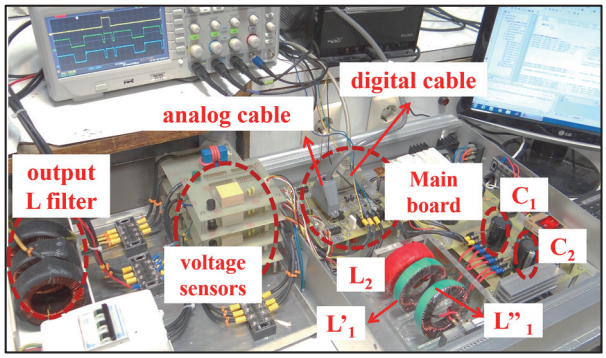


Fig. 13. The designed prototype for q-ZSI.

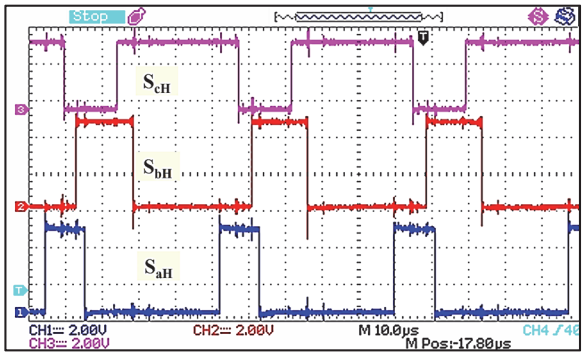
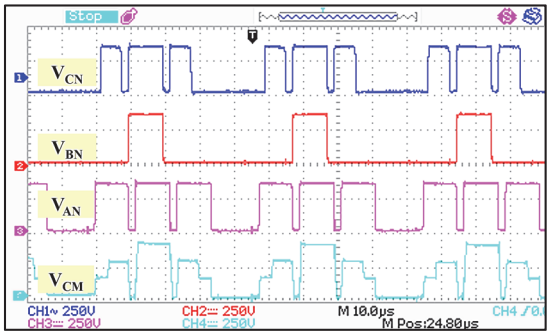
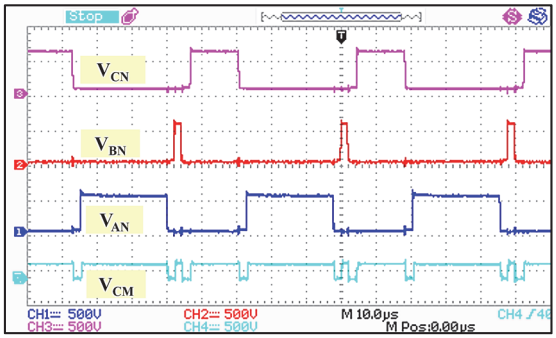


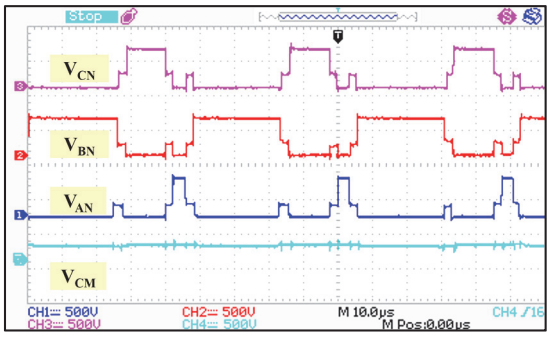
Fig. 15. The upper switches commands by timer phase shift method.



(a)

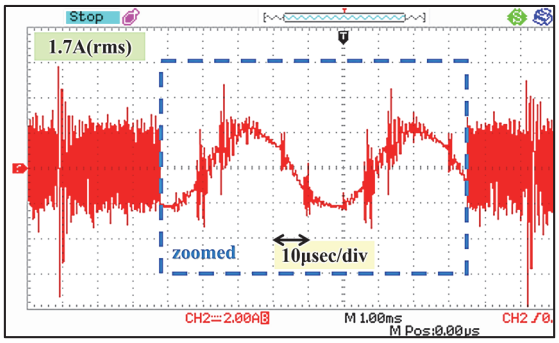


(b)

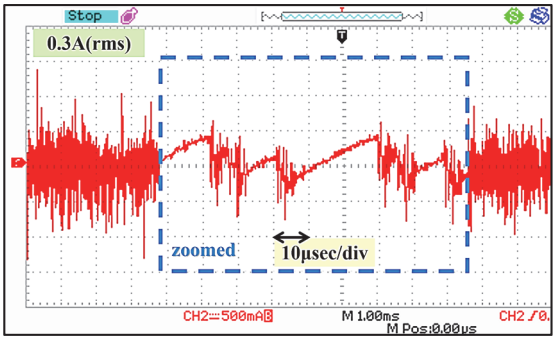


(c)

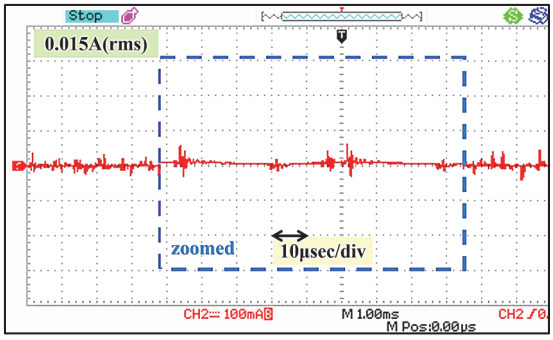
Fig. 16. The phase terminals output voltage and the CMV voltage (a) SVM q-ZSI; (b). OPWM q-ZSI; (c) OPWM mq-ZSI.



(a)



(b)



(c)

Fig. 17. The leakage current. (a) SVM q-ZSI; (b). OPWM q-ZSI; (c) OPWM mq-ZSI.

processor by the analog cable (shown in Fig. 13). The PV input voltage is modeled with a DC supply voltage. The module FSBS15CH60 from FAIRCHILD is used as the power converter, at the bottom of the main board in Fig. 13. L_1' and L_1'' in Fig. 13 is nearly equal to $333\mu H$ and $666\mu H$ respectively. The output phase currents (without leakage current) for SVM and OPWM methods are shown in Fig. 14(a)-(b). The RMS value of the output current equals 3.5A. The prototype system provides 1.2kW.

The upper switches commands for "phase shift method" in OPWM scalar implementation are shown in Fig. 15. The odd vectors ($\boldsymbol{V_1}$, $\boldsymbol{V_3}$ and $\boldsymbol{V_5}$) are implemented by the pulses shown in Fig. 15, with the same order depicted in Fig. 6. For example, S_{aH} pulse duration in Fig. 15, represents $\boldsymbol{V_1}$ duration and a part of SH state. The odd vector transitions occur in SH intervals.

The CMV and the output terminals voltage of the q-ZSI are measured for SVM and OPWM methods. In Fig. 16(a)-(b), the CMV of the q-ZSI is shown for SVM and OPWM methods respectively. The CMV waveforms in Fig. 16(a)-(b), have the typical forms of the CMV in a SVM q-ZSI (Fig. 3) and OPWM q-ZSI (Fig. 7). Although the leg terminal voltage is increased by the factor of 1.5 in Fig. 16(b), the CMV step variations are decreased compared to that shown in Fig. 16(a). The CMV fluctuations in Fig. 16(b) is due to SH states which can be identified by zero-voltage intervals. The output terminals voltages (V_{aN}, V_{bN} and V_{cN}) in Fig. 16(b) contain uniform step variations with the amplitude of $590V$. In Fig. 16(c), the CMV for OPWM mq-ZSI is depicted. Using a two-piece inductor at the input of q-ZSI, non-uniform fluctuations with the amplitude of approximately $200V$ are added to the output terminals voltages. The CMV in Fig. 16 (c) is nearly constant and is equal to $170V$. A little glitch is seen on the CMV at SH moments. Considering $150nF$ stray capacitor and zero ground impedance, the leakage current is measured for SVM q-ZSI, OPWM q-ZSI and OPWM mq-ZSI. The results are shown in Fig. 17(a)-(c). SVM q-ZSI has the maximum leakage current, equals to 1.7A rms. The most dominant harmonic in Fig. 17(a) is $21kHz$ (switching frequency). In OPWM q-ZSI, the leakage current is reduced significantly and

is equal to 0.3A; this current is shown in Fig. 17(b). In Fig. 17(b), the higher order switching harmonics are also seen in the waveform. In mq-ZSI, by redesigning the input inductor, the leakage current is reduced to its smallest value of about 15mA. Higher amplitude leakage current (as in Fig. 17(a)) affects strongly the output current THD. In SVM q-ZSI, OPWM q-ZSI and mq-ZSI (which their leakage currents are shown in Fig. 17(a)-(c)) the output currents THD are 22.2%, 9.6% and 8.4% respectively.

VI. Conclusion

In this paper, by using OPWM modulation technique and minor change in q-ZSI structure, the leakage current is blocked. Applying existing CMV reduction methods as OPWM method in the traditional q-ZSI doesn't result in constant CMV, because of SH intervals. In the example case, by applying OPWM, the leakage current is reduced significantly. By a minor change in the Z network filter design and applying OPWM, it is possible to keep the CMV as a nearly constant value. No extra semiconductor element is added to the converter; only the input inductor is splitted into two parts. The voltage variations of CMV is compensated with the inductor connecting to the negative terminal.

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